# LTM170E4 Information

Date : Aug. 25, 2000
Customer :

**Prepared By Ji Hoon Kim**
**Checked By Yoo Dong Jo**

**LCD Application Engineering Group**
**AMLCD Division**

## 1. Changing Items

| Item | | | LT170E2 | LTM170E4 | Note |
|---|---|---|---|---|---|
| Mounting Method | | | Front mounting | Front/Side mounting | *Compact & Slim<br><br>*For compatibility, mounting bracket should be attached to E4 model.<br>-> Refer to the figure 2.3 |
| Out-Dim. | Module size (mm; H*V*D) | | 404x 322x 25(Max) | 383.5x 306x 22.8(Max) | |
| | User hole | Hor. | 394.0± 0.3 | 374.0± 0.3 | |
| | | Ver. (Left/Right) | 310.2/215.0± 0.3 | 269.0/257.8± 0.3 | |
| | Bezel opening (mm; H*V) | | 342.0*274.4 | 341.52*273.936 | *System housing should be designed to avoid the interference<br>-> Refer to the figure 2.1 & 2.2 |
| Connector | I/F Connector | | JAE FI-WE31P-HF<br>( 31 Pin ) | JAE FI-X30S-HF<br>( 30 Pin ) | E2:TMDS, E4:LVDS(2 CH) |
| | Location | | The connector of the E4 is located somewhat to the right lower side than E2. | | ->Refer to the figure 2.3 |
| | B/L Connector | | JST<br>BHR - 04VS - 1<br>( 4Pin X 1 ) | JST<br>BHSR - 02VS - 1<br>( 2Pin X 2 ) | *Inverter should be changed. |

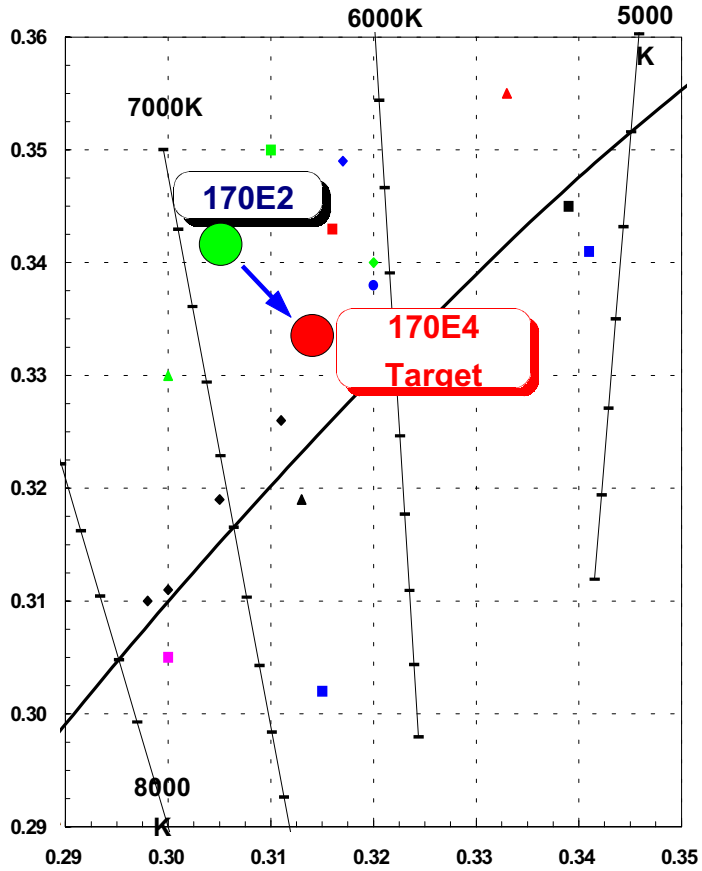
## 1.1 Module Size

- ✓ More **Compact size** : 404 x 322 x 25(Max) => 383.5x 306x 22.8(Max)
- ✓ Mechanical compatibility with LT170E2 model : **additional bracket** is needed.

## 1.2 Optical Characteristics

- ✓ Color coordinate is approached near to **Black-body Temp**.
  0.305, 0.342 => 0.318, 0.339
- ✓ Color Gamut is improved : 50% => **60%**
- ✓ Brightness is improved : 170nits (typ.) => **200nits** (typ.)
- ✓ Response Time : 70ms (typ.) => **35ms** (typ.)

▶ **More suitable for multi-media application.**




## 1.3 Interface

- ✓ Changed from TMDS to **LVDS.(2 Channel)**
  .LVDS Rx is merged into Timing controller IC.
- ✓ Input connector : 31pin => **30pin**

## 1.4 Back-light Unit

- ✓ Lamp connector : 4pin x 1ea => 2pin x 2ea
- ✓ Possible to insert feed-back circuit in design of inverter.

# 2. Mechanical Change

## 2.1 Bezel Opening

- Active area is same as E2, but bezel opening size is reduced.
- Therefore, Horizontal and vertical width of B/M (margin between top-chassis and active area) is reduced from 2.04mm to 1.8mm. ☞ **Refer to the Figure 2-1**

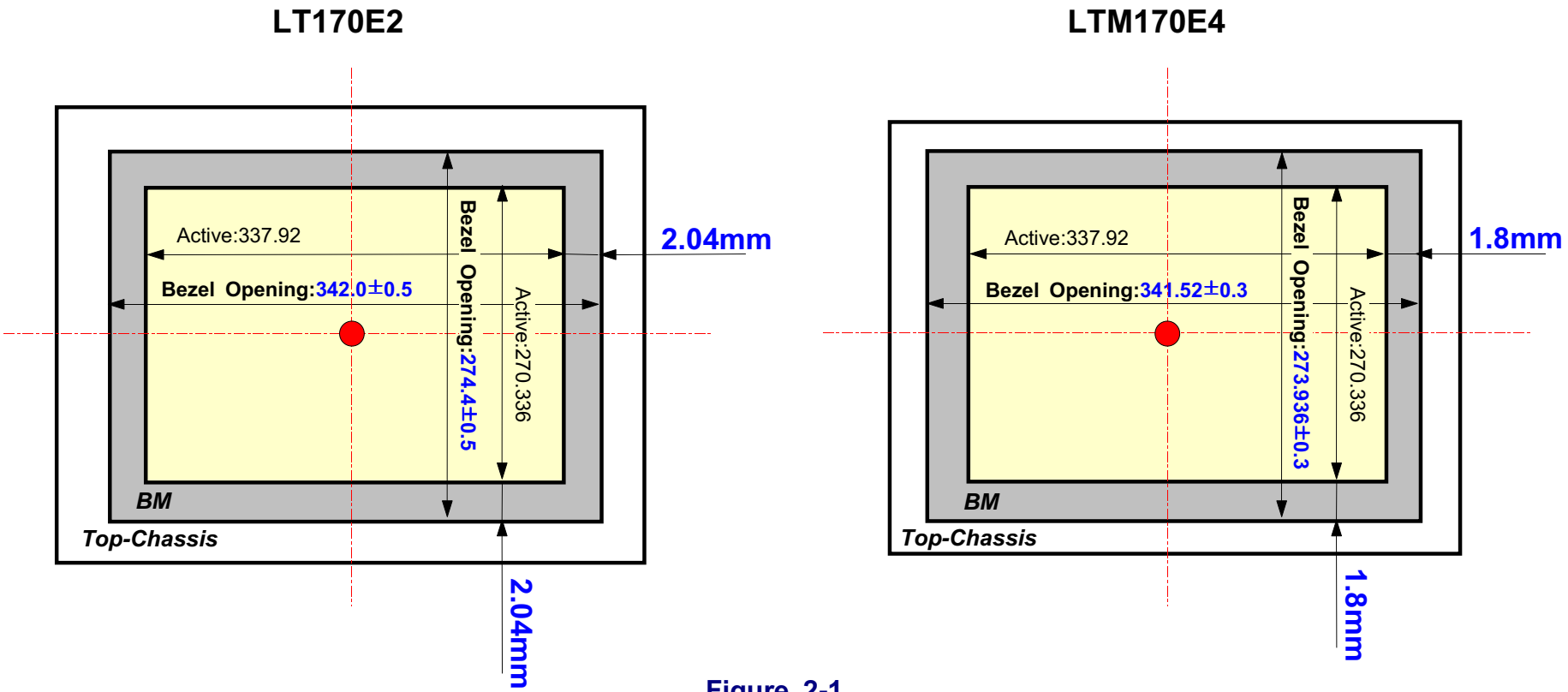



**Figure 2-1**

- System housing should be designed to avoid the interference.
  - If you want adopt E4 model in your current system designed for E2, you should check the point as shown below.
  - **Reduction may cause interference between system housing-front and top chassis of the panel.**
    ☞ **Refer to the Figure 2-2**

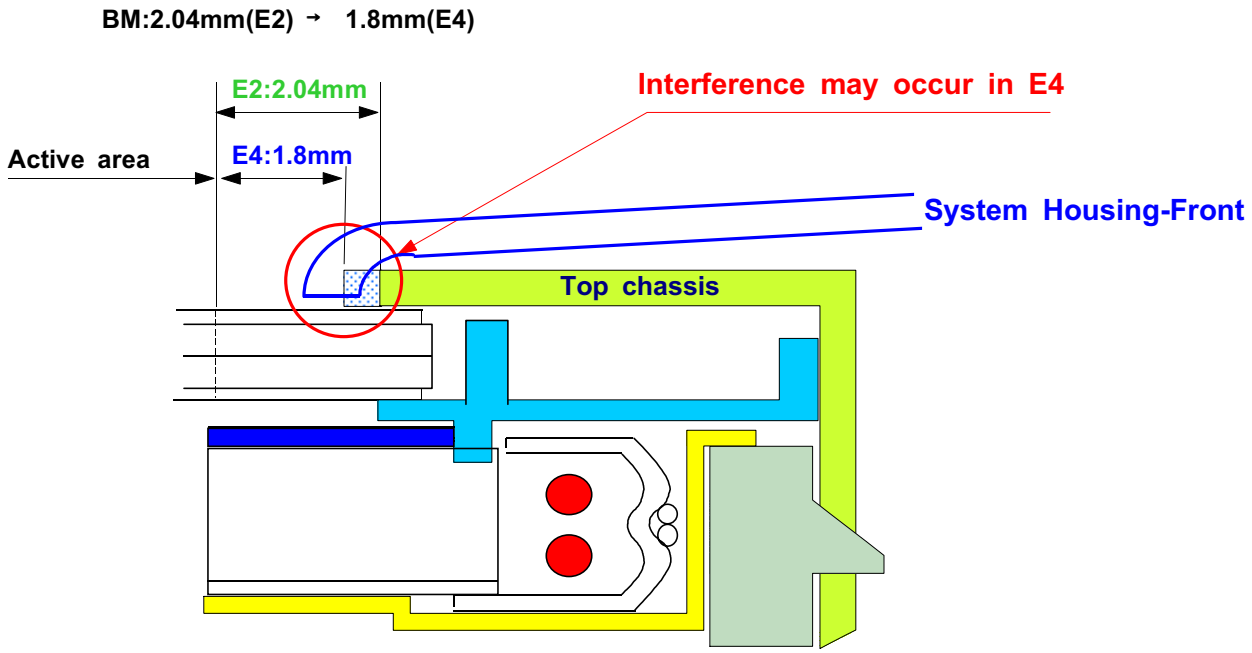



**Figure 2-2**

## 2.2 Location of User Hole

- Because Locations of user holes are not same as E2, mounting brackets should be attached to the 170E4 model for compatibility. ☞ **Refer to the Figure 2-3**

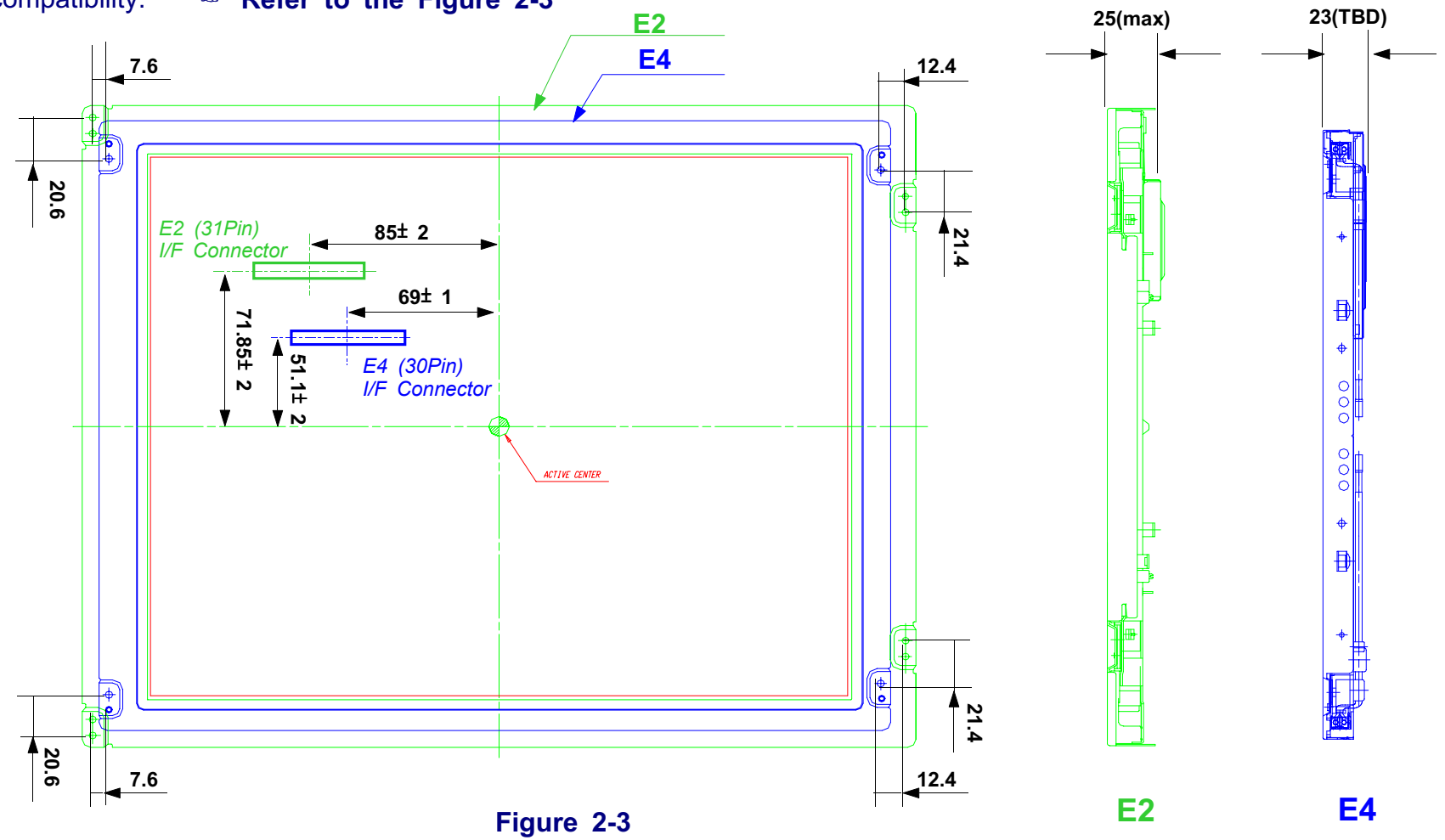
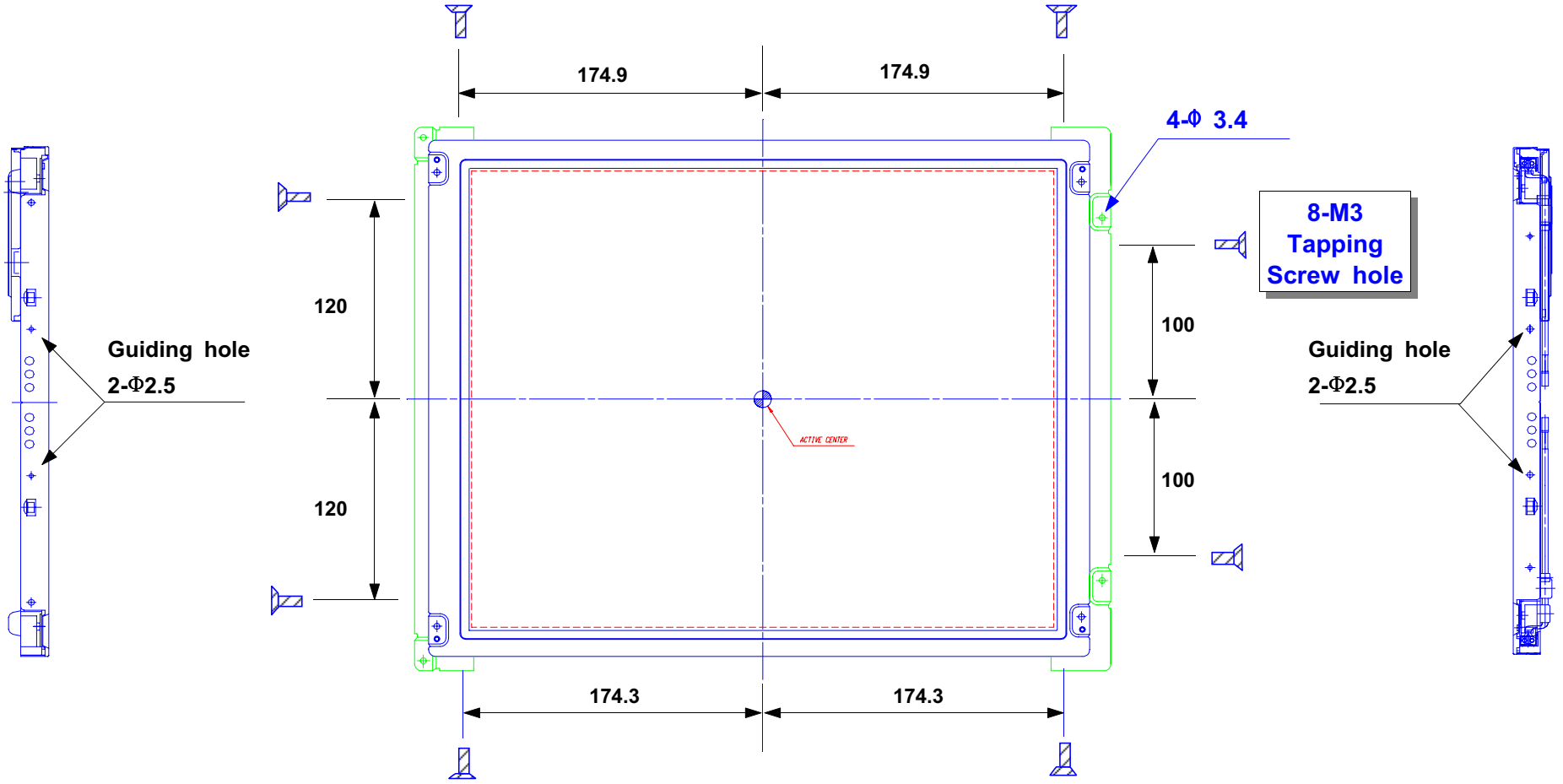



**Figure 2-3**

- You can fix the brackets to the module using screw holes and guiding holes.
  ☞**Refer to the Figure 2-4**




*** For more detail informations, Please Refer to the Outline Dimensions**

## 2.3 Mounting height

- The height from panel surface to the top surface of the chassis is more high than E2.
- But the height from bottom of the mounting tab to Panel surface is same.
- So you can easily design without height adjustment

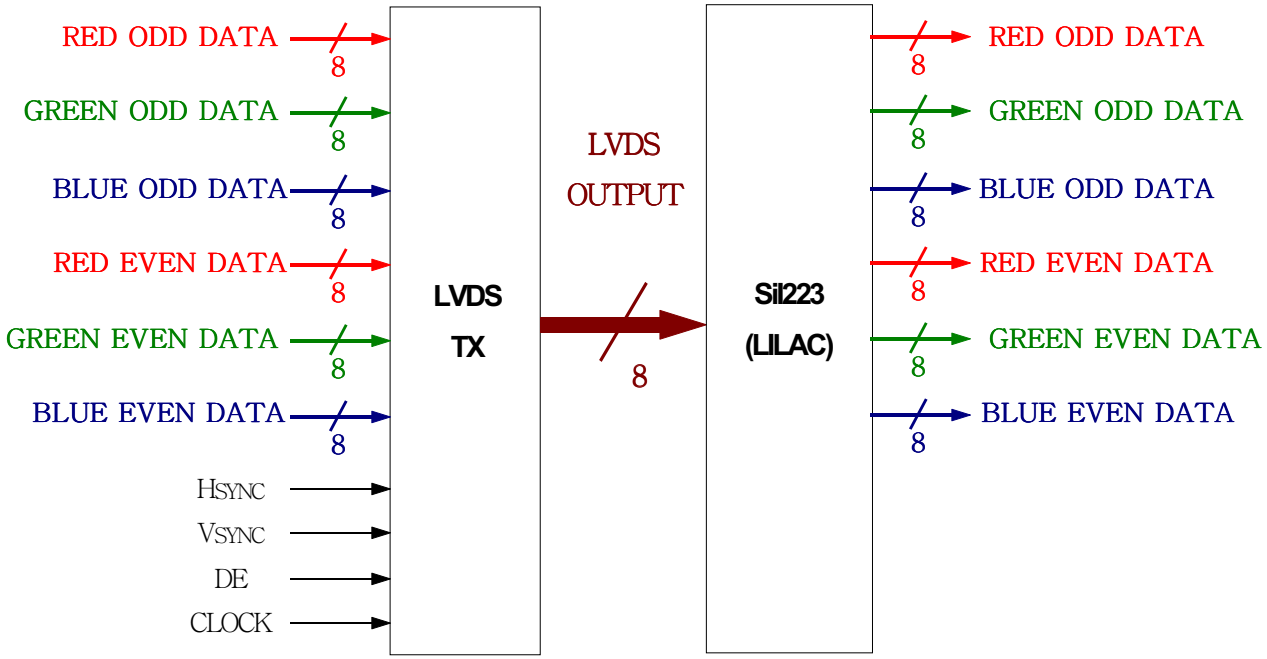
☞ **Height of mounting bracket's holes should be same as panel's**.

## 2.4 Location of Interface connector

- The connector of the E4 is located somewhat to the right lower side than E2. ☞ **Refer to the Figure 2-3**

# 3. Interface

## 3.1 LVDS I/F Block Diagram




Note : There is difference between N/S spec & Sil223 spec(Silicon Image).
In N/S and Samsung TFT-LCD spec, Odd(Even) data is First(Second) pixel data.
But in Sil223 spec, Odd(Even) data is represented as Second(First) pixel data.
So you should be careful to interpret all data.

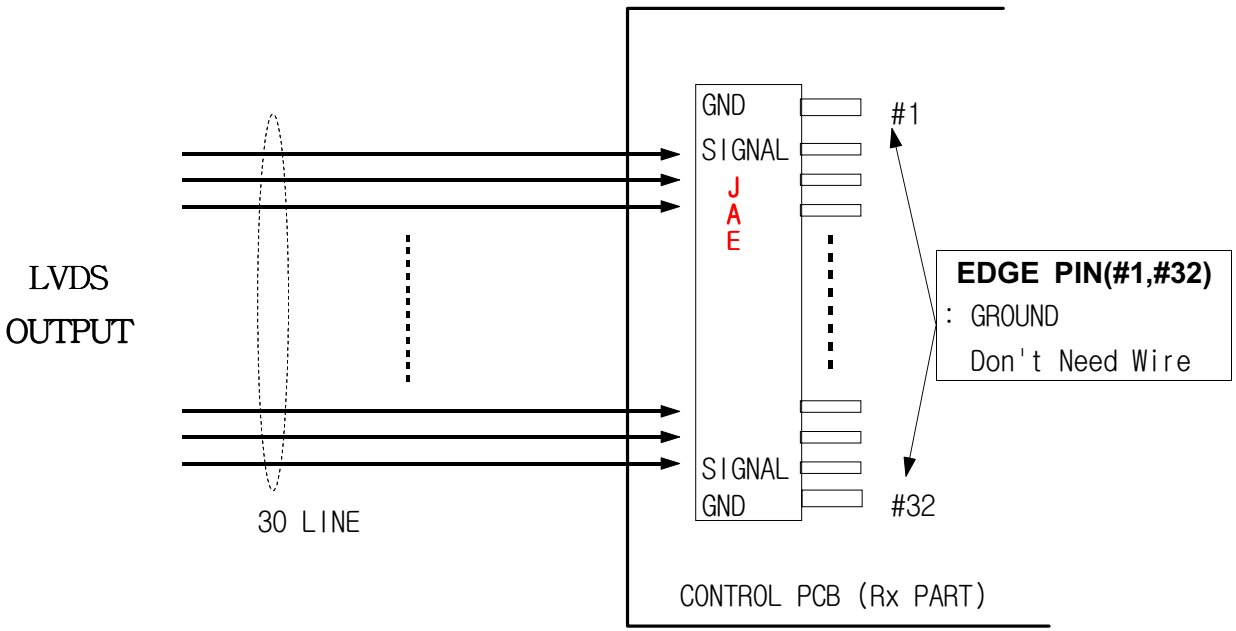
## 3.2 Input Terminal Pin Assignment

- Input Signal & Power ( Connector : JAE FI-X30S-HF )
  ( Matching Socket : JAE FI-X30H )

O = " First Pixel Data "
E = " Second Pixel Data "

| Pin # | Symbol | Function | Polarity | Output Pin # (Transmitter) |
|---|---|---|---|---|
| *1* | *GND* | *Power Ground* | - | Refer to Table |
| 2 | RxO0- | First Pixel Data | Negative | |
| 3 | RxO0+ | | Positive | |
| 4 | RxO1- | | Negative | |
| 5 | RxO1+ | | Positive | |
| 6 | RxO2- | | Negative | |
| 7 | RxO2+ | | Positive | |
| 8 | GND | Power Ground | - | |
| 9 | RxOC- | Low voltage swing differential input odd clock | Negative | |
| 10 | RxOC+ | | Positive | |
| 11 | RxO3- | First Pixel Data | Negative | |
| 12 | RxO3+ | | Positive | |
| 13 | RxE0- | Second Pixel Data | Negative | |
| 14 | RxE0+ | | Positive | |
| 15 | GND | Power Ground | - | |
| 16 | RxE1- | Second Pixel Data | Negative | |
| 17 | RxE1+ | | Positive | |
| 18 | GND | Power Ground | - | |
| 19 | RxE2- | Second Pixel Data | Negative | |
| 20 | RxE2+ | | Positive | |

| Pin # | Symbol | Function | Polarity | Output Pin # (Transmitter) |
|---|---|---|---|---|
| 21 | RxEC- | Low voltage swing differential input even clock | Negative | Refer to Table |
| 22 | RxEC+ | | Positive | |
| 23 | RxE3- | Second Pixel Data | Negative | |
| 24 | RxE3+ | | Positive | |
| 25 | GND | Power Ground | - | |
| 26 | NC | - | - | |
| 27 | DE | Signal | - | |
| 28 | NC | - | - | |
| 29 | POWER (5V) | Power | - | |
| 30 | POWER (5V) | Power | - | |
| 31 | POWER (5V) | Power | - | |
| *32* | *GND* | *Power Ground* | - | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |



## 3.3 JAE FI-X30S-HF (30 PIN) PIN MAP

O = " First Pixel Data " / E = " Second Pixel Data "

| VGA-TFT Data | | DS90C383 | DS90C385 | DS90C387 |
|---|---|---|---|---|
| LSB/MSB | Color Bit | PIN NAME (PIN#) | PIN NAME (PIN#) | PIN NAME(PIN#) |
| LSB | R00 / RE0 | 1st TXIN0 (51) / 2nd TXIN0 (51) | | R10 (10) / R20 (84) |
| | R01 / RE1 | 1st TXIN1 (52) / 2nd TXIN1 (52) | | R11 (9) / R21 (81) |
| | R02 / RE2 | 1st TXIN2 (54) / 2nd TXIN2 (54) | | R12 (8) / R22 (80) |
| | R03 / RE3 | 1st TXIN3 (55) / 2nd TXIN3 (55) | | R13 (7) / R23 (79) |
| | R04 / RE4 | 1st TXIN4 (56) / 2nd TXIN4 (56) | | R14 (6) / R24 (78) |
| | R05 / RE5 | 1st TXIN6 (3) / 2nd TXIN6 (3) | | R15 (5) / R25 (77) |
| | R06 / RE6 | 1st TXIN27 (50) / 2nd TXIN27 (50) | | R16 (4) / R26 (76) |
| MSB | R07 / RE7 | 1st TXIN5 (2) / 2nd TXIN5 (2) | | R17 (3) / R27 (75) |
| LSB | G00 / GE0 | 1st TXIN7 (4) / 2nd TXIN7 (4) | | G10 (2) / G20 (74) |
| | G01 / GE1 | 1st TXIN8 (6) / 2nd TXIN8 (6) | | G11 (1) / G21 (73) |
| | G02 / GE2 | 1st TXIN9 (7) / 2nd TXIN9 (7) | | G12 (100) / G22 (72) |
| | G03 / GE3 | 1st TXIN12 (11) / 2nd TXIN12 (11) | | G13 (99) / G23 (71) |
| | G04 / GE4 | 1st TXIN13 (12) / 2nd TXIN13 (12) | | G14 (96) / G24 (70) |
| | G05 / GE5 | 1st TXIN14 (14) / 2nd TXIN14 (14) | | G15 (95) / G25 (69) |
| | G06 / GE6 | 1st TXIN10 (8) / 2nd TXIN10 (8) | | G16 (94) / G26 (66) |
| MSB | G07 / GE7 | 1st TXIN11 (10) / 2nd TXIN11 (10) | | G17 (93) / G27 (65) |
| LSB | B00 / BE0 | 1st TXIN15 (15) / 2nd TXIN15 (15) | | B10 (92) / B20 (64) |
| | B01 / BE1 | 1st TXIN18 (19) / 2nd TXIN18 (19) | | B11 (91) / B21 (63) |
| | B02 / BE2 | 1st TXIN19 (20) / 2nd TXIN19 (20) | | B12 (90) / B22 (62) |
| | B03 / BE3 | 1st TXIN20 (22) / 2nd TXIN20 (22) | | B13 (89) / B23 (61) |
| | B04 / BE4 | 1st TXIN21 (23) / 2nd TXIN21 (23) | | B14 (88) / B24 (60) |
| | B05 / BE5 | 1st TXIN22 (24) / 2nd TXIN22 (24) | | B15 (87) / B25 (59) |
| | B06 / BE6 | 1st TXIN16 (16) / 2nd TXIN16 (16) | | B16 (86) / B26 (58) |
| MSB | B07 / BE7 | 1st TXIN17 (18) / 2nd TXIN17 (18) | | B17 (85) / B27 (57) |

☞ DS90C387 : BAL pin(pin#24) → "LOW" Fix,
DUAL pin(pin# 23) -> "HIGH" Fix.

## 3.4 Interface Timing

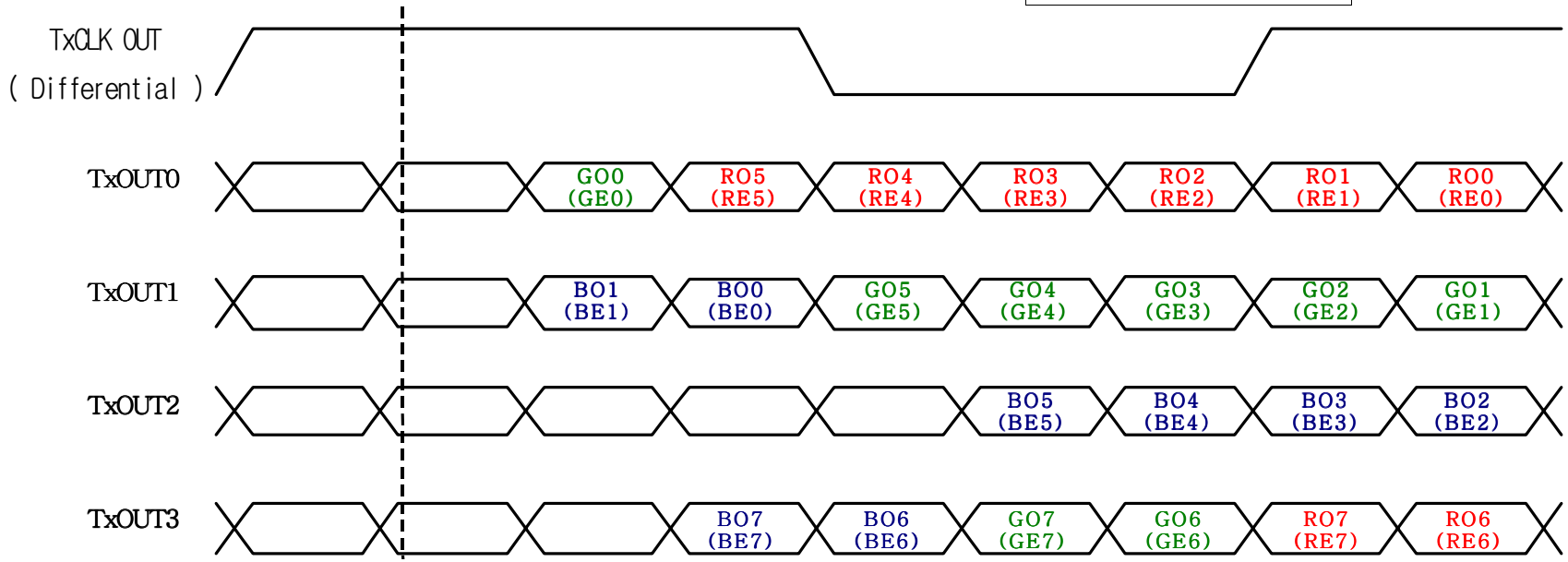
| Signal | Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Clock | Frequency | 1/TC | 40 | - | 54 | MHz | |
| | Hgh Time | TCH | 4 | - | - | nsec | |
| | Low Time | TCL | 4 | - | - | nsec | |
| Data | Setup Time | TDS | 4 | - | - | nsec | |
| | Hold Time | TDH | 4 | - | - | nsec | |
| Data Enable | Setup Time | TES | 4 | - | - | nsec | (1) |
| Frame Frequency | Cycle | TV | - | 16.7 | 16.7 | msec | |
| | | | 1032 | 1066 | 1066 | lines | |
| Vertical Active Disply Term | Display Period | TVD | 1024 | 1024 | 1024 | lines | |
| | Verticle Blank Period | TVB | 8 | - | - | lines | |
| One Line Scanning Time | Cycle | TH | 672 | - | 844 | clocks | |
| Horizontal Active Display Term | Display Period | THD | 640 | 640 | 640 | clocks | |

Note (1) When LTM170E4-L01 model is operated by DE only mode, Hsync and Vsync input signals should be fixed to low for stable operation. Otherwise, the module could operate abnormally.

## 3.5 LVDS OUTPUT TIMING

### 1) DS90C383, DS90C385 LVDS OUTPUT TIMING IN TRANSMISSION

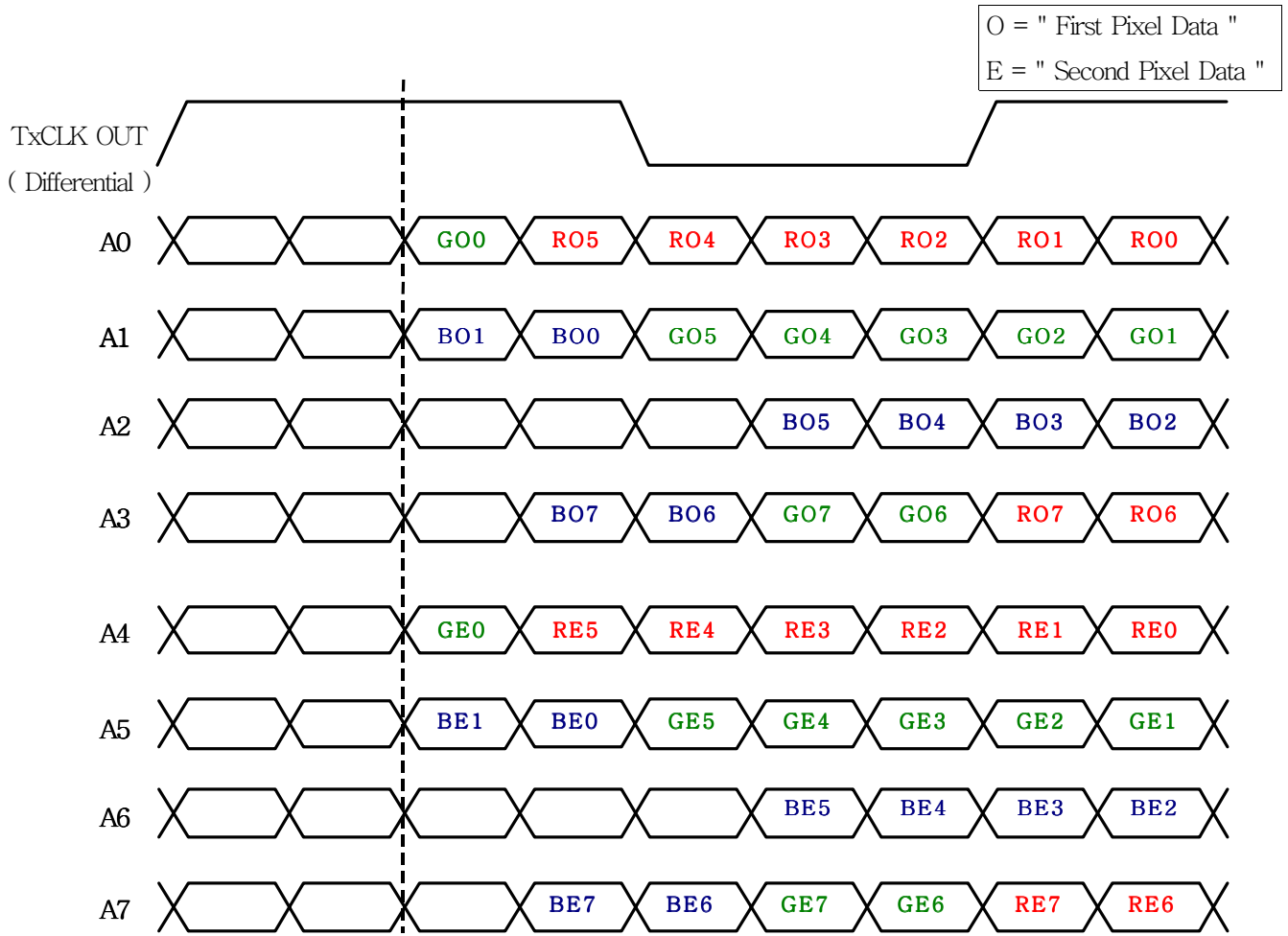
O = " First Pixel Data "
E = " Second Pixel Data "




☞ GO0 : LSB Green data of 1st LVDS Tx Output
GE0 : LSB Green data of 2nd LVDS Tx Output

## 3.5 LVDS OUTPUT TIMING

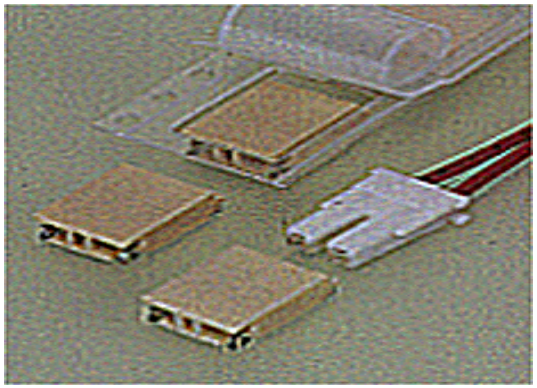
### 2) DS90C387 LVDS OUTPUT TIMING IN TRANSMISSION (BAL= LOW)

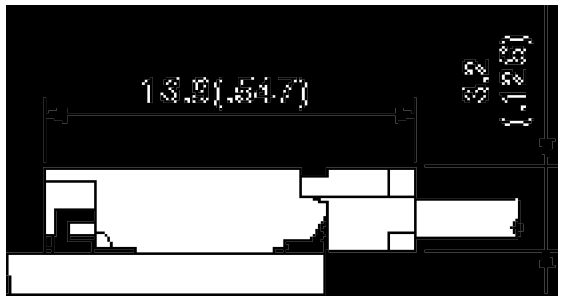


# 4. Back-Light

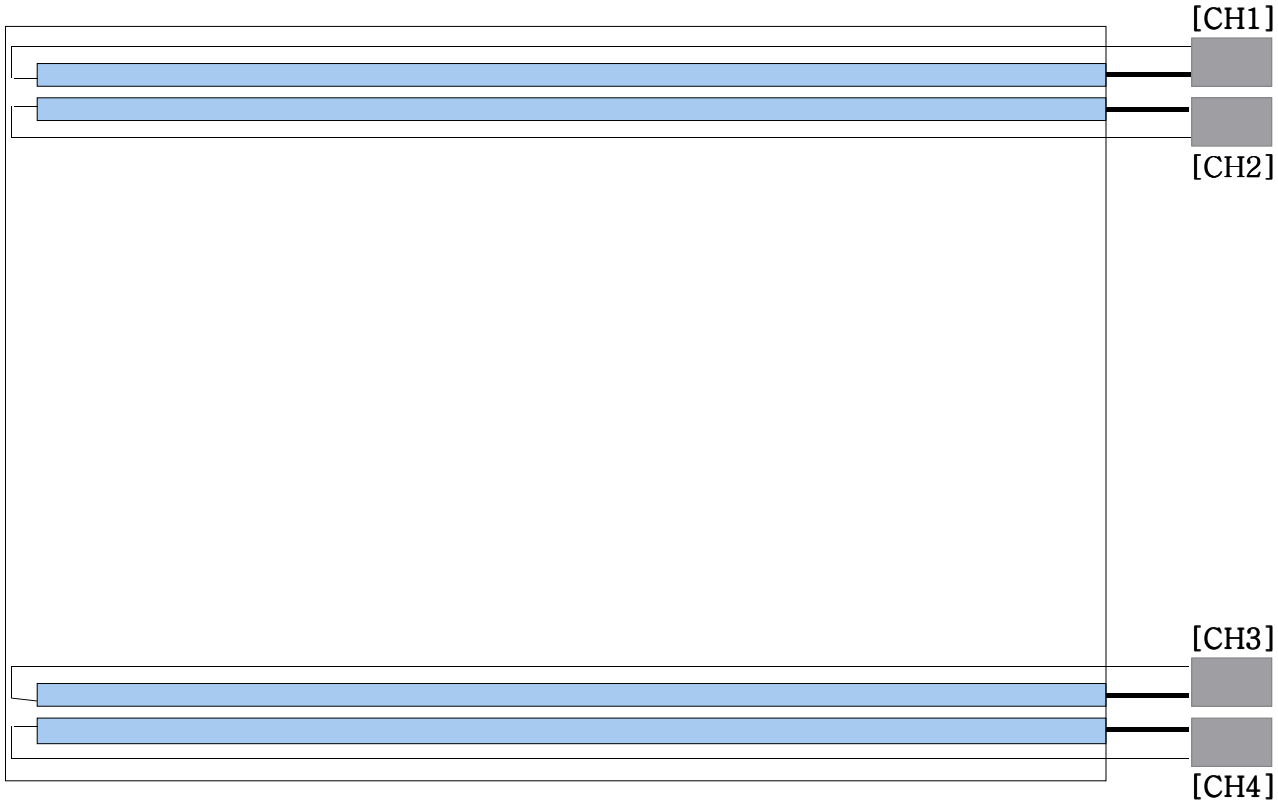
## 4.1 Back-Light Unit Connector

| Pin No. | Input [Ch1][Ch2], [Ch3][Ch4] | Color | Function |
|---|---|---|---|
| 1 | Hot | PINK | High Voltage |
| 2 | Cold | WHITE | Ground |
| 3 | Hot | BLUE | High Voltage |
| 4 | Cold | BLACK | Ground |
| Connector Part No. | JST BHSR - 02VS - 1 | | |
| Matching Connector | SM02B - BHSS -1-TB | | |

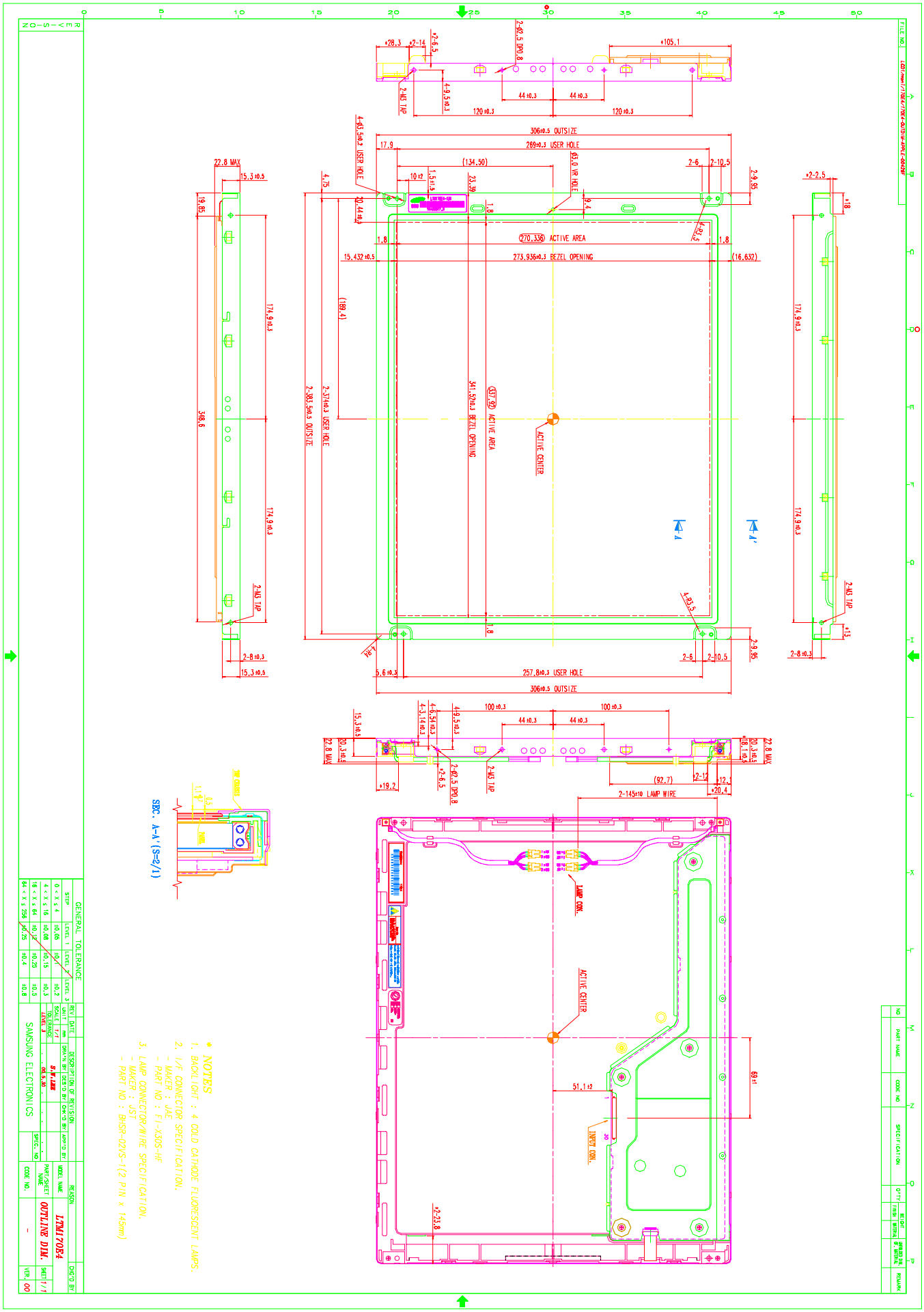




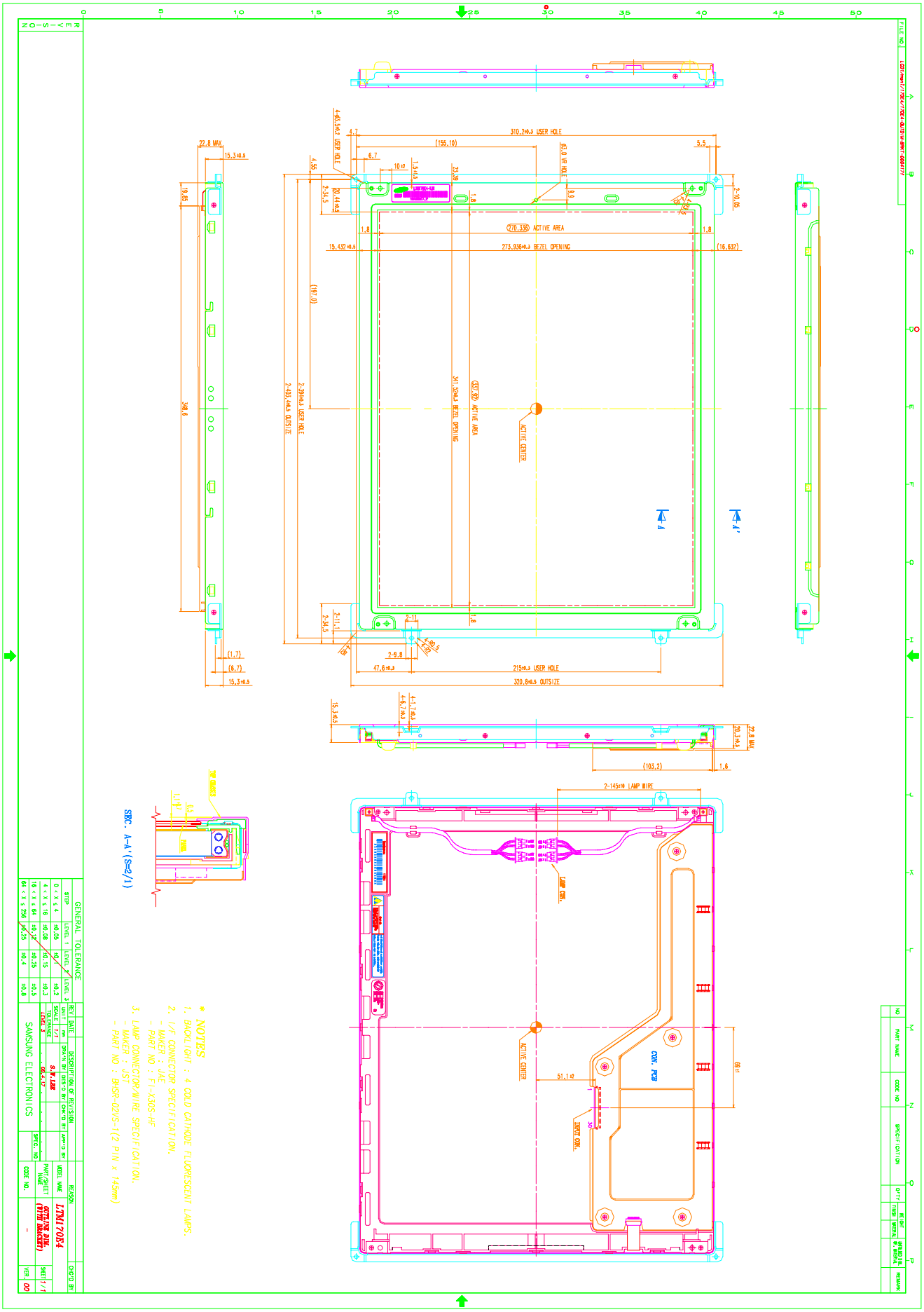
## 4.2 Block Diagram



# Out-dimension of LTM170E4-L01

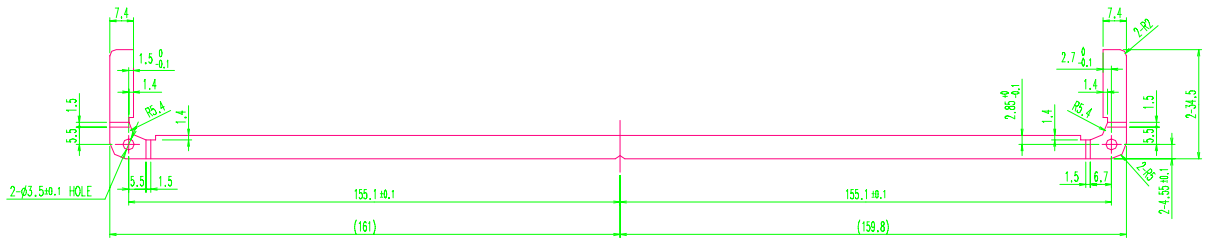


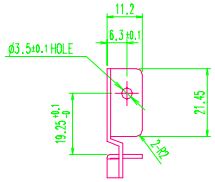
# Bracket information for LTM170E4-L01



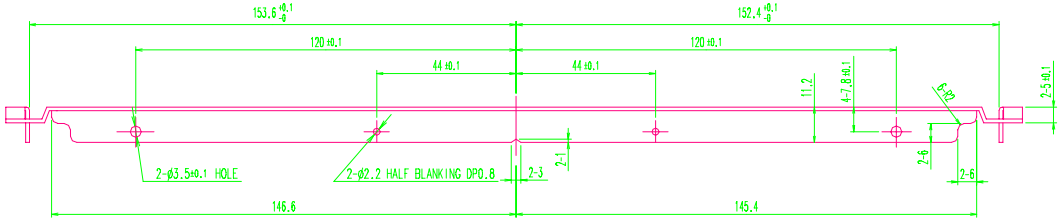
FILE NO. /LCD1/moni/170E4/170E4-BRKT-COMPATIBLE-L-00F

| NO | PART NAME | CODE NO | SPECIFICATION | Q'TY | WEIGHT FINISH | WEIGHT MATERIAL | UNFOLDED DIM. OF. MATERIAL | REMARK |
|---|---|---|---|---|---|---|---|---|
| 1 | BRACKET-COMPATIBLE(L) | LJ61-00375A | SECC,T1.2,LTM170E4 | 1 EA | | | | |




VIEW RIGHT & LEFT




## * NOTES

1. PART TO FREE FROM RUST AND SCRATCH
2. MATERIAL : SECC T1.2
3. BURR HEIGHT : 0.08mm MAX
4. UNLESS SPECIFIED, ALL CONERS AND EDGES ARE R0.3

REVISION

| GENERAL TOLERANCE | | | |
|---|---|---|---|
| STEP | LEVEL 1 | LEVEL 2 | LEVEL 3 |
| 0 < X ≤ 4 | ±0.05 | ±0.1 | ±0.2 |
| 4 < X ≤ 16 | ±0.08 | ±0.15 | ±0.3 |
| 16 < X ≤ 64 | ±0.12 | ±0.25 | ±0.5 |
| 64 < X ≤ 256 | ±0.25 | ±0.4 | ±0.8 |

| REV | DATE | DESCRIPTION OF REVISION | CHG'D BY |
|---|---|---|---|
| | | | |

| UNIT | mm | DRA'N BY | DES'D BY | CHK'D BY | APP'D BY |
|---|---|---|---|---|---|
| SCALE | / | | S.W.LEE | | |
| TOLERANCE LEVEL 2 | | . . | . 2000 04 07 . | | . . |

SAMSUNG ELECTRONICS

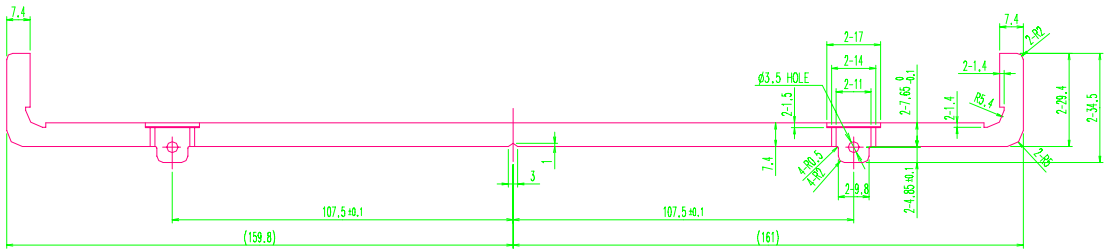
SPEC. NO SD

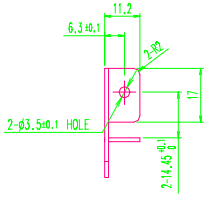
| REASON | CHG'D BY |
|---|---|
| | |

| | | | |
|---|---|---|---|
| MODEL NAME | LTM170E4 | | |
| PART/SHEET NAME | BRACKET-COMPATIBLE(L) | SHEET | 1/1 |
| CODE NO. | LJ61-00375A | VER. | 00 |

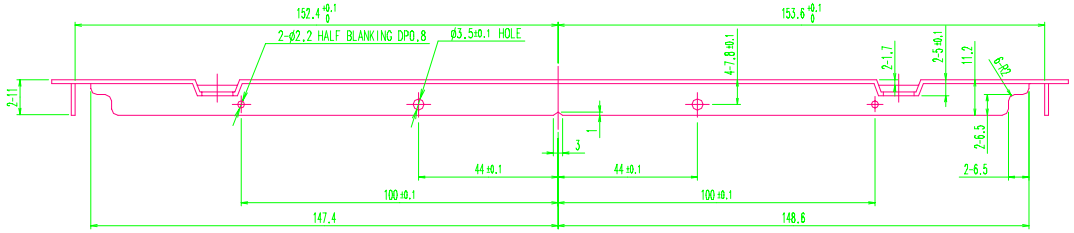
FILE NO. /LCD1/moni/170E4/170E4-BRKT-COMPATIBLE-R-00F

| NO | PART NAME | CODE NO | SPECIFICATION | Q'TY | WEIGHT FINISH | WEIGHT MATERIAL | UNFOLDED DIM. OR. MATERIAL | REMARK |
|---|---|---|---|---|---|---|---|---|
| 1 | BRACKET-COMPATIBLE(R) | LJ61-00376A | SECC,T1.2,LTM170E4 | 1 EA | | | | |




VIEW RIGHT & LEFT

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| 0 < X ≤ 4 | ±0.05 | ±0.1 | ±0.2 |
| 4 < X ≤ 16 | ±0.08 | ±0.15 | ±0.3 |
| 16 < X ≤ 64 | ±0.12 | ±0.25 | ±0.5 |
| 64 < X ≤ 256 | ±0.25 | ±0.4 | ±0.8 |

| REV | DATE | DESCRIPTION OF REVISION | REASON | CHG'D BY |
|---|---|---|---|---|

| UNIT | mm | DRA'N BY | DES'D BY | CHK'D BY | APP'D BY |
|---|---|---|---|---|---|
| SCALE | / | | S.W.LEE | | |
| TOLERANCE LEVEL 2 | | . . | 2000.02.24 | . . | . . |

SAMSUNG ELECTRONICS

SPEC. NO SD

| | | | |
|---|---|---|---|
| MODEL NAME | LTM170E4 | | |
| PART/SHEET NAME | BRACKET-COMPATIBLE(R) | SHEET | 1/1 |
| CODE NO. | LJ61-00376A | VER. | 00 |

# ◆ Out-dimension of LT170E2-131