LTM2882

Dual Isolated RS232 μModule Transceiver + Power

FEATURES

- **RS232 Transceiver: 2500V_{RMS} for 1 Minute**
- **UL-CSA Recognized cULus File #E151738**
- **CSA Component Acceptance Notice 5A**
- **Isolated DC Power: 5V at Up to 200mA**
- **No External Components Required**
- **1.62V to 5.5V Logic Supply for Flexible Digital Interfacing**
- **High Speed Operation**
  - **1Mbps for 250pF/3kΩ Load**
  - **250kbps for 1nF/3kΩ Load**
  - **100kbps for 2.5nF/3kΩ TIA/EIA-232-F Load**
- 3.3V (LTM2882-3) or 5V (LTM2882-5) Operation
- No Damage or Latchup to ±10kV HBM ESD on Isolated RS232 Interface or Across Isolation Barrier
- High Common Mode Transient Immunity: 30kV/μs
- Maximum Continuous Working Voltage: 560V_{PEAK}
- True RS232 Compliant Output Levels
- 15mm × 11.25mm BGA and LGA Packages

APPLICATIONS

- Isolated RS232 Interface
- Industrial Communication
- Test and Measurement Equipment
- Breaking RS232 Ground Loops

DESCRIPTION

The LTM®2882 is a complete galvanically isolated dual RS232 μModule® (micromodule) transceiver. No external components are required. A single 3.3V or 5V supply powers both sides of the interface through an integrated, isolated DC/DC converter. A logic supply pin allows easy interfacing with different logic levels from 1.62V to 5.5V, independent of the main supply.

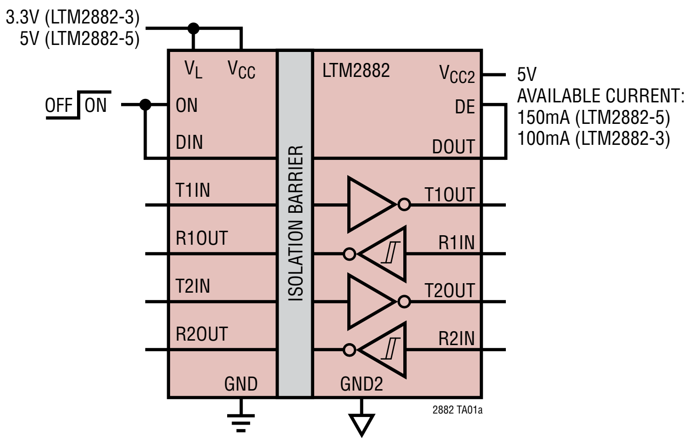
Coupled inductors and an isolation power transformer provide 2500V_{RMS} of isolation between the line transceiver and the logic interface. This device is ideal for systems with different grounds, allowing for large common mode voltages. Uninterrupted communication is guaranteed for common mode transients greater than 30kV/μs.

This part is compatible with the TIA/EIA-232-F standard. Driver outputs are protected from overload and can be shorted to ground or up to ±15V without damage. An auxiliary isolated digital channel is available. This channel allows configuration for half-duplex operation by controlling the DE pin.

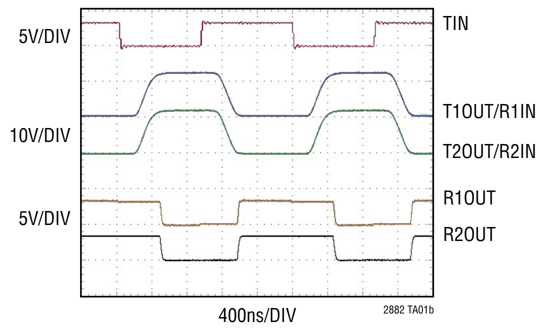
Enhanced ESD protection allows this part to withstand up to ±10kV (human body model) on the transceiver interface pins to isolated supplies and across the isolation barrier to logic supplies without latchup or damage.

TYPICAL APPLICATION

Isolated Dual RS232 μModule Transceiver



1Mbps Operation



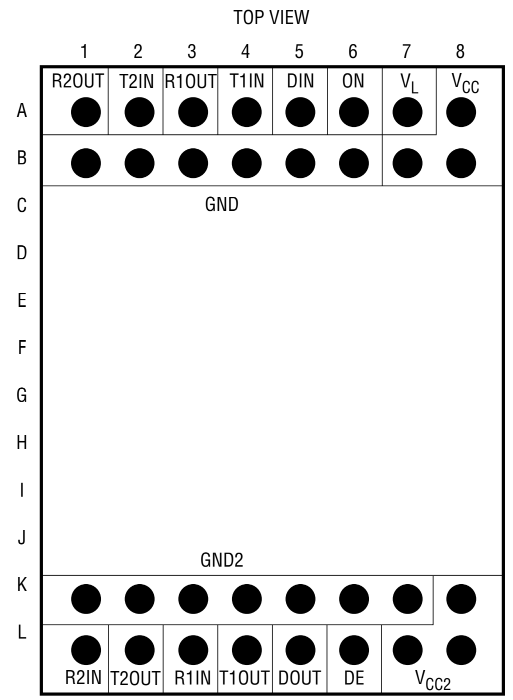
DRIVER OUTPUTS TIED TO RECEIVER INPUTS
TOUT LOAD = 250pF + RIN
ROUT LOAD = 150pF

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND .... –0.3V to 6V
V_L to GND .... –0.3V to 6V
V_{CC2} to GND2... –0.3V to 6V
Logic Inputs
  T1IN, T2IN, ON, DIN to GND........–0.3V to (V_L + 0.3V)
  DE to GND2............................–0.3V to (V_{CC2} + 0.3V)
Logic Outputs
  R1OUT, R2OUT to GND...............–0.3V to (V_L + 0.3V)
  DOUT to GND2........................–0.3V to (V_{CC2} + 0.3V)
Driver Output Voltage
  T1OUT, T2OUT to GND2..........................–15V to 15V
Receiver Input Voltage
  R1IN, R2IN to GND2 .... –25V to 25V
Operating Temperature Range (Note 4)
  LTM2882C ....0°C ≤ T_A ≤ 70°C
  LTM2882I .... –40°C ≤ T_A ≤ 85°C
Maximum Internal Operating Temperature............ 105°C
Storage Temperature Range .... –40°C to 105°C
Peak Package Body Reflow Temperature .... 245°C

PIN CONFIGURATION



BGA PACKAGE
32-PIN (15mm × 11.25mm × 3.42mm)
T_{JMAX} = 105°C,
θ_{JA} = 30°C/W, θ_{JCtop} = 27.8°C/W,
$\theta_{JCbottom}$ = 19.3°C/W, θ_{JB} = 24°C/W,
WEIGHT = 1.1g

LGA PACKAGE
32-PIN (15mm × 11.25mm × 2.8mm)
T_{JMAX} = 105°C,
θ_{JA} = 29°C/W, θ_{JCtop} = 27.9°C/W,
$\theta_{JCbottom}$ = 18°C/W, θ_{JB} = 22.7°C/W,
WEIGHT = 1.1g

ORDER INFORMATION http://www.linear.com/product/LTM2882#orderinfo

PART NUMBER	INPUT VOLTAGE	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
			DEVICE	FINISH CODE			
LTM2882CY-3#PBF	3V to 3.6V	SAC305 (RoHS)	LTM2882Y-3	e1	BGA	3	0°C to 70°C
LTM2882IY-3#PBF							–40°C to 85°C
LTM2882HY-3#PBF **(OBSOLETE)**							–40°C to 105°C
LTM2882MPY-3#PBF **(OBSOLETE)**							–55°C to 105°C
LTM2882CY-5#PBF	4.5V to 5.5V		LTM2882Y-5				0°C to 70°C
LTM2882IY-5#PBF							–40°C to 85°C
LTM2882HY-5#PBF **(OBSOLETE)**							–40°C to 105°C
LTM2882MPY-5#PBF **(OBSOLETE)**							–55°C to 105°C
LTM2882CV-3#PBF	3V to 3.6V	Au (RoHS)	LTM2882V-3	e4	LGA		0°C to 70°C
LTM2882IV-3#PBF							–40°C to 85°C
LTM2882CV-5#PBF	4.5V to 5.5V		LTM2882V-5				0°C to 70°C
LTM2882IV-5#PBF							–40°C to 85°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: www.linear.com/leadfree
- This product is not recommended for second side reflow. For more information, go to: www.linear.com/BGA-assy
- Recommended BGA and LGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging
- This product is moisture sensitive. For more information, go to: www.linear.com/umodule/pcbassembly

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2882-3 V_{CC} = 3.3V, LTM2882-5 V_{CC} = 5.0V, V_L = V_{CC}, and GND = GND2 = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{CC}	Input Supply Range	LTM2882-3	●	3.0	3.3	3.6	V
		LTM2882-5	●	4.5	5.0	5.5	V
V_L	Logic Supply Range		●	1.62		5.5	V
I_{CC}	Input Supply Current	ON = 0V	●		0	10	µA
		LTM2882-3, No Load	●		24	30	mA
		LTM2882-5, No Load	●		17	25	mA
V_{CC2}	Regulated Output Voltage, Loaded	LTM2882-3 DE = 0V, I_{LOAD} = 100mA	●	4.7	5.0		V
		LTM2882-5 DE = 0V, I_{LOAD} = 150mA	●	4.7	5.0		V
$V_{CC2(NOLOAD)}$	Regulated Output Voltage, No Load	DE = 0, No Load		4.8	5.0	5.35	V
	Efficiency	I_{CC2} = 100mA, LTM2882-5 (Note 2)			65		%
I_{CC2}	Output Supply Short-Circuit Current				200		mA
Driver							
V_{OLD}	Driver Output Voltage Low	R_L = 3kΩ	●	–5	–5.7		V
V_{OHD}	Driver Output Voltage High	R_L = 3kΩ	●	5	6.2		V
I_{OSD}	Driver Short-Circuit Current	V_{T1OUT}, V_{T2OUT} = 0V, V_{CC2} = 5.5V	●		±35	±70	mA
I_{OZD}	Driver Three-State (High Impedance) Output Current	DE = 0V, V_{T1OUT}, V_{T2OUT} = ±15V	●		±0.1	±10	µA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver							
V_{IR}	Receiver Input Threshold	Input Low	●	0.8	1.3		V
		Input High	●		1.7	2.5	V
V_{HYSR}	Receiver Input Hysteresis		●	0.1	0.4	1.0	V
R_{IN}	Receiver Input Resistance	$-15V \le (V_{R1IN}, V_{R2IN}) \le 15V$	●	3	5	7	kΩ
Logic							
V_{ITH}	Logic Input Threshold Voltage	ON, T1IN, T2IN, DIN = $1.62V \le V_L < 2.35V$	●	$0.25 \bullet V_L$		$0.75 \bullet V_L$	V
		ON, T1IN, T2IN, DIN = $2.35V \le V_L \le 5.5V$	●	0.4		$0.67 \bullet V_L$	V
		DE	●	0.4		$0.67 \bullet V_{CC2}$	V
I_{INL}	Logic Input Current		●			±1	µA
V_{HYS}	Logic Input Hysteresis	T1IN, T2IN, DIN (Note 2)			150		mV
V_{OH}	Logic Output High Voltage	R1OUT, R2OUT					
		I_{LOAD} = –1mA (Sourcing), $1.62V \le V_L < 3.0V$	●	$V_L - 0.4$			V
		I_{LOAD} = –4mA (Sourcing), $3.0V \le V_L \le 5.5V$	●	$V_L - 0.4$			V
		DOUT, I_{LOAD} = –4mA (Sourcing)	●	$V_{CC2} - 0.4$			V
V_{OL}	Logic Output Low Voltage	R1OUT, R2OUT					
		I_{LOAD} = 1mA (Sinking), $1.62V \le V_L < 3.0V$	●			0.4	V
		I_{LOAD} = 4mA (Sinking), $3.0V \le V_L \le 5.5V$	●			0.4	V
		DOUT, I_{LOAD} = 4mA (Sinking)	●			0.4	V
ESD (HBM) (Note 2)							
	RS232 Driver and Receiver Protection	(T1OUT, T2OUT, R1IN, R2IN) to (V_{CC2}, GND2)			±10		kV
		(T1OUT, T2OUT, R1IN, R2IN) to (V_{CC}, V_L, GND)			±10		kV
	Isolation Boundary	(V_{CC2}, GND2) to (V_{CC}, V_L, GND)			±10		kV

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2882-3 V_{CC} = 3.3V, LTM2882-5 V_{CC} = 5.0V, V_L = V_{CC}, and GND = GND2 = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Maximum Data Rate (T1IN to T1OUT, T2IN to T2OUT)	R_L = 3kΩ, C_L = 2.5nF (Note 3)	●	100			kbps
		R_L = 3kΩ, C_L = 1nF (Note 3)	●	250			kbps
		R_L = 3kΩ, C_L = 250pF (Note 3)	●	1000			kbps
	Maximum Data Rate (DIN to DOUT)	C_L = 15pF (Note 3)	●	10			Mbps
Driver							
	Driver Slew Rate ($6V/t_{THL}$ or t_{TLH})	R_L = 3kΩ, C_L = 50pF (Figure 1)	●			150	V/µs
t_{PHLD}, t_{PLHD}	Driver Propagation Delay	R_L = 3kΩ, C_L = 50pF (Figure 1)	●		0.2	0.5	µs
t_{SKEWD}	Driver Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$	R_L = 3kΩ, C_L = 50pF (Figure 1)			40		ns
t_{PZHD}, t_{PZLD}	Driver Output Enable Time	DE = ↑, R_L = 3kΩ, C_L = 50pF (Figure 2)	●		0.6	2	µs
t_{PHZD}, t_{PLZD}	Driver Output Disable Time	DE = ↓, R_L = 3kΩ, C_L = 50pF (Figure 2)	●		0.3	2	µs

SWITCHING CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver							
t_{PHLR}, t_{PLHR}	Receiver Propagation Delay	C_L = 150pF (Figure 3)	●		0.2	0.4	μs
t_{SKEWR}	Receiver Skew $\lvert t_{PHLR} - t_{PLHR} \rvert$	C_L = 150pF (Figure 3)			40		ns
t_{RR}, t_{FR}	Receiver Rise or Fall Time	C_L = 150pF (Figure 3)	●		60	200	ns
Auxiliary Channel							
t_{PHLL}, t_{PLHL}	Propagation Delay	C_L = 15pF, t_R and t_F < 4ns (Figure 4)	●		60	100	ns
t_{RL}, t_{FL}	Rise or Fall Time	C_L = 150pF (Figure 4)	●		60	200	ns
Power Supply							
	Power-Up Time	ON = ↑ to $V_{CC2(MIN)}$	●		0.2	2	ms

ISOLATION CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{ISO}	Rated Dielectric Insulation Voltage	1 Minute, Derived from 1 Second Test		2500			V_{RMS}
		1 Second (Notes 5, 6)		±4400			V
	Common Mode Transient Immunity	V_L = ON = 3.3V, V_{CM} = 1kV, Δt = 33ns (Note 2)		30			kV/μs
V_{IORM}	Maximum Working Insulation Voltage	(Notes 2, 5)		560			V_{PEAK}
				400			V_{RMS}
	Partial Discharge	V_{PR} = 1050 V_{PEAK} (Notes 2, 5)				5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 2)		600			V_{RMS}
DTI	Depth of Erosion	IEC 60112 (Note 2)			0.017		mm
	Distance Through Insulation	(Note 2)			0.06		mm
	Input to Output Resistance	(Notes 2, 5)		10^9			Ω
	Input to Output Capacitance	(Notes 2, 5)			6		pF
	Creepage Distance	(Notes 2, 5)			9.48		mm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and not subject to production test.

Note 3: Maximum Data Rate is guaranteed by other measured parameters and is not tested directly.

Note 4: This device includes over-temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 105°C when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

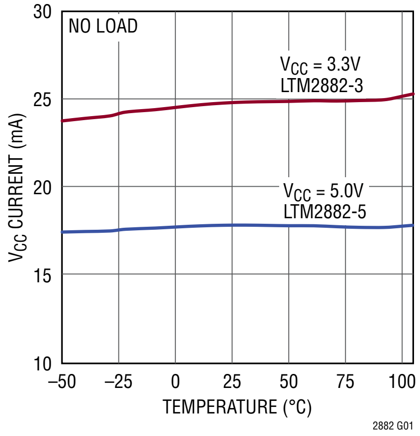
Note 5: Tests performed from GND to GND2, all pins shorted each side of isolation barrier.

Note 6: The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

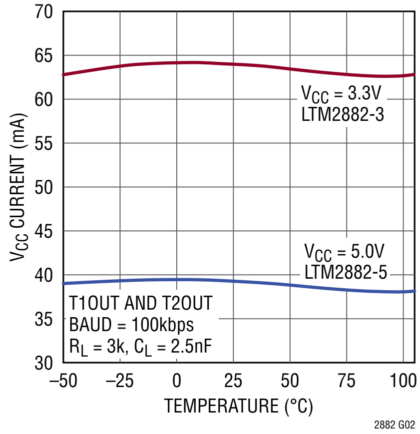
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2882-3 V_{CC} = 3.3V, LTM2882-5 V_{CC} = 5V, V_L = 3.3V, and GND = GND2 = 0V, ON = V_L unless otherwise noted.

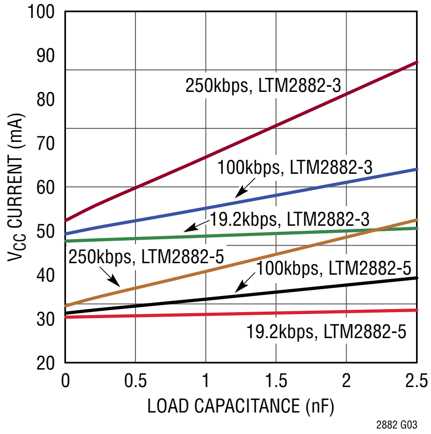
V_{CC} Supply Current vs Temperature



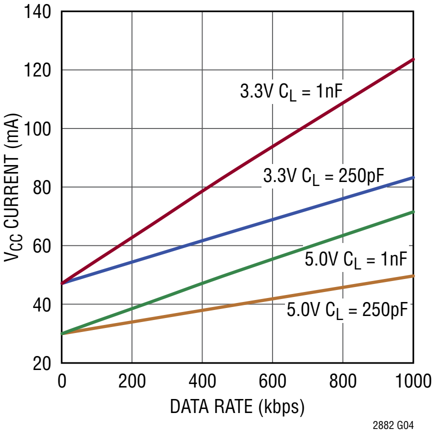
V_{CC} Supply Current vs Temperature



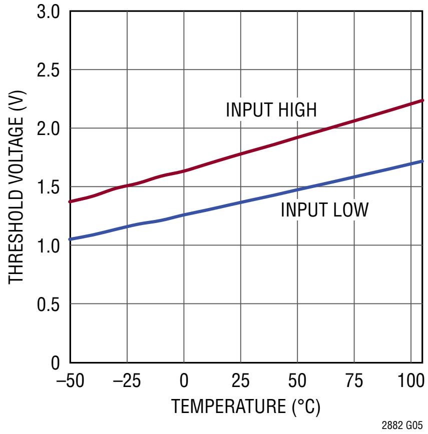
V_{CC} Supply Current vs Load Capacitance (Dual Transceiver)



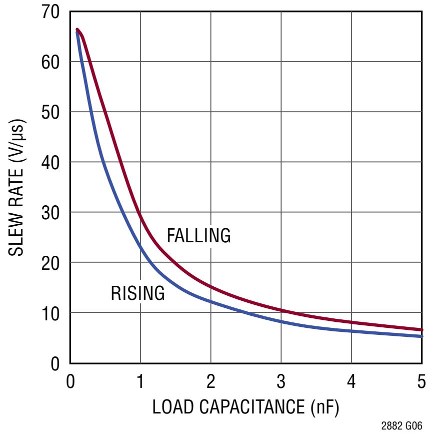
V_{CC} Supply Current vs Data Rate (Dual Transceiver)



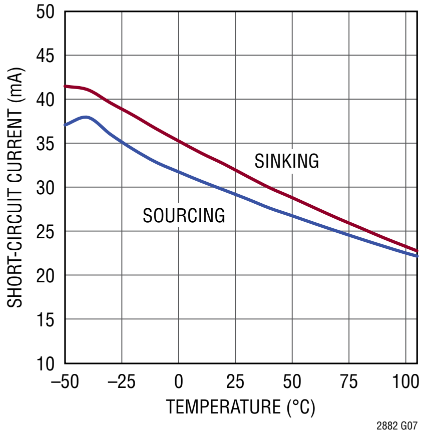
Receiver Input Threshold vs Temperature



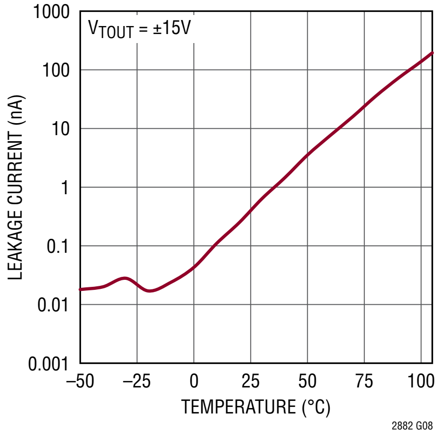
Driver Slew Rate vs Load Capacitance



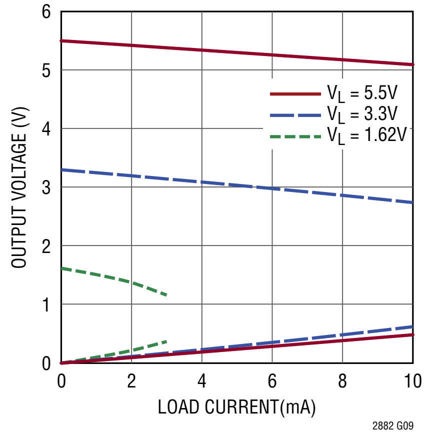
Driver Short-Circuit Current vs Temperature



Driver Disabled Leakage Current vs Temperature at ±15V



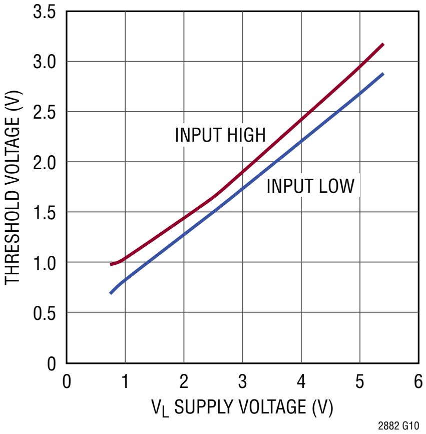
Receiver Output Voltage vs Load Current



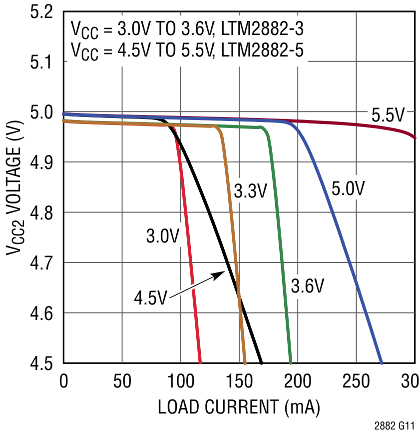
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2882-3 V_{CC} = 3.3V, LTM2882-5 V_{CC} = 5V, V_L = 3.3V, and GND = GND2 = 0V, ON = V_L unless otherwise noted.

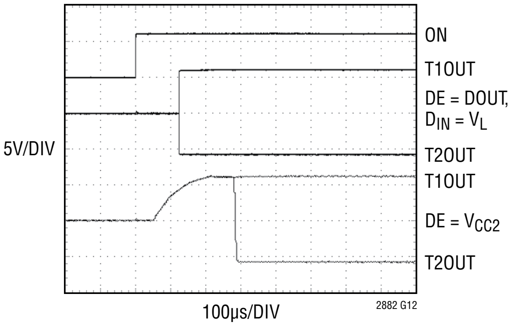
Logic Input Threshold vs V_L Supply Voltage



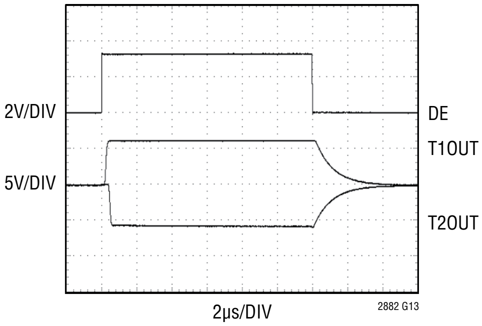
V_{CC2} Output Voltage vs Load Current



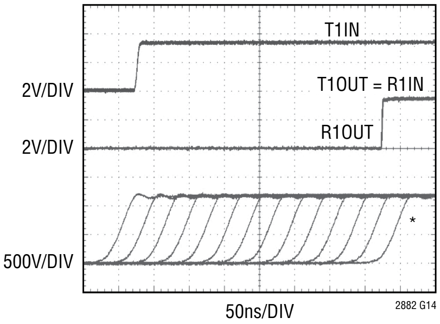
Driver Outputs Exiting Shutdown



Driver Outputs Enable/Disable



Operating Through 35kV/µs Common Mode Transients

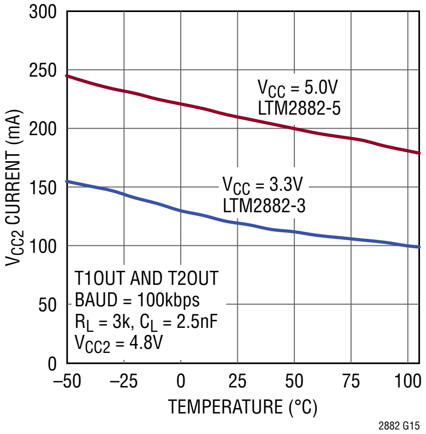


* MULTIPLE SWEEPS OF COMMON MODE TRANSIENTS

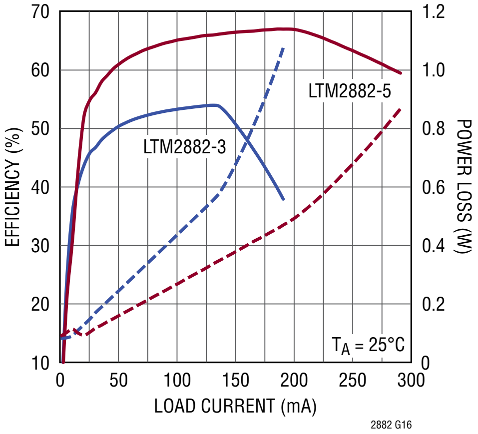
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2882-3 V_{CC} = 3.3V, LTM2882-5 V_{CC} = 5V, V_L = 3.3V, and GND = GND2 = 0V, ON = V_L unless otherwise noted.

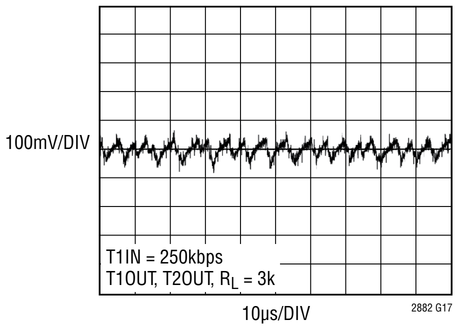
V_{CC2} Surplus Current vs Temperature



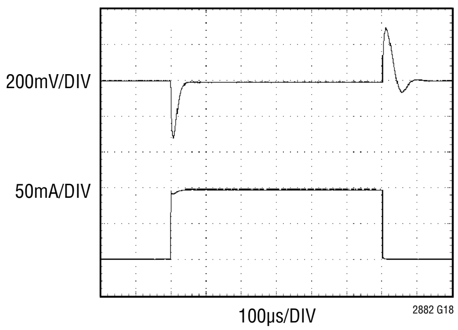
V_{CC2} Power Efficiency



V_{CC2} Ripple and Noise



V_{CC2} Load Step Response



TEST CIRCUITS

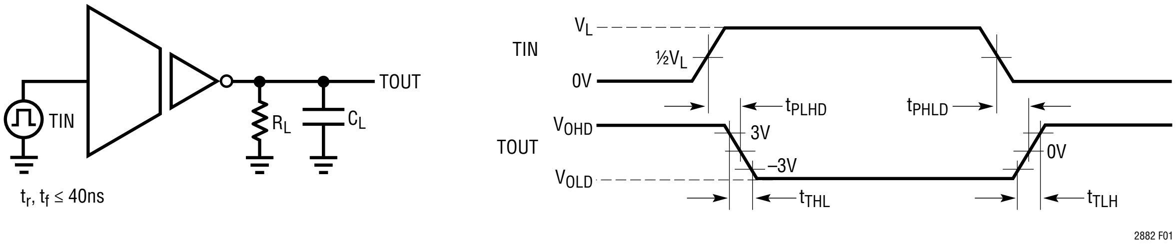


Figure 1. Driver Slew Rate and Timing Measurement

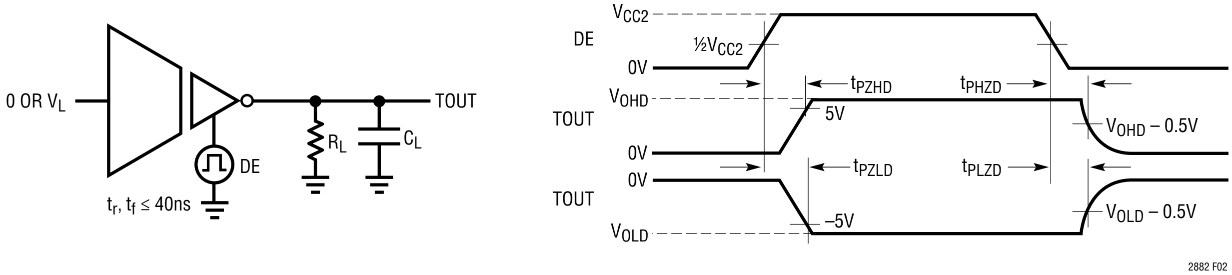


Figure 2. Driver Enable/Disable Times

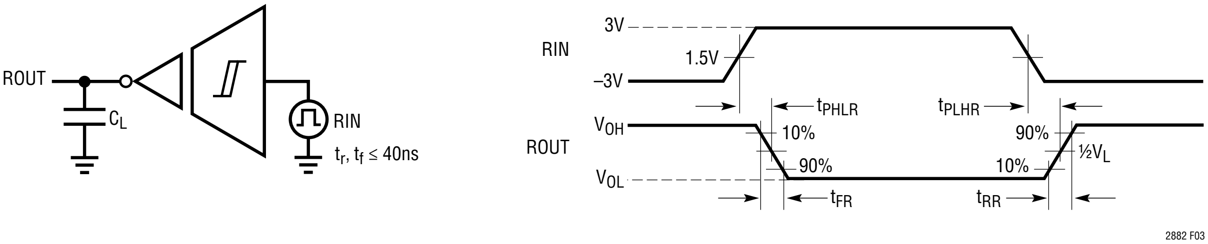


Figure 3. Receiver Timing Measurement

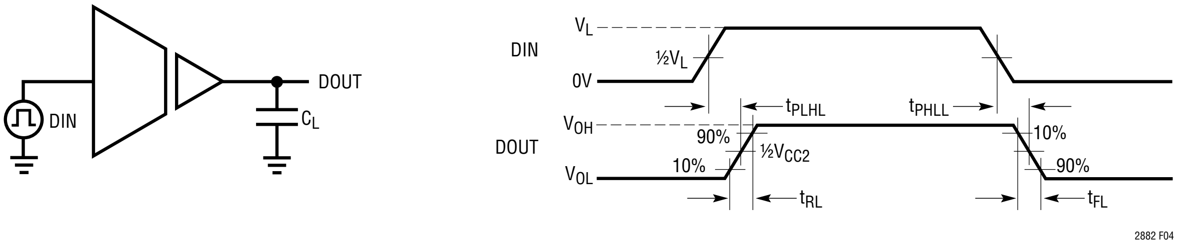


Figure 4. Auxiliary Channel Timing Measurement

PIN FUNCTIONS

LOGIC SIDE

R2OUT (Pin A1): Channel 2 RS232 Inverting Receiver Output. Controlled through isolation barrier from receiver input R2IN. Under the condition of an isolation communication failure R2OUT is in a high impedance state.

T2IN (Pin A2): Channel 2 RS232 Inverting Driver Input. A logic low on this input generates a high on isolated output T2OUT. A logic high on this input generates a low on isolated output T2OUT. Do not float.

R1OUT (Pin A3): Channel 1 RS232 Inverting Receiver Output. Controlled through isolation barrier from receiver input R1IN. Under the condition of an isolation communication failure R1OUT is in a high impedance state.

T1IN (Pin A4): Channel 1 RS232 Inverting Driver Input. A logic low on this input generates a high on isolated output T1OUT. A logic high on this input generates a low on isolated output T1OUT. Do not float.

DIN (Pin A5): General Purpose Non-Inverting Logic Input. A logic high on DIN generates a logic high on isolated output DOUT. A logic low on DIN generates a logic low on isolated output DOUT. Do not float.

ON (Pin A6): Enable. Enables power and data communication through the isolation barrier. If ON is high the part is enabled and power and communications are functional to the isolated side. If ON is low the logic side is held in reset and the isolated side is unpowered. Do not float.

V_L (Pin A7): Logic Supply. Interface supply voltage for pins DIN, R2OUT, T2IN, R1OUT, T1IN, and ON. Operating voltage is 1.62V to 5.5V. Internally bypassed to GND with 2.2µF.

V_{CC} (Pins A8, B7-B8): Supply Voltage. Operating voltage is 3.0V to 3.6V for LTM2882-3, and 4.5V to 5.5V for LTM2882-5. Internally bypassed to GND with 2.2µF.

GND (Pins B1-B6): Circuit Ground.

ISOLATED SIDE

GND2 (Pins K1-K7): Isolated Side Circuit Ground. These pads should be connected to the isolated ground and/or cable shield.

V_{CC2} (Pins K8, L7-L8): Isolated Supply Voltage Output. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to 5V. Supply voltage for pins R1IN, R2IN, DE, and DOUT. Internally bypassed to GND2 with 2.2µF.

R2IN (Pin L1): Channel 2 RS232 Inverting Receiver Input. A low on isolated input R2IN generates a logic high on R2OUT. A high on isolated input R2IN generates a logic low on R2OUT. Impedance is nominally 5kΩ in receive mode or unpowered.

T2OUT (Pin L2): Channel 2 RS232 Inverting Driver Output. Controlled through isolation barrier from driver input T2IN. High impedance when the driver is disabled (DE pin is low).

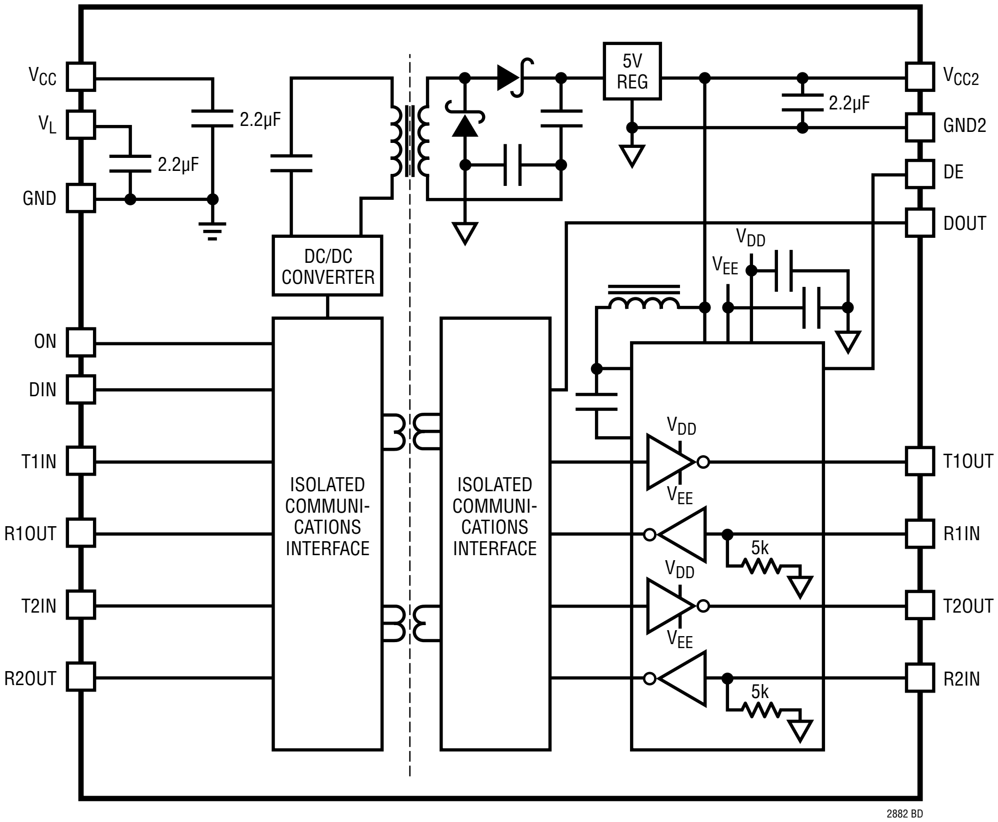
R1IN (Pin L3): Channel 1 RS232 Inverting Receiver Input. A low on isolated input R1IN generates a logic high on R1OUT. A high on isolated input R1IN generates a logic low on R1OUT. Impedance is nominally 5kΩ in receive mode or unpowered.

T1OUT (Pin L4): Channel 1 RS232 Inverting Driver Output. Controlled through isolation barrier from driver input T1IN. High impedance when the driver is disabled (DE pin is low).

DOUT (Pin L5): General Purpose Non-Inverting Logic Output. Logic output connected through isolation barrier to DIN.

DE (Pin L6): Driver Output Enable. A low input forces both RS232 driver outputs, T1OUT and T2OUT, into a high impedance state. A high input enables both RS232 driver outputs. Do not float.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Overview

The LTM2882 μModule transceiver provides a galvanically-isolated robust RS232 interface, powered by an integrated, regulated DC/DC converter, complete with decoupling capacitors. The LTM2882 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM2882 blocks high voltage differences, eliminates ground loops and is extremely tolerant of common mode transients between grounds. Error-free operation is maintained through common mode events greater than 30kV/μs providing excellent noise isolation.

μModule Technology

The LTM2882 utilizes isolator μModule technology to translate signals and power across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using coreless transformers formed in the μModule substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The μModule technology provides the means to combine the isolated signaling with our advanced dual RS232 transceiver and powerful isolated DC/DC converter in one small package.

DC/DC Converter

The LTM2882 contains a fully integrated isolated DC/DC converter, including the transformer, so that no external components are necessary. The logic side contains a full-bridge driver, running at about 2MHz, and is AC-coupled to a single transformer primary. A series DC blocking capacitor prevents transformer saturation due to driver duty cycle imbalance. The transformer scales the primary voltage, and is rectified by a full-wave voltage doubler. This topology eliminates transformer saturation caused by secondary imbalances.

The DC/DC converter is connected to a low dropout regulator (LDO) to provide a regulated low noise 5V output, V_{CC2}.

An integrated boost converter generates a 7V V_{DD} supply and a charge pumped –6.3V V_{EE} supply. V_{DD} and V_{EE} power the output stage of the RS232 drivers and are regulated to levels that guarantee greater than ±5V output swing.

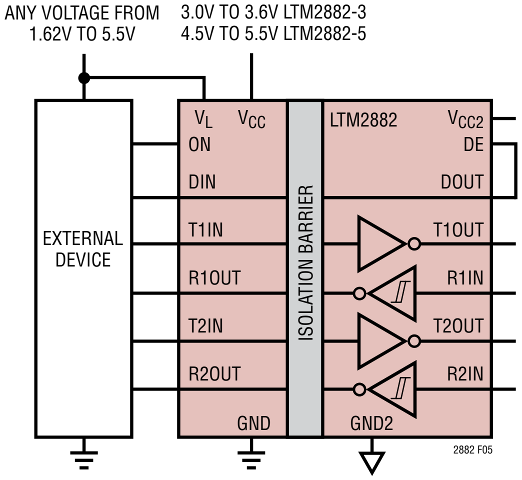


Figure 5. V_{CC} and V_L Are Independent

The internal power solution is sufficient to support the transceiver interface at its maximum specified load and data rate, and has the capacity to provide additional 5V power on the isolated side V_{CC2} and GND2 pins. V_{CC} and V_{CC2} are each bypassed internally with 2.2μF ceramic capacitors.

V_L Logic Supply

A separate logic supply pin V_L allows the LTM2882 to interface with any logic signal from 1.62V to 5.5V as shown in Figure 5. Simply connect the desired logic supply to V_L.

There is no interdependency between V_{CC} and V_L; they may simultaneously operate at any voltage within their specified operating ranges and sequence in any order. V_L is bypassed internally by a 2.2μF capacitor.

Hot Plugging Safely

Caution must be exercised in applications where power is plugged into the LTM2882's power supplies, V_{CC} or V_L, due to the integrated ceramic decoupling capacitors. The parasitic cable inductance along with the high Q characteristics of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage ratings and damage the LTM2882. Refer to Linear Technology Application Note 88, entitled "Ceramic Input Capacitors Can Cause Overvoltage Transients" for a detailed discussion and mitigation of this phenomenon.

APPLICATIONS INFORMATION

Channel Timing Uncertainty

Multiple channels are supported across the isolation boundary by encoding and decoding of the inputs and outputs. The technique used assigns T1IN/R1IN the highest priority such that there is no jitter on the associated output channels T1OUT/R1OUT, only delay. This preemptive scheme will produce a certain amount of uncertainty on T2IN/R2IN to T2OUT/R2OUT and DIN to DOUT. The resulting pulse width uncertainty on these low priority channels is typically ±6ns, but may vary up to about 40ns.

Half-Duplex Operation

The DE pin serves as a low-latency driver enable for half-duplex operation. The DE pin can be easily driven from the logic side by using the uncommitted auxiliary digital channel, DIN to DOUT. Each driver is enabled and disabled in less than 2μs, while each receiver remains continuously active. This mode of operation is illustrated in Figure 6.

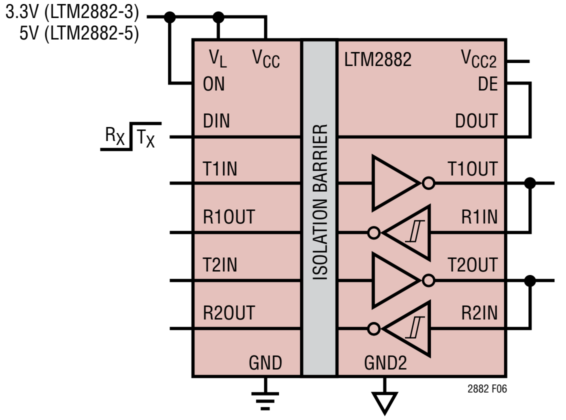


Figure 6. Half-Duplex Configuration Using D_{OUT} to Drive DE

Driver Overvoltage and Overcurrent Protection

The driver outputs are protected from short-circuits to any voltage within the absolute maximum range of ±15V relative to GND2. The maximum current is limited to no more than 70mA to maintain a safe power dissipation and prevent damaging the LTM2882.

Receiver Overvoltage and Open Circuit

The receiver inputs are protected from common mode voltages of ±25V relative to GND2.

Each receiver input has a nominal input impedance of 5kΩ relative to GND2. An open circuit condition will generate a logic high on each receiver's respective output pin.

RF, Magnetic Field Immunity

The LTM2882 has been independently evaluated and has successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3	Radiated, Radio-Frequency, Electromagnetic Field Immunity
EN 61000-4-8	Power Frequency Magnetic Field Immunity
EN 61000-4-9	Pulsed Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 1.

Table 1

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3, Annex D	80MHz to 1GHz	10V/m
	1.4MHz to 2GHz	3V/m
	2GHz to 2.7GHz	1V/m
EN 61000-4-8, Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8, Level 5	60Hz	100A/m*
EN 61000-4-9, Level 5	Pulse	1000A/m

*Non IEC Method

APPLICATIONS INFORMATION

PCB Layout

The high integration of the LTM2882 makes PCB layout very simple. However, to optimize its electrical isolation characteristics, EMI, and thermal performance, some layout considerations are necessary.

- Under heavily loaded conditions V_{CC} and GND current can exceed 300mA. Sufficient copper must be used on the PCB to insure resistive losses do not cause the supply voltage to drop below the minimum allowed level. Similarly, the V_{CC2} and GND2 conductors must be sized to support any external load current. These heavy copper traces will also help to reduce thermal stress and improve the thermal conductivity.
- Input and Output decoupling is not required, since these components are integrated within the package. An additional bulk capacitor with a value of 6.8µF to 22µF is recommended. The high ESR of this capacitor reduces board resonances and minimizes voltage spikes caused by hot plugging of the supply voltage. For EMI sensitive applications, an additional low ESL ceramic capacitor of 1µF to 4.7µF, placed as close to the power and ground terminals as possible, is recommended. Alternatively, a number of smaller value parallel capacitors may be used to reduce ESL and achieve the same net capacitance.
- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The use of solid ground planes for GND and GND2 is recommended for non-EMI critical applications to optimize signal fidelity, thermal performance, and to minimize RF emissions due to uncoupled PCB trace conduction. The drawback of using ground planes, where EMI is of concern, is the creation of a dipole antenna structure which can radiate differential voltages formed between GND and GND2. If ground planes are used it is recommended to minimize their area, and use contiguous planes as any openings or splits can exacerbate RF emissions.
- For large ground planes a small capacitance (≤ 330pF) from GND to GND2, either discrete or embedded within the substrate, provides a low impedance current return path for the module parasitic capacitance, minimizing any high frequency differential voltages and substantially reducing radiated emissions. Discrete capacitance will not be as effective due to parasitic ESL. In addition, voltage rating, leakage, and clearance must be considered for component selection. Embedding the capacitance within the PCB substrate provides a near ideal capacitor and eliminates component selection issues; however, the PCB must be 4 layers. Care must be exercised in applying either technique to insure the voltage rating of the barrier is not compromised.

The PCB layout in Figures 7a to 7e show the low EMI demo board for the LTM2882. The demo board uses a combination of EMI mitigation techniques, including both embedded PCB bridge capacitance and discrete GND to GND2 capacitors. Two safety rated type Y2 capacitors are used in series, manufactured by Murata, part number GA342QR7GF471KW01L. The embedded capacitor effectively suppresses emissions above 400MHz, whereas the discrete capacitors are more effective below 400MHz.

EMI performance is shown in Figure 8, measured using a Gigahertz Transverse Electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, “Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides.”

APPLICATIONS INFORMATION

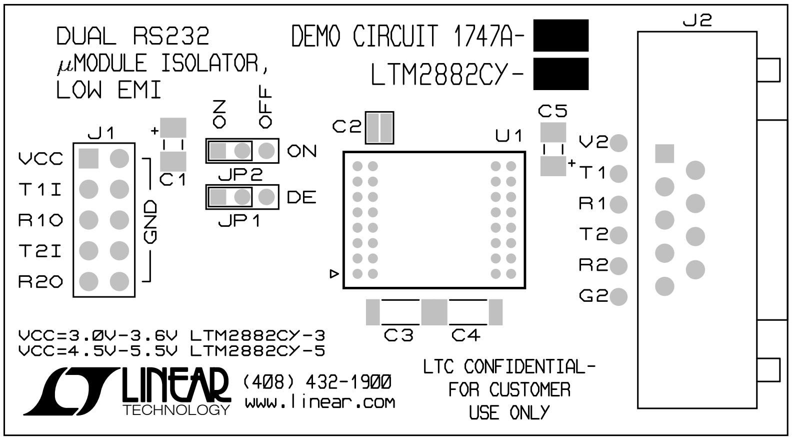


Figure 7a. Low EMI Demo Board Layout

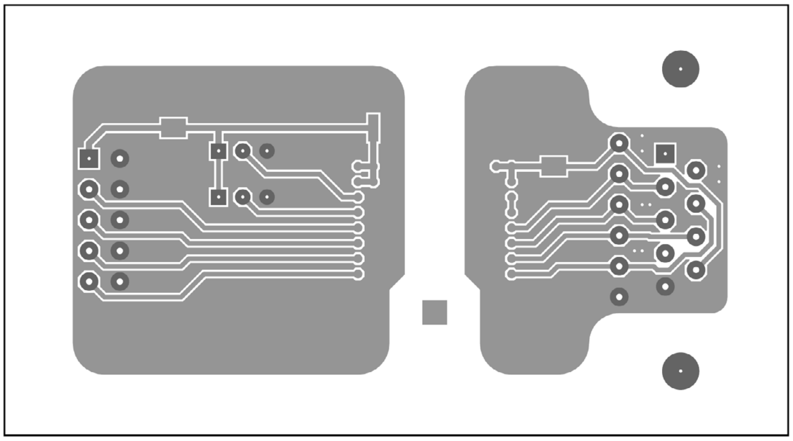


Figure 7b. Low EMI Demo Board Layout (DC1747A), Top Layer

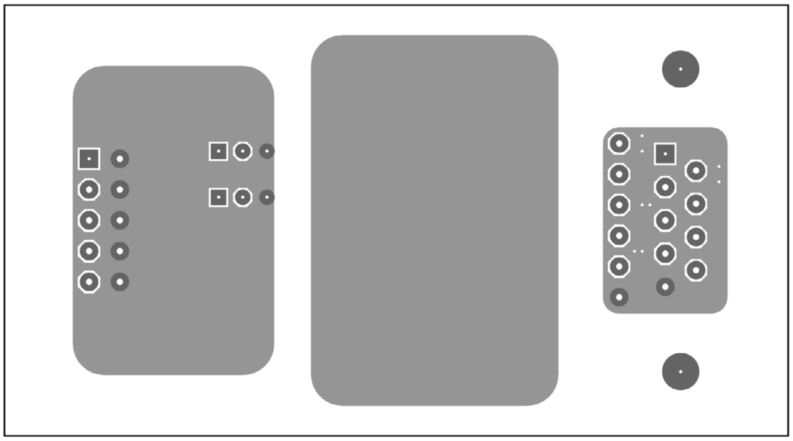


Figure 7c. Low EMI Demo Board Layout (DC1747A), Inner Layer 1

APPLICATIONS INFORMATION

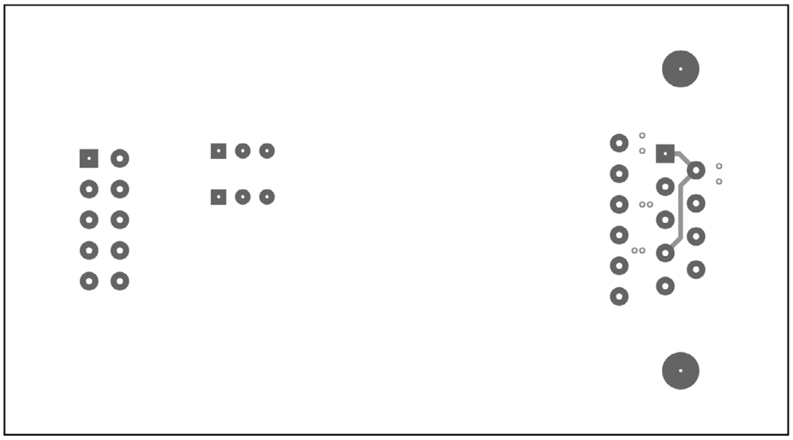


Figure 7d. Low EMI Demo Board Layout (DC1747A), Inner Layer 2

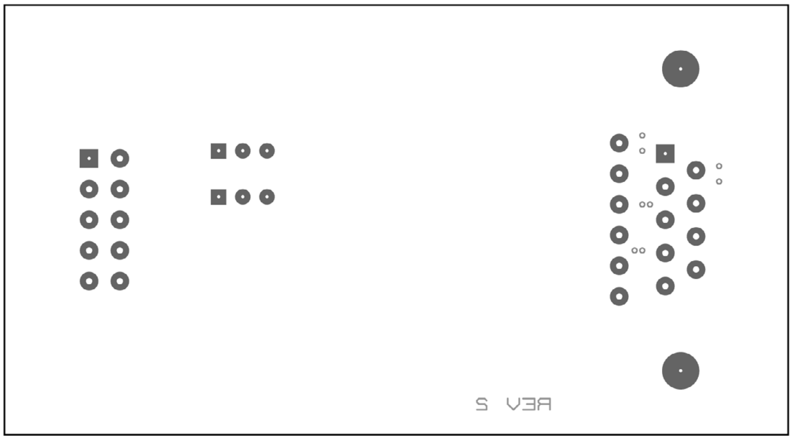


Figure 7e. Low EMI Demo Board Layout (DC1747A), Bottom Layer

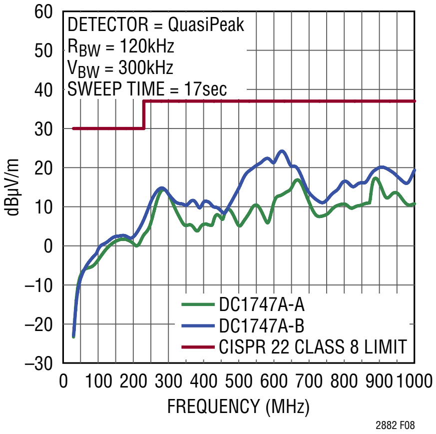


Figure 8. Low EMI Demo Board Emissions

TYPICAL APPLICATIONS

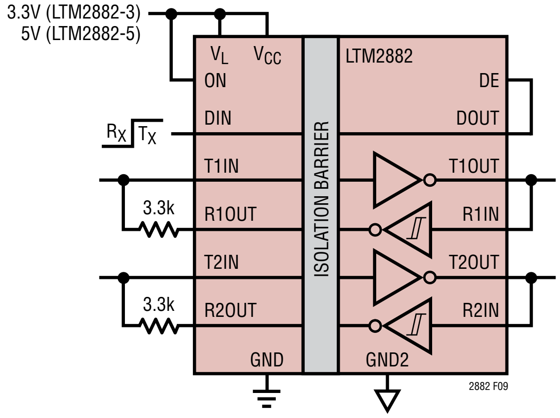
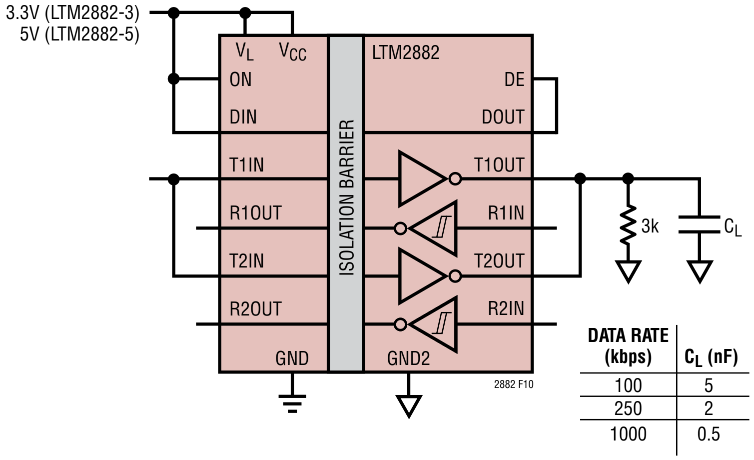


Figure 9. Single Line Dual Half-Duplex Isolated Transceiver



DATA RATE (kbps)	C_L (nF)
100	5
250	2
1000	0.5

Figure 10. Driving Larger Capacitive Loads

TYPICAL APPLICATIONS

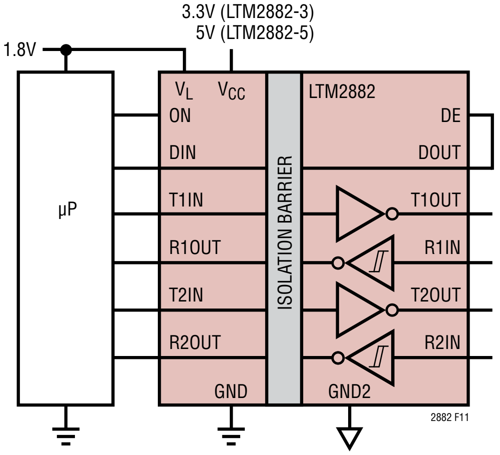


Figure 11. 1.8V Microprocessor Interface

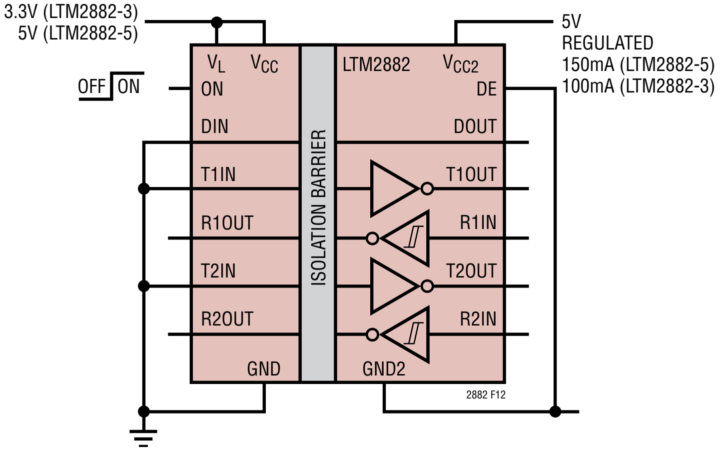


Figure 12. Isolated 5V Power Supply

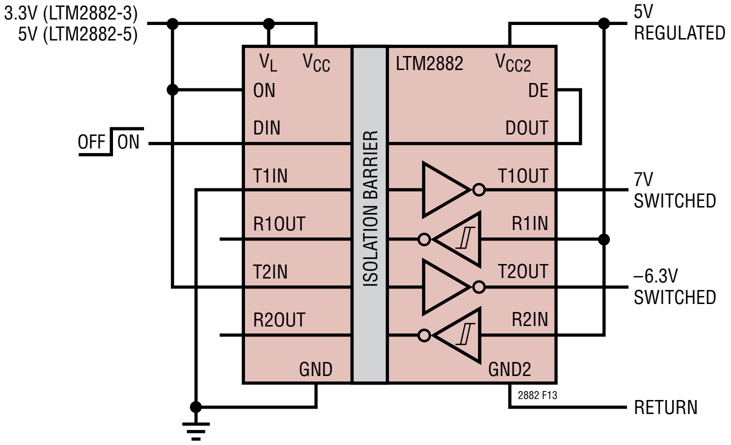
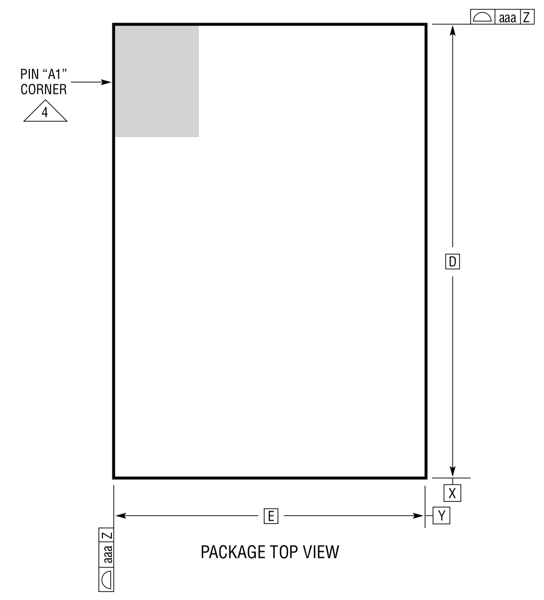


Figure 13. Isolated Multirail Power Supply with Switched Outputs

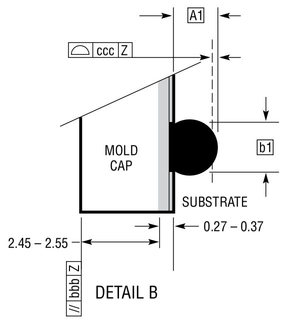
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM2882#packaging for the most recent package drawings.

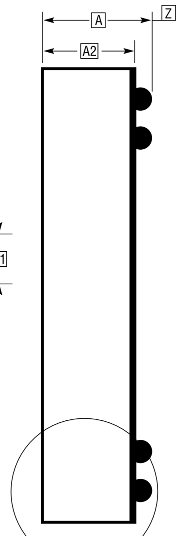
BGA Package
32-Lead (15mm × 11.25mm × 3.42mm)
(Reference LTC DWG # 05-08-1851 Rev D)



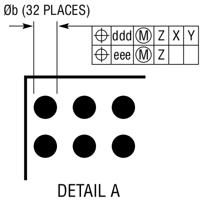
PACKAGE TOP VIEW



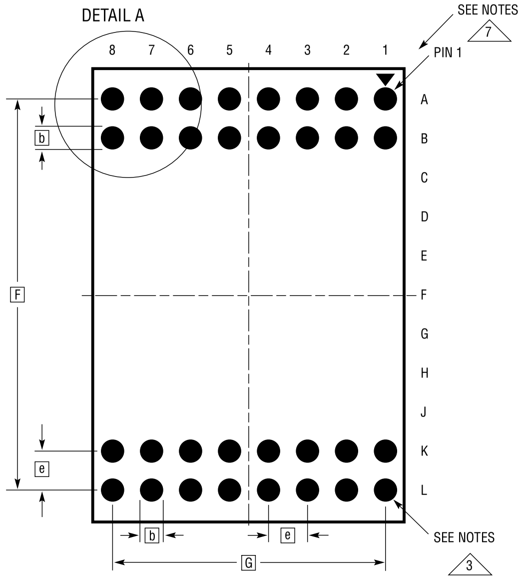
DETAIL B



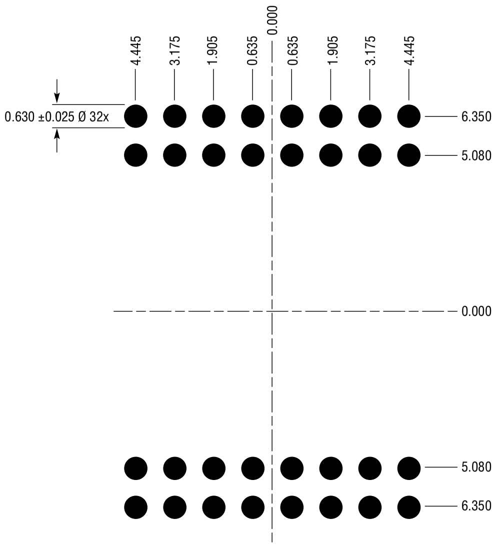
DETAIL B
PACKAGE SIDE VIEW



DETAIL A



PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

	DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.0		
E		11.25		
e		1.27		
F		12.70		
G		8.89		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	

TOTAL NUMBER OF BALLS: 32

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. ALL DIMENSIONS ARE IN MILLIMETERS

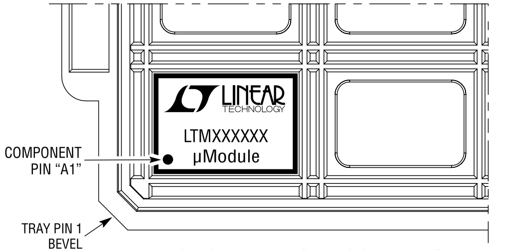
3 BALL DESIGNATION PER JESD MS-028 AND JEP95

4 DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE

5. PRIMARY DATUM -Z- IS SEATING PLANE

6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu

7 ⚠ PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



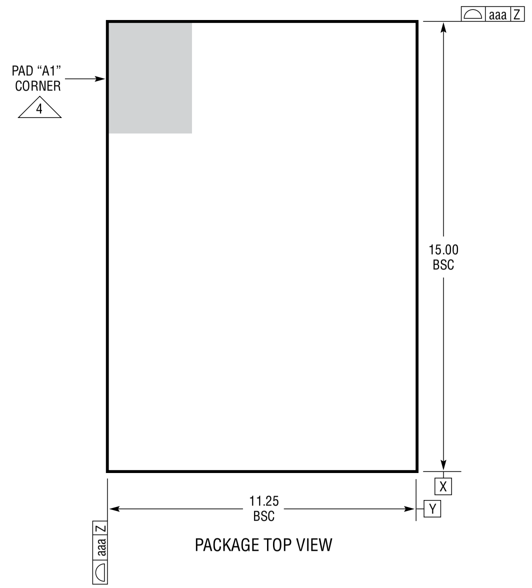
PACKAGE IN TRAY LOADING ORIENTATION

BGA 32 1112 REV D

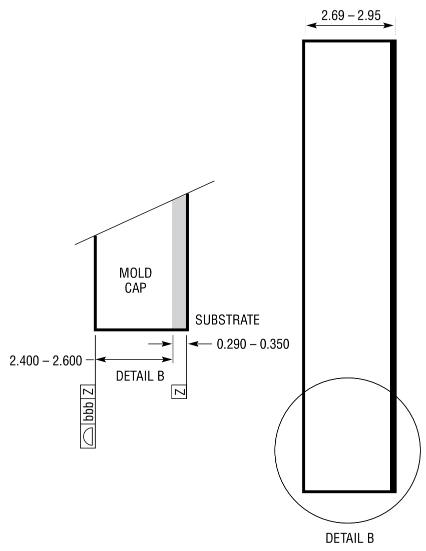
PACKAGE DESCRIPTION

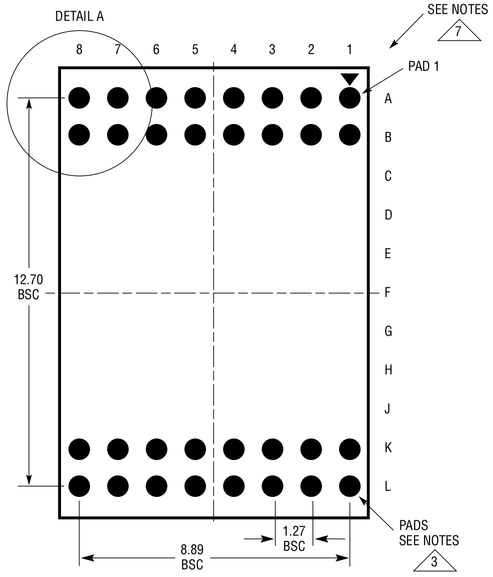
Please refer to http://www.linear.com/product/LTM2882#packaging for the most recent package drawings.

LGA Package
32-Lead (15mm × 11.25mm × 2.82mm)
(Reference LTC DWG # 05-08-1773 Rev A)

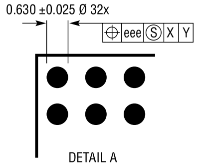


PACKAGE TOP VIEW

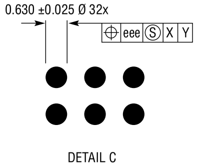




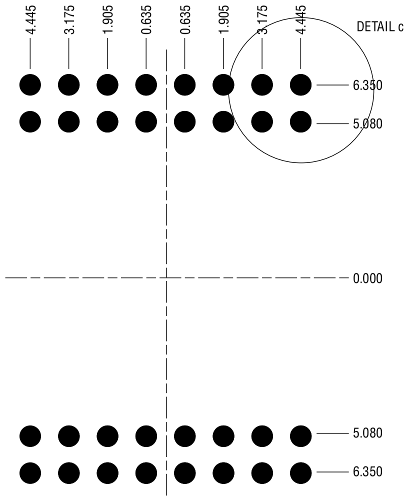
PACKAGE BOTTOM VIEW



DETAIL A



DETAIL C



SUGGESTED PCB LAYOUT
TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. ALL DIMENSIONS ARE IN MILLIMETERS

3 LAND DESIGNATION PER JESD MO-222

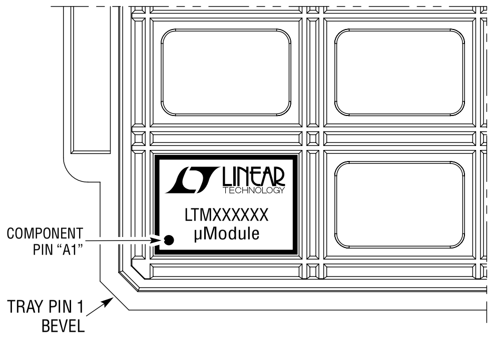
4 DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE

5. PRIMARY DATUM -Z- IS SEATING PLANE

6. THE TOTAL NUMBER OF PADS: 32

7 ⚠ PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

SYMBOL	TOLERANCE
aaa	0.10
bbb	0.10
eee	0.05



PACKAGE IN TRAY LOADING ORIENTATION

LGA 32 0113 REV A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	3/10	Changes to Features	1
		Add BGA Package to Pin Configuration, Order Information and Package Description Sections	2, 15
		Changes to LGA Package in Pin Configuration Section	2
		Update to Pin Functions	9
		Update to RF, Magnetic Field Immunity Section	12
		"PCB Layout Isolation Considerations" Section Replaced	13
B	3/11	H-Grade parts added. Reflected throughout the data sheet.	1-20
C	1/12	MP-Grade parts added. Reflected throughout the data sheet.	1-24
D	11/12	Storage temperature range updated.	2
E	5/14	Removed H-grade and MP-grade parts throughout the data sheet.	1-22
		Reduced Maximum Internal Operating Temperature and Storage Temperature Range.	2
		Added CTI and DTI parameters.	5
F	9/14	Revised Output Supply Short-Circuit Current (I_{CC2})	3
G	4/16	Added CSA information	1
		Revised I_{CC} (LTM2882-5) limit	3

TYPICAL APPLICATIONS

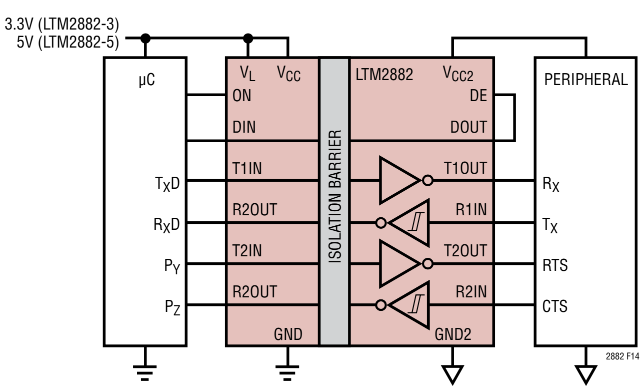


Figure 14. Isolated RS232 Interface with Handshaking

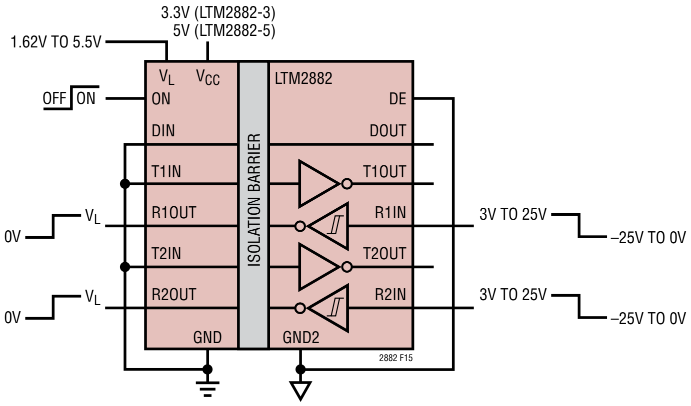


Figure 15. Isolated Dual Inverting Level Translator

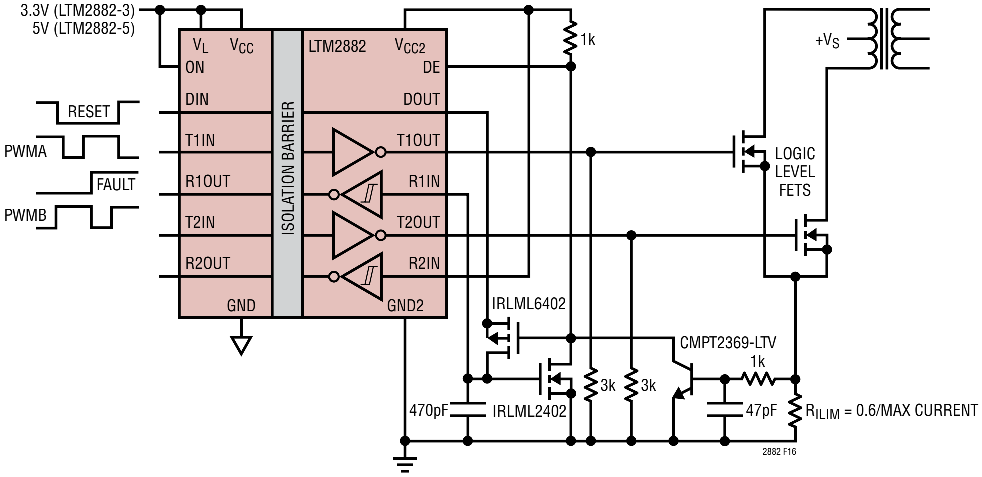


Figure 16. Isolated Gate Drive with Overcurrent Detection

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM2881	Isolated RS485/RS422 μModule Transceiver with Low EMI Integrated DC/DC Converter	20Mbps, ±15kV HBM ESD, 2500V_{RMS} Isolation with 1W Power
LTC2870/LTC2871	RS232/RS485 Multiprotocol Transceivers with Integrated Termination	20Mbps RS485 and 500kbps RS232, ±26kV ESD, 3V to 5V Operation
LTC2804	1Mbps RS232 Transceiver	Dual Channel, Full-Duplex, ±10kV HBM ESD
LTC1535	Isolated RS485 Transceiver	2500 V_{RMS} Isolation with External Transformer Driver
LTM2883	SPI/Digital or I^2C Isolated μModule with Adjustable 5V and 12V Rails	2500 V_{RMS} Isolation with Power in BGA Package
LTM2892	SPI/Digital or I^2C Isolated μModule	3500 V_{RMS} Isolation, 6 Channels

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