



ELECTRONICS

Product Information



Product Information

SAMSUNG TFT-LCD

MODEL NO. : LTN133AT07-001

LCD Development Team 3

Samsung Electronics Co . , LTD.



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GENERAL DESCRIPTION

DESCRIPTION

LTN133AT07-001 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight unit. The resolution of a 13.3" contains 1,280 x 800 pixels and can display up to 262,144 colors. 6 O'clock direction is the Optimum viewing angle.

FEATURES

- High contrast ratio, high aperture structure
- 1280 x 800 pixels resolution
- Low power consumption
- Fast Response
- Single CCFL
- DE(Data enable) only mode
- 3.3V LVDS Interface
- Onboard EEDID chip

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	268.08(H) x 178.80(V) (13.3" diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	262,144		
Number of pixel	1280 x RGB(3) x 800	pixel	16 : 10
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.2235(H) x 0.2235(V) (TYP.)	mm	113.6DPI
Display Mode	Normally white		
Surface treatment	Haze 0, Hard-Coating 3H		Glare

MECHANICAL INFORMATION

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal (H)	298.5	299.0	299.5	mm	
	Vertical (V)	194.5	195.0	195.5	mm	
	Depth (D)	-	-	5.5	mm	(1)
Weight		-	350	365	g	

Note (1) Measurement condition of outline dimension

. Equipment : Vernier Calipers

. Push Force : 500g ·f (minimum)

1. ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

$$V_{DD} = 3.3V, V_{SS} = GND = 0V$$

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V	(1)
Logic Input Voltage	V_{DD}	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V	(1)

Note (1) Within T_a ($25 \pm 2^\circ\text{C}$)

(2) BACK-LIGHT UNIT

$$T_a = 25 \pm 2^\circ\text{C}$$

Item	Symbol	Min.	Max.	Unit	Note
Lamp Current	I_L	3.0	7.0	mA _{rms}	(1)
Lamp frequency	F_L	50	80	kHz	(1)

Note 1) Permanent damage to the device may occur if maximum values are exceeded

Functional operation should be restricted to the conditions described under normal operating conditions.

2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state.

Measuring equipment : TOPCON BM-5A and PR-650

* Ta = 25 ± 2 °C, VDD=3.3V, fv= 60Hz, fDCLK = **68.9**MHz, IL = 6.0 mA

Item		Symbol	Condition	Min.	Typ.	Max	Unit
Contrast Ratio (5 Points)		CR		300	500	-	-
Response Time at Ta (Rising + Falling)		T _{RT_BW}		-	25	35	msec
Average Luminance of White (5 Points)		Y _{L,AVE}	Normal Viewing Angle ϕ = 0 θ = 0	220	250	-	cd/m ²
Color Chromaticity (CIE)	Red	R _X		0.550	0.580	0.610	-
		R _Y		0.310	0.340	0.370	
	Green	G _X		0.290	0.320	0.350	
		G _Y		0.510	0.540	0.570	
	Blue	B _X		0.135	0.155	0.185	
		B _Y		0.095	0.125	0.155	
	White	W _X		0.283	0.313	0.343	
		W _Y		0.299	0.329	0.359	
Viewing Angle	Hor.	θ _L		CR ≥ 10	40	45	-
		θ _H	40		45	-	
	Ver.	ϕ _H	10		15	-	
		ϕ _L	25		30	-	
13 Points White Variation		δ _L		-	-	1.8	-

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta= 25 ± 2°C

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply		V _{DD}	3.0	3.3	3.6	V	
Differential Input Voltage for LVDS Receiver Threshold	High	V _{IH}	-	-	+100	mV	V _{CM} = +1.2V
	Low	V _{IL}	-100	-	-	mV	
Vsync Frequency		f _v	-	60	-	Hz	
Hsync Frequency		f _h	-	49.38	-	KHz	f _v *823
Main Frequency		f _{DCLK}	-	71.1	-	MHz	f _h *1440
Rush Current		I _{RUSH}	-	-	1.5	A	(4)
Current of Power Supply	White	I _{DD}	-	280	-	mA	(2),(3)*a
	Mosaic		-	300	-	mA	(2),(3)*b
	V. stripe		-	350	400	mA	(2),(3)*c

Note (1) Display data pins and timing signal pins should be connected.(GND = 0V)

(2) f_v = 60Hz, f_{DCLK} = 68.9MHZ, V_{DD} = 3.3V , DC Current.

(3) Power dissipation pattern

3.2 BACK-LIGHT UNIT

The backlight system is an edge-lighting type with a single CCFT (Cold Cathode Fluorescent Tube).
The characteristics of a single lamp are shown in the following table.

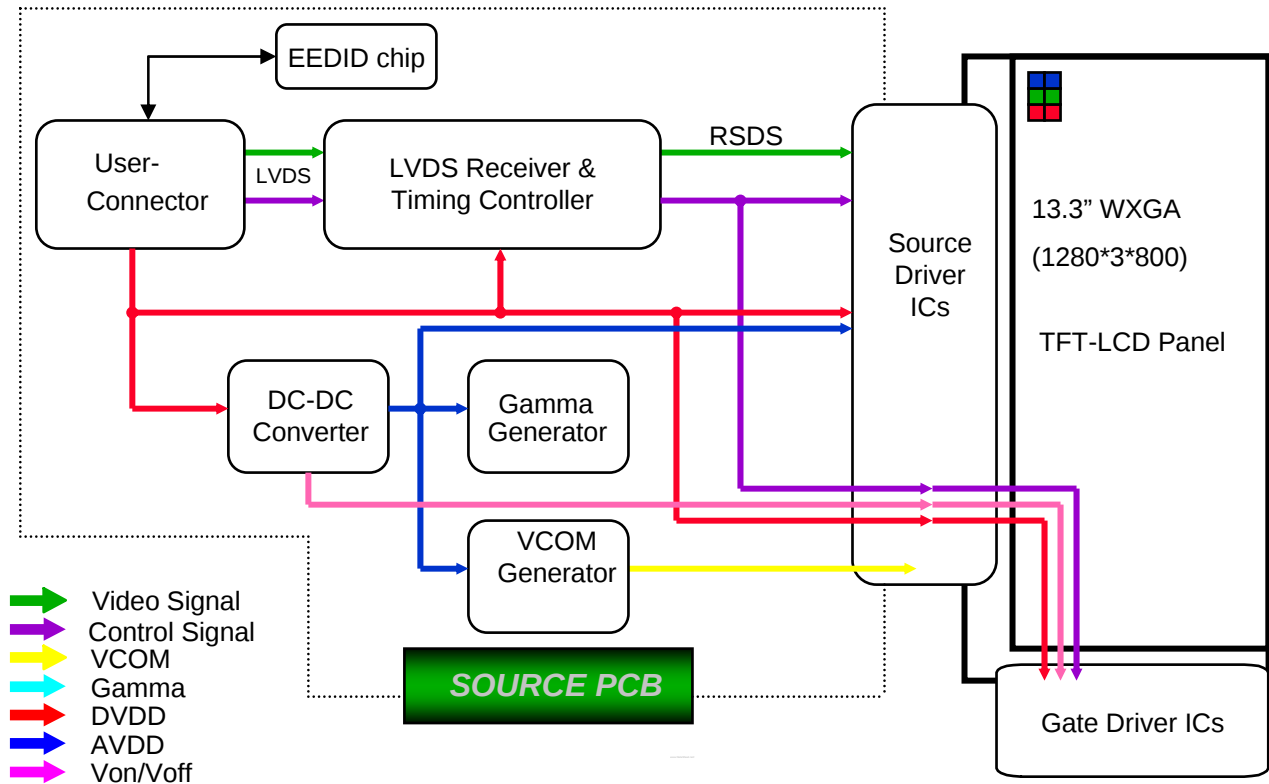
- INVERTER : SEM SIC 130T

Ta= 25 ± 2 °C

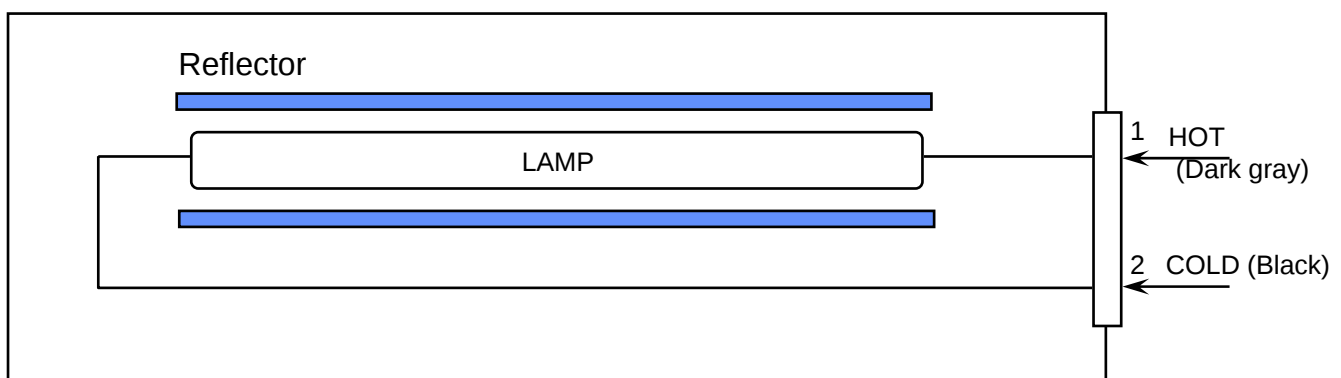
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Lamp Current	I _L	3.0	6.0	6.5	mArms	
Lamp Voltage	V _L	-	640	-	Vrms	I _L = 6.0mA
Frequency	f _L	50	60	65	KHz	
Power Consumption	P _L	-	3.84	-	W	I _L = 6.0mA
Operating Life Time	Hr	10,000	-	-		I _L = 6.5mA
Startup Voltage	V _s	-	-	1080	Vrms	25°C
				1295	Vrms	0°C

4. BLOCK DIAGRAM

4.1 TFT LCD Module



4.2 BACK-LIGHT UNIT



Note) The output of the inverter may change according to the material of the reflector.

5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (LVDS, Connector : HIROSE DF-19KR-20P-1H)

No.	Symbol	Function	Polarity	Remarks
1	VSS	Ground		
2	VDD	POWER SUPPLY +3.3V		
3	VDD	POWER SUPPLY +3.3V		
4	VEEDID	DDC 3.3V Power		
5	NC	No Connection		
6	CLKEDID	DDC Clock		
7	DATAEDID	DDC data		
8	RxIN0-	LVDS Differential Data INPUT (R0-R5,G0)	Negative	
9	RxIN0+	LVDS Differential Data INPUT (R0-R5,G0)	Positive	
10	GND	Ground		
11	RxIN1-	LVDS Differential Data INPUT (G1-G5,B0-B1)	Negative	
12	RxIN1+	LVDS Differential Data INPUT (Odd G1-G5,B0-B1)	Positive	
13	GND	Ground		
14	RxIN2-	LVDS Differential Data INPUT (B2-B5,Sync,DE)	Negative	
15	RxIN2+	LVDS Differential Data INPUT (B2-B5,Sync,DE)	Positive	
16	GND	Ground		
17	RxCLK-	LVDS Differential Data INPUT	Negative	
18	RxCLK+	LVDS Differential Data INPUT	Positive	
19	GND	Ground		
20	GND	Ground		

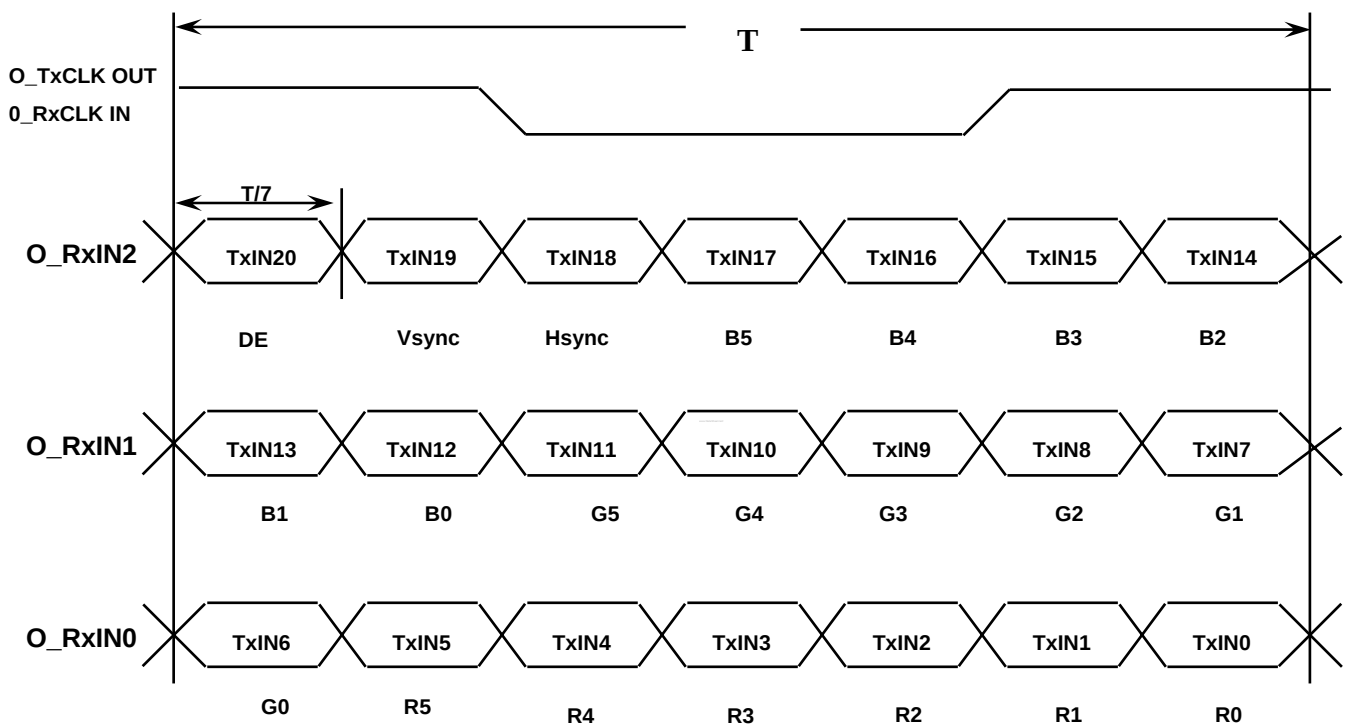
5.2 BACK LIGHT UNIT

Connector : JST BHSR - 02VS -1
Mating Connector : SM02B-BHSS-1(JST)

Pin NO.	Symbol	Color	Function
1	HOT	Dark gray	High Voltage
2	COLD	Black	Low Voltage

5.3 Timing Diagrams of LVDS For Transmission

LVDS Receiver : Integrated T-CON

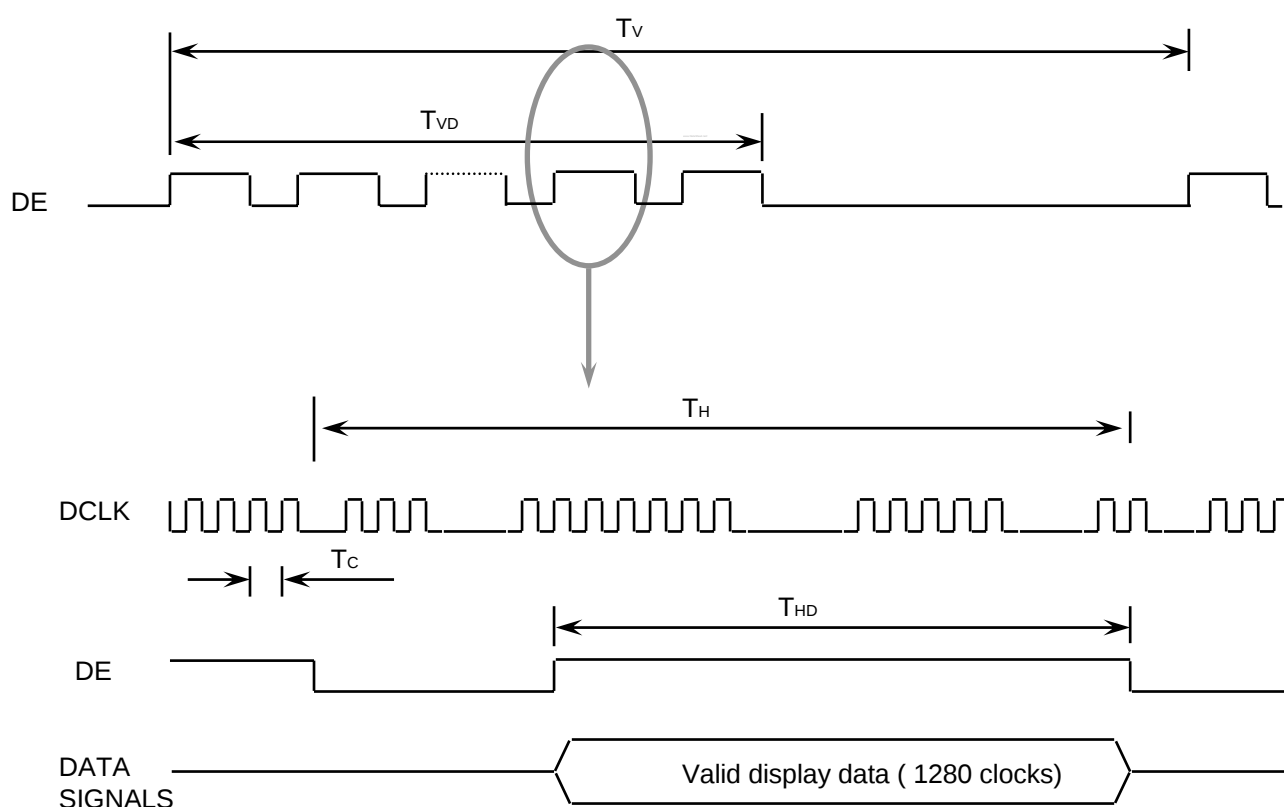


6. INTERFACE TIMING

6.1 Timing Parameters

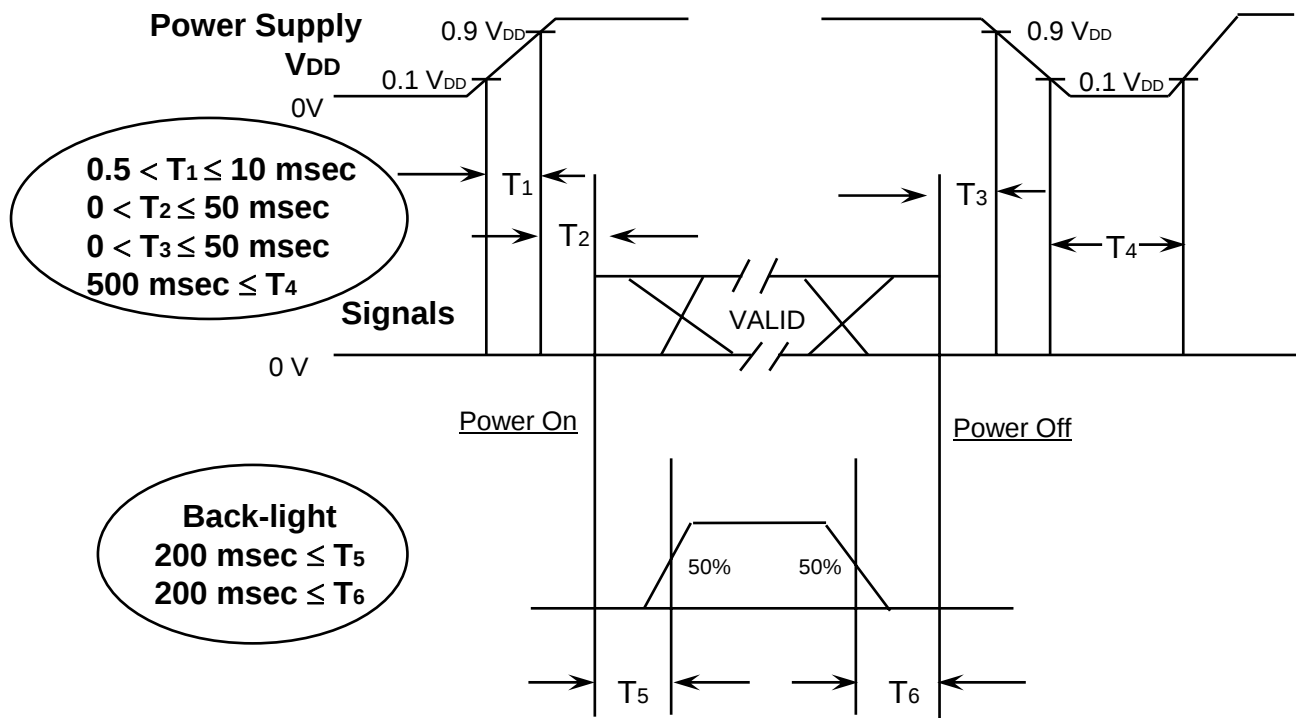
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frame Frequency	Cycle	TV	804	823	833	Lines	
Vertical Active Display Term	Display Period	TVD	-	800	-	Lines	
One Line Scanning Time	Cycle	TH	1316	1440	1500	Clocks	
Horizontal Active Display Term	Display Period	THD	-	1280	-	Clocks	

6.2 Timing diagrams of interface signal



6.3 Power ON/OFF Sequence

: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

- T1 : Vdd rising time from 10% to 90%
- T2 : The time from Vdd to valid data at power ON.
- T3 : The time from valid data off to Vdd off at power Off.
- T4 : Vdd off time for Windows restart
- T5 : The time from valid data to B/L enable at power ON.
- T6 : The time from valid data off to B/L disable at power Off.

NOTE.

- (1) The supply voltage of the external system for the module input should be the same as the definition of VDD.
- (2) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become white.
- (3) In case of VDD = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

7. MECHANICAL OUTLINE DIMENSION

[Refer to the next page]

