SAMSUNG ELECTRONICS

Approval

TO

DATE : August 29, 2001

SAMSUNG TFT-LCD

MODEL NO. : LTN141P2-L01

Notes :

Any Modification of Spec is not allowed without SEC' permission

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PREPARED BY : **Application Engineering Team**

SAMSUNG ELECTRONICS CO., LTD.

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CONTENTS

Revision History

Approval

Date	Rev.No.	Page	Summary
Mar.13.2000	000	ALL	LTN141P2-L01 SXGA-Plus(1400X1050 pixel) MODEL was first issued.
April.20.2000	001	13 14,16	To add EDID into block diagram of LCD module To change the pin description of interface connector
Sept.28.2000	002	ALL 7 13 15 16,18 20,21 24 27,28,29	Approval spec was issued. Update color chromaticity. Add Inverter electrical characteristics Add Inverter block diagram Update Input termination pin assignment (SPWG 2.O version) Add Inverter input pin definition Update interface timing.(DE only mode) Add items(Packing, Marking and Others)
Oct. 03.2000	003	13	Update Inverter electrical characteristics
Mar. 16.2001	004	13	Add the measurement condition.
April. 19.2001	005	1 26	LTN141P2-L01(EMI Solution)Model was first issued Update outline dimension.
Aug. 29.2001	006	1 26	LTN141P2-L01(RSDS)Model was first issued Update outline dimension.

GENERAL DESCRIPTION

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DESCRIPTION

LTN141P2-L01 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a TFT LCD panel, a driver circuit and a back-light system. The resolution of a 14.1″ contains 1400 x 1050 pixels and can display up to 262,144colors. 6 o'clock direction is the optimum viewing angle.

FEATURES

- Thin and light weight
- High contrast ratio
- SXGA-Plus (1400x1050 pixels) resolution
- Low power consumption
- DE (Data enable) only mode.

APPLICATIONS

- Notebook PC and desktop monitors
- Display terminals for AV application products
- Monitors for Industrial machine
- If the usage of this product is not for PC application, but for others, please contact SEC.

GENERAL INFORMATION

ITEM	SPECIFICATION	UNIT	NOTE
Display area	285.6(H) x 214.2(V) (14.1″ diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	262,144		
Number of pixel	1400 x 1050 (SXGA-Plus)	pixel	
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.204(H) x 0.204(V) (TYP.)	mm	124dpi
Display Mode	Normally white		
Surface treatment	HAZE 25, HARD-COATING 3H		

ITEM		MIN.	TYP.	MAX.	NOTE
Module size	Horizontal (H)	285.5	299	299.5	LCD panel only
	Vertical (V)	227.5	228	228.5	
	Depth (D)	5.7	6.0	6.4	
Weight		-	530	550	LCD panel only
			545	565	Inverter assembly

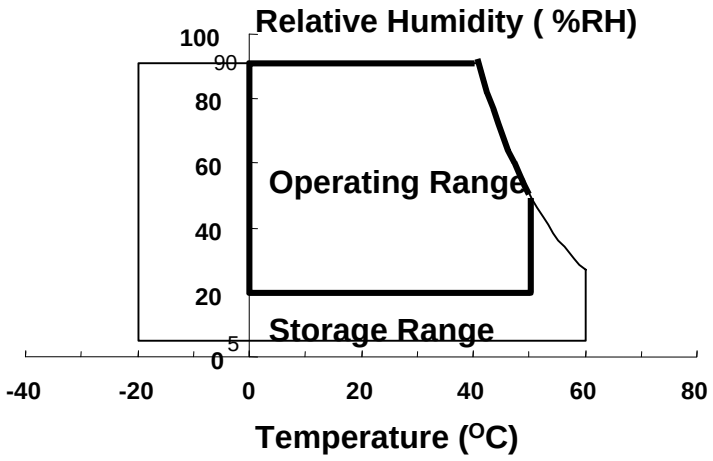
Note (1) Measurement condition of outline dimension
. Equipment : Vernier Calipers
. Push Force : 500g ·f (minimum)
(2) User Hole Torque : 2.8 kg·f·cm, 5 times

1. ABSOLUTE MAXIMUM RATINGS

1.1 ABSOLUTE RATINGS OF ENVIRONMENT

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Storage temperature	T_{STG}	-20	60	%°C	(1)
Operating temperature (Temperature of glass surface)	T_{OPR}	0	50	%°C	(1)
Shock (non-operating)	Snop	-	220	G	(2),(4)
Vibration (non-operating)	Vnop	-	1. 5	G	(3),(4)

Note (1) Temperature and relative humidity range are shown in the figure below.
90 % RH Max. (40 °C ≥ Ta)
Maximum wet - bulb temperature at 39 °C or less. (Ta > 40%°C) No condensation.



(2) (2)ms, (half) sine wave, one time for ± X, ± Y, ± Z.
(3) (10) - (300) Hz, Sweep rate (10) min, (30)min for X,Y,Z.
(4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.

1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

(Vss = GND = 0 V)

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Power Supply Voltage	V_{DD}	Vss -0.3	4.0	V	(1)
Logic Input Voltage	V_{IN}	Vss -0.3	VDD+0.3	V	(1)

NOTE (1) Within Ta = 25 ± 2 °C

(2) BACK-LIGHT UNIT

Ta = 25 ± 2 °C

ITEM	SYMBOL	MIN.	MAX.	UNIT.	NOTE
Lamp current	I_L	3.0	7.0	mA_{rms}	(1)
Lamp frequency	F_L	40	80	KHz	(1)

NOTE (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

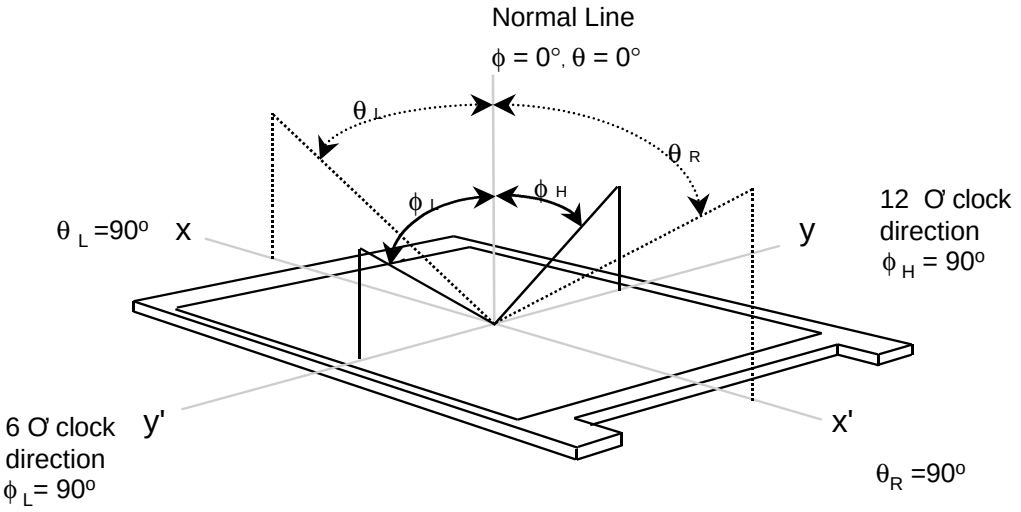
2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5).
Measuring equipment : TOPCON BM-5A

* Ta = 25 ± 2°C , V_{DD}=3.3V, fv= 60Hz, f_{DCLK}=54MHz, I_L =6.0 mA

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Contrast Ratio (5 Points)		CR	ϕ = 0, θ = 0 Normal Viewing Angle	150	180	-		
Response Time at Ta	Rising	T_R		-	10	20	msec	(1), (3)
	Falling	T_F		-	30	50		
Average Luminance of White (5 Points)		$Y_{L,AVE}$		120	150	-	cd/m^2	(1), (4)
Color Chromaticity (CIE)	Red	R_X		0.529	0.559	0.589		(1), (5)
		R_Y		0.304	0.334	0.364		
	Green	G_X		0.273	0303	0.333		
		G_Y		0.508	0.538	0.568		
	Blue	B_X		0.123	0.153	0.183		
		B_Y		0.103	0.133	0.163		
	White	W_X		0.283	0.313	0.343		
		W_Y		0.299	0.329	0.359		
Viewing Angle	Hor.	θ_L	CR(at center point) ≥ 10	40	-	-	Degrees	
		θ_R		40	-	-		
	Ver.	ϕ_H		15	-	-		
		ϕ_L		35	-	-		
13 Points White Variation		δ_L		-	-	2.0		(6)

Note 1) Definition of Viewing Angle : Viewing angle range($10 \leq C/R$)

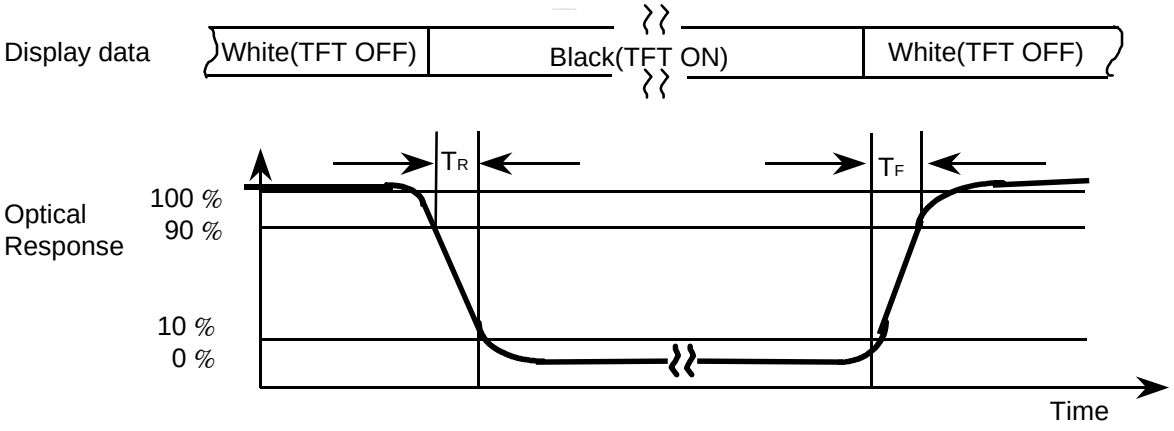


Note 2) Definition of Contrast Ratio (CR) : Ratio of gray max (Gmax) ,gray min (Gmin) at 5 points(4, 5, 7, 9, 10)

$$CR = \frac{CR(4) + CR(5) + CR(7) + CR(9) + CR(10)}{5}$$

POINTS : ④ , ⑤ , ⑦ , ⑨ , ⑩ at FIGURE OF NOTE 6)

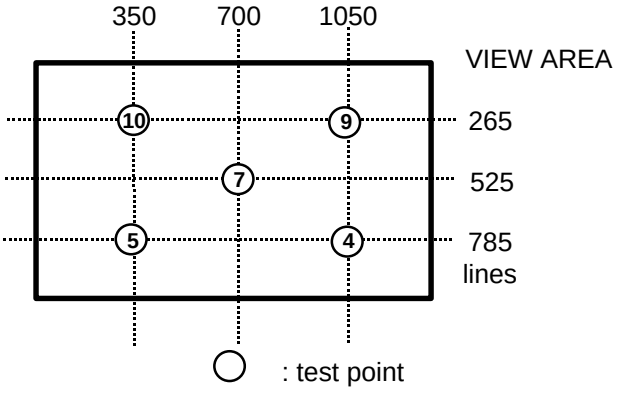
Note 3) Definition of Response time :



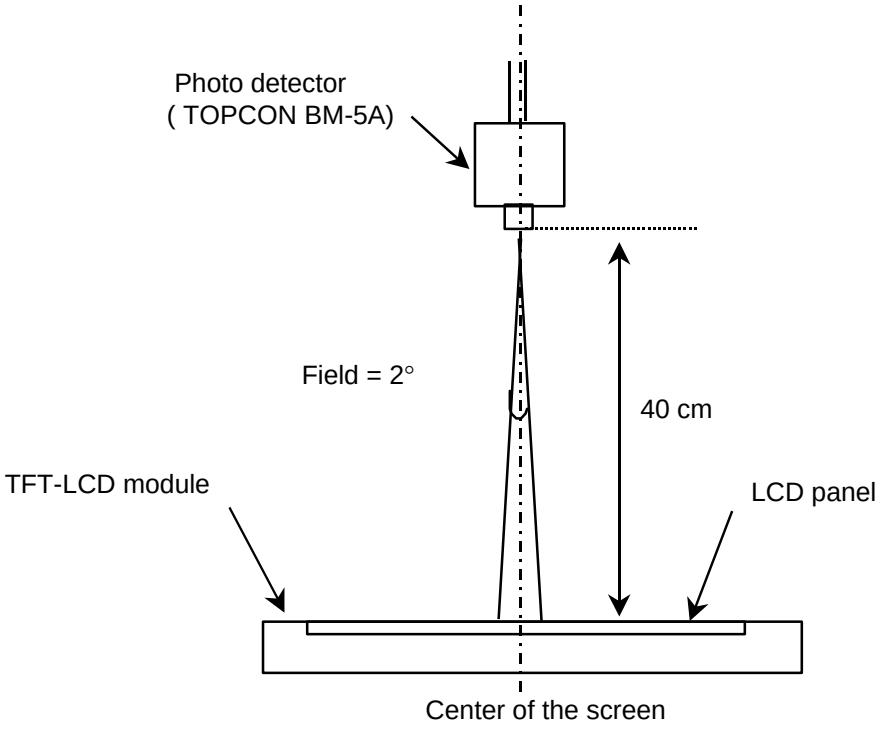
Note 4) Definition of Average Luminance of White : measure the luminance of white at 5 points.

Average Luminance of White ($Y_{L,AVE}$)

$$Y_{L,AVE} = \frac{Y_{L4} + Y_{L5} + Y_{L7} + Y_{L9} + Y_{L10}}{5}$$



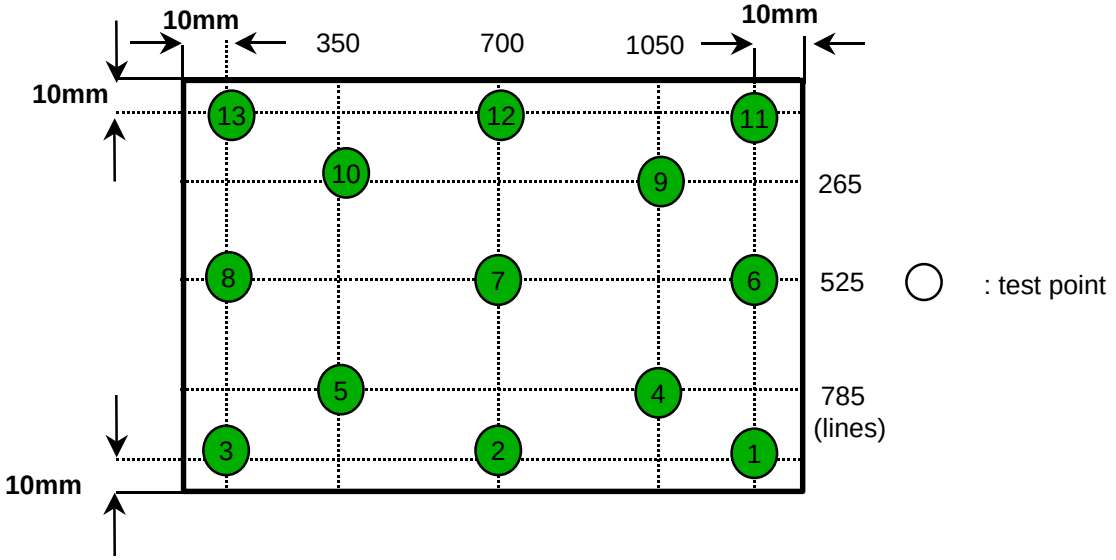
Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 minutes, the measurement should be executed. Measurement should be executed in a stable, windless,and dark room.
30 minutes after lighting the back-light. This should be measured in the center of screen.
Lamp current : 6.0 mA
Environment condition : Ta = 25 ± 2 °C



Optical characteristics measurement setup

Note 6) Definition of 13 points white variation (δ_W), CR variation(C_{VER}) [① ~ ⑬]

$$\delta_L = \frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}}$$



3. ELECTRICAL CHARACTERISTICS

Approval

3.1 TFT LCD MODULE

Ta = 25 ± 2%°C

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Voltage of Power Supply		V_{DD}	3.0	3.3	3.6	V	
Differential Input Voltage for LVDS Receiver Threshold	High	V_{IH}	-	-	+100	mV	(1)
	Low	V_{IL}	-100	-	-	mV	
Vsync Frequency		fv	-	60	-	Hz	
Hsync Frequency		f_H	-	63.98	-	KHz	
Main Frequency		f_{DCLK}	-	54	-	MHz	
Rush Current		I_{RUSH}	-	-	1.5	A	(5)
Current of Power Supply	White	I_{DD}	-	400	-	mA	(2),(4)
	Mosaic		-	450	-	mA	(2),(4)
	V.stripe		-	550	600	mA	(2),(4)

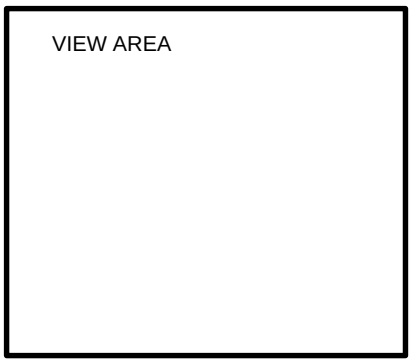
Note (1) Condition : V_{CM}=+1.2V(Common mode Voltage)

(2) f_V=60Hz, f_{DCLK} =54MHZ, Vdd = 3.3V , DC Current.

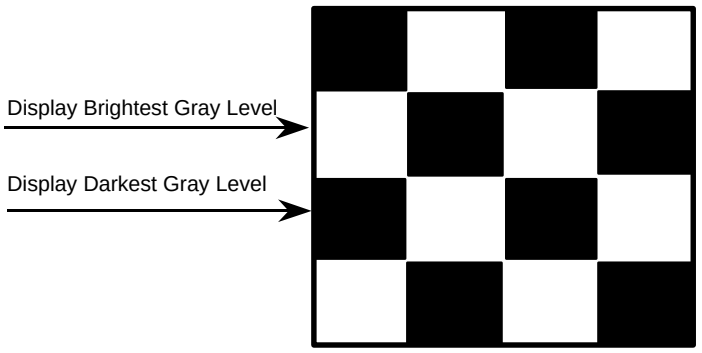
(3) 1 pixel /clock

(4) Power dissipation check pattern

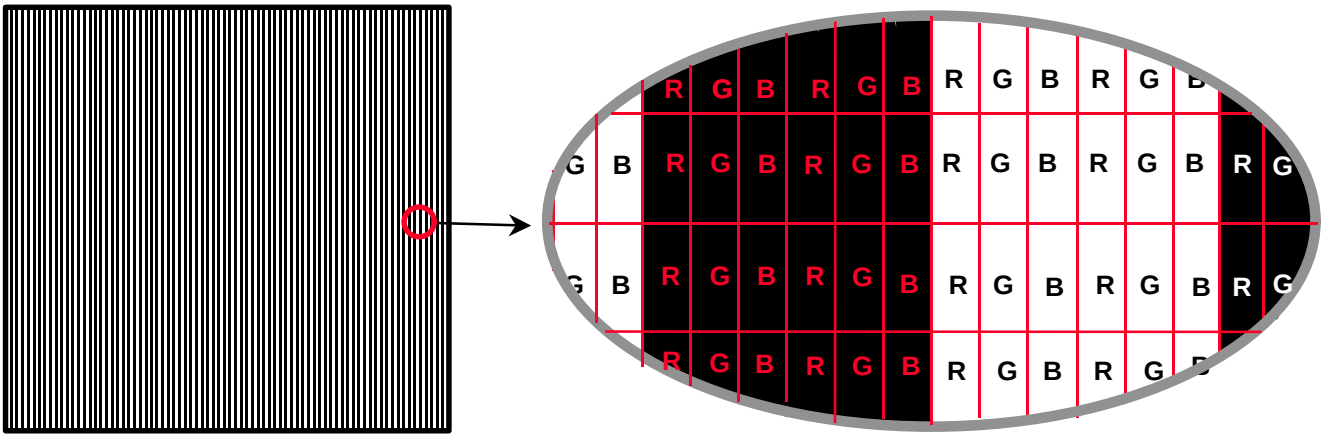
*a) White Pattern



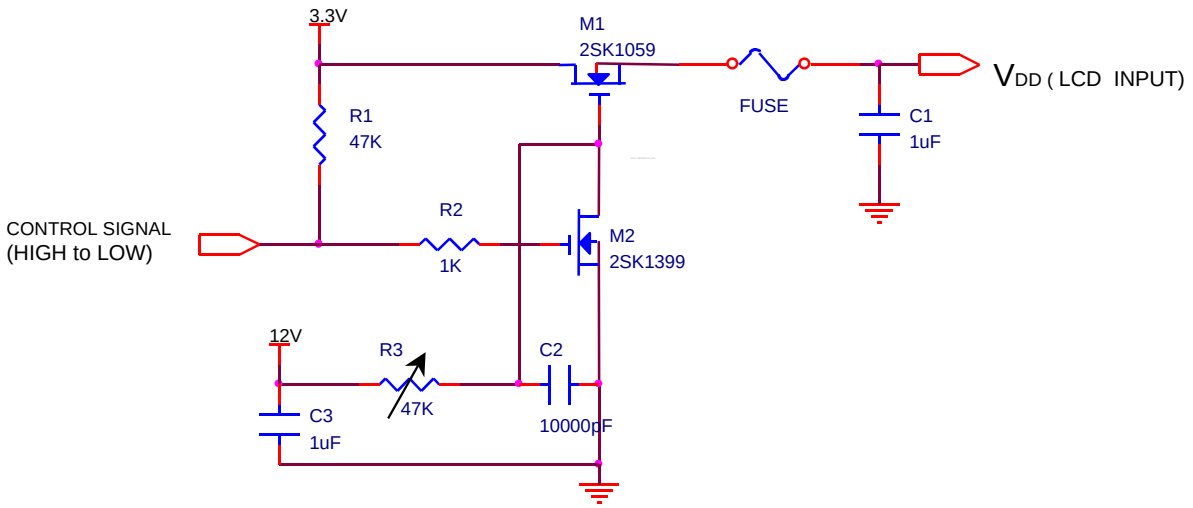
*b)Mosaic Pattern



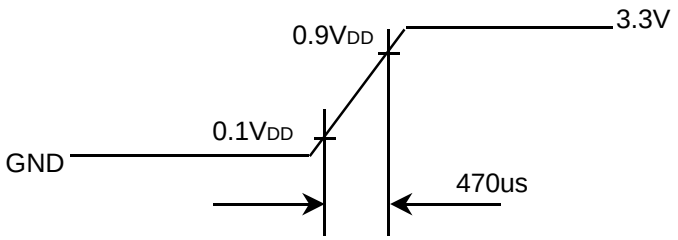
*c) Vertical stripe pattern



5) Rush current measurement condition



VDD rising time is 470us



3.2 BACKLIGHT UNIT

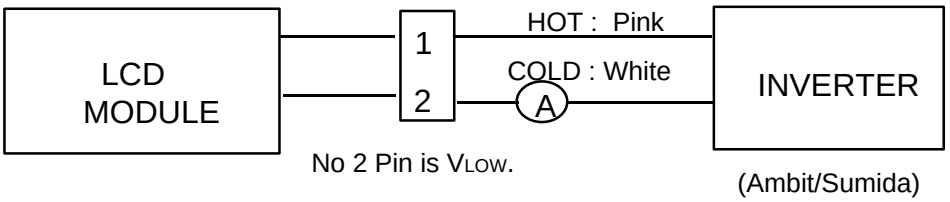
The back-light system is an edge - lighting type with a single CCFT (Cold Cathode Fluorescent Tube).
The characteristics of a single lamp are shown in the following tables.

INVERTER : AMBIT/SUMIDA Ta = 25 ± 2°C

ITEM	SYMB	MIN	TYP	MAX	UNIT	NOTE
Lamp Current	I_L	3.0		6.5	mA_{rms}	(1)
Lamp Voltage	V_L	-	650	-	V_{rms}	I_L=6.0mA
Frequency	f_L	40	-	65	KHz	(2)
Power Consumption	P_L	-	4.0	-	W	(3) I_L=(6.0)mA
Operating Life Time	Hr	10,000	-	-	Hour	(4)
Startup Voltage	V_S	-	-	1100 (25°C) 1300 (0°C)	V_{rms}	(5)

Note) **The waveform of the inverter output voltage must be area symmetric and the design of the inverter must have specifications for the modularized lamp.**
The performance of the back-light, for example life time or brightness, is much influenced by the characteristics of the DC-AC inverter for the lamp. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.
When you design or order the inverter, please make sure that a poor lighting caused by the mismatch of the back-light and the inverter(miss lighting, flicker, etc.) never occur. When you confirm it, the module should be operated in the same condition as it is installed in your instrument.

Note (1) Lamp current is measured with a high frequency current meter as shown below.



(2) Lamp frequency may produce interference with horizontal synchronous frequency and this may cause line flow on the display. Therefore lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.

(3) refer to I_L X V_L to calculate.

(4) Life time (Hr) of a lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ± 2°C and I_L = (6.0) mA_{rms} until one of the following event occurs.
1. When the brightness becomes 50% or lower than it' s original.
2. When the Effective ignition length becomes 80% or lower than it' s original value.
(Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

(5) The voltage above this value should be applied to the lamp for more than 1 second to startup Otherwise the lamp may not be turned on.

3.3 INVERTER

Inverter : AMBIT, SUMIDA

Ta = 25 ± 2°C

ITEM		MIN	TYP	MAX	UNIT	NOTE
Input Voltage(Vin)		9.0	14.4	21.0	mArms	
Open Circuit Voltage		1200	1400	1700	Vrms	IL =6.0 mArms
Lamp Voltage			650		Vrms	
Lamp Current		2.0 ±5% @SMB_DAT FFH	-	6.0±5% @SMB_DAT 00H	mArms	Vin=14.4V
Efficiency	Optical	-	29	-	Nit/W	After 30min turn on at the center of LCD Vin=14.4V @6.0mA
	Electrical	-	81	85	%	
Operating Frequency		50±5	55±5	60±5	kHz	SMB_DAT=00H
Input Voltage Ripple		-	-	0.5	Vpp	Peak to peak value
Input Power Consumption		-	4.8	5.0	W	(1) Iout=6.0mArms
In-rush current		-	-	1	A	
Shutdown time		0.6	1.0	1.4	sec	
Start-up time		-	-	0.1	sec	(2)

Note

(1) Iin=330mA, Efficiency=81%

(2) Inverter start-up time

(3) Efficiency should be calculated as below formulation.

Optical efficiency = output Brightness(nits) / Input power(watt)

Electrical efficiency = output power / input power

(4) SEC recommends user to set the value of SMB_Data to meet the minimum current(3.0mA) of Lamp.

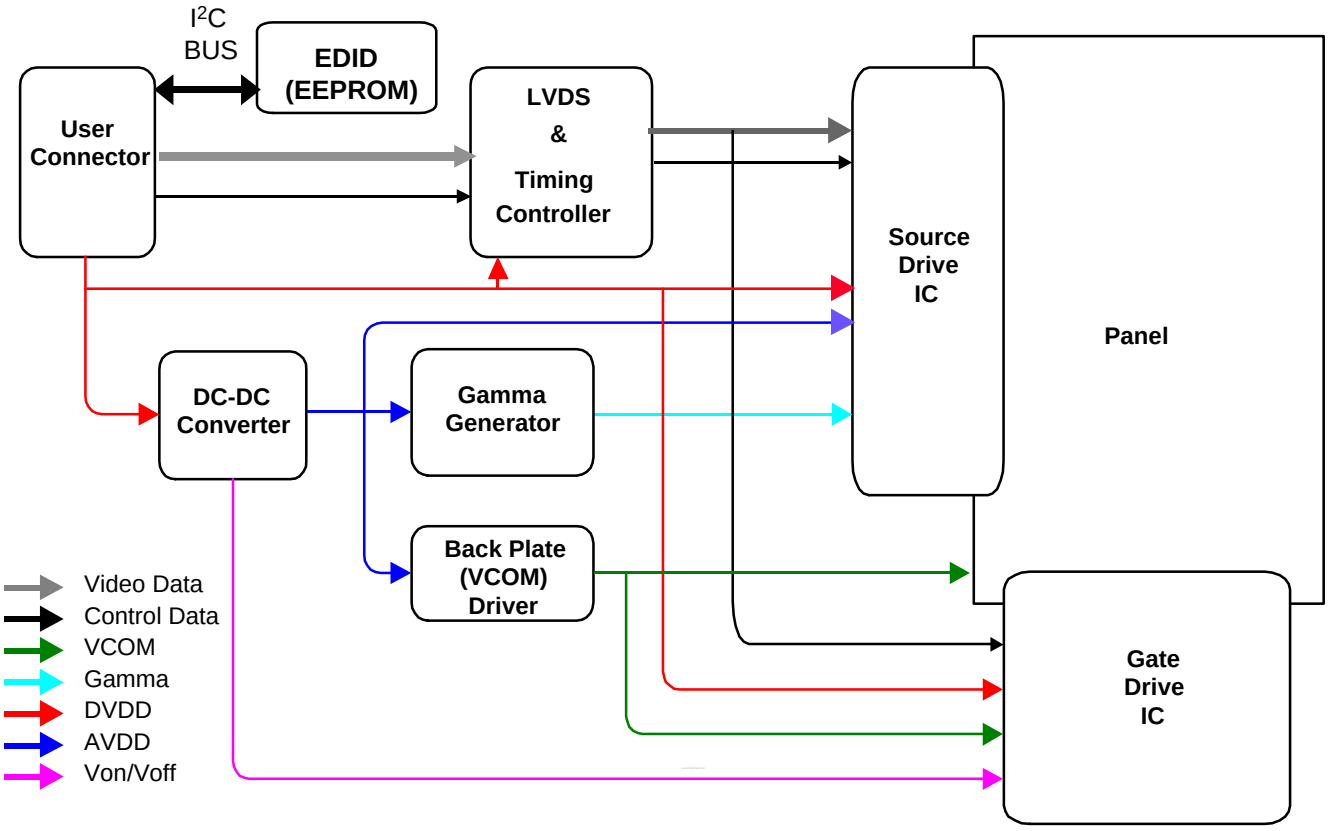
.Reference value of SMB_Data for 3.0mA of Lamp current : **C0H**

If the lamp current is under the 3.0mA, the lamp flicker may happen.

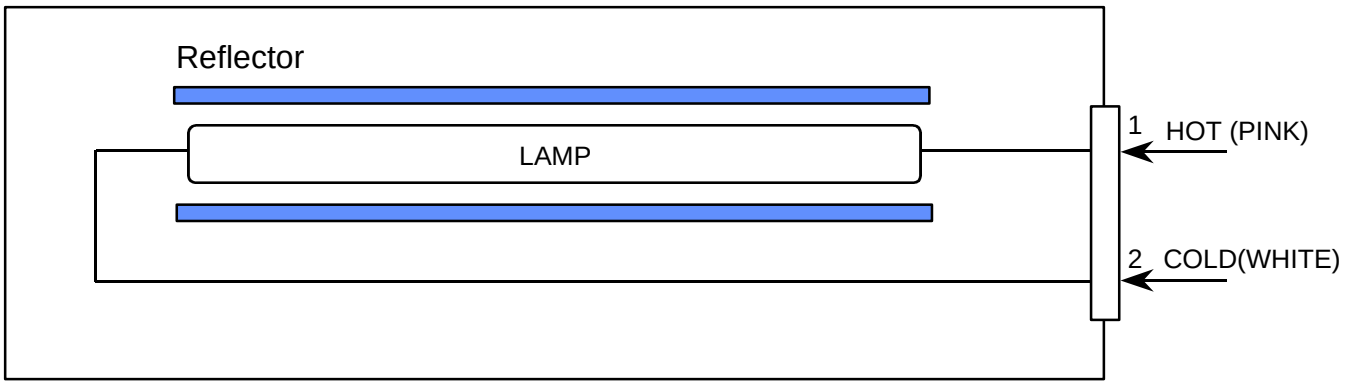
4. BLOCK DIAGRAM

4.1 TFT LCD MODULE

Connector : JAE FI-XB30SR-HF11



4.2 BACKLIGHT UNIT

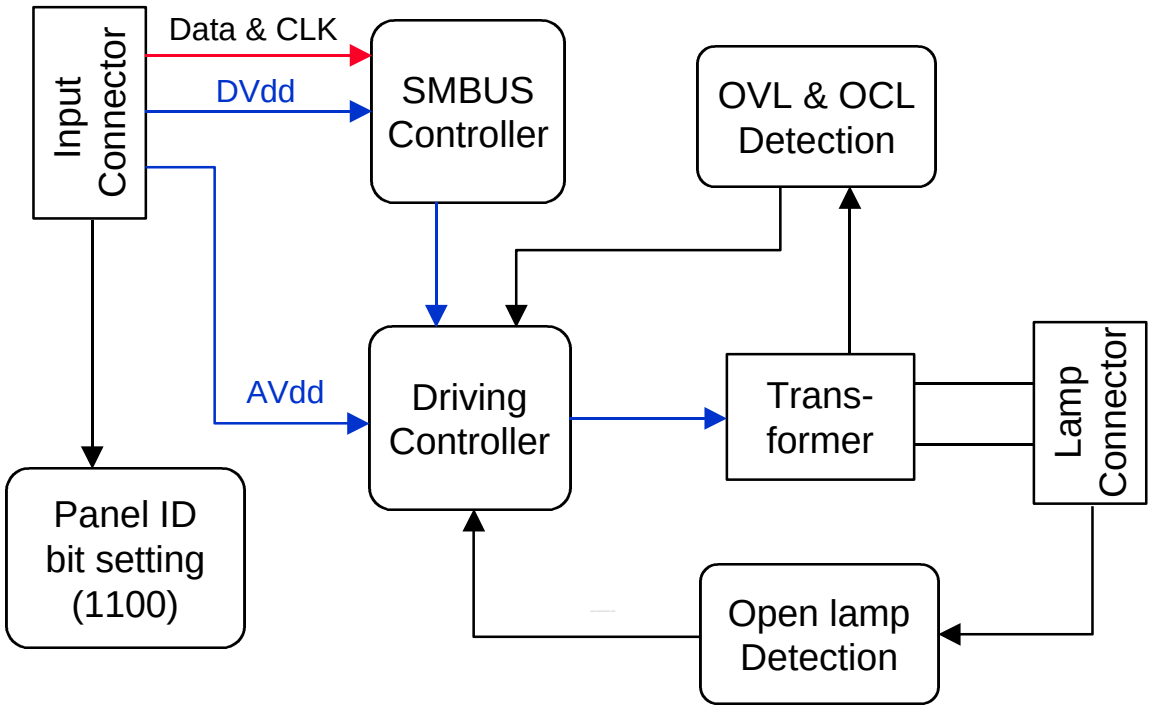


Note) The output of the inverter may change according to the material of the reflector.

4.3 INVERTER

Input Connector : JAE, WR-L16S-VF-1 or JAE, WR-L16S-VF-HD5-1

Lamp Connector : JST, SM02B-BHSS-1-TB



5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (LVDS, Connector : JAE FI-XB30SR-HF10 Mating Connector : JAE FI-X30M)

PIN NO	SYMBOL	FUNCTION	POLARITY	REMARK
1	Vss	Ground		
2	VDD	POWER SUPPLY +3.3V		
3	VDD	POWER SUPPLY +3.3V		
4	VEEDID	DDC 3.3V Power		
5	NC	Reserved for supplier test point		
6	CLKEDID	DDC Clock		
7	DATAEDID	DDC data		
8	O_RxIN0-	LVDS Differential Data INPUT (Odd R0-R5,G0)	Negative	
9	O_RxIN0+	LVDS Differential Data INPUT (Odd R0-R5,G0)	Positive	
10	GND	Ground		
11	O_RxIN1-	LVDS Differential Data INPUT (Odd G1-G5,B0-B1)	Negative	
12	O_RxIN1+	LVDS Differential Data INPUT (Odd G1-G5,B0-B1)	Positive	
13	GND	Ground		
14	O_RxIN2-	LVDS Differential Data INPUT (Odd B1-B5,Sync,DE)	Negative	
15	O_RxIN2+	LVDS Differential Data INPUT (Odd B1-B5,Sync,DE)	Positive	
16	GND	Ground		
17	O_RxCLK-	LVDS Differential Data INPUT (Odd Clock)	Negative	
18	O_RxCLK+	LVDS Differential Data INPUT (Odd Clock)	Positive	
19	GND	Ground		
20	E_RxIN0-	LVDS Differential Data INPUT (Even R0-R5,G0)	Negative	
21	E_RxIN0+	LVDS Differential Data INPUT (Even R0-R5,G0)	Positive	
22	GND	Ground		
23	E_RxIN1-	LVDS Differential Data INPUT (Even G1-G5,B0-B1)	Negative	
24	E_RxIN1+	LVDS Differential Data INPUT (Even G1-G5,B0-B1)	Positive	
25	GND	Ground		
26	E_RxIN2-	LVDS Differential Data INPUT (Even B1-B5,Sync,DE)	Negative	
27	E_RxIN2+	LVDS Differential Data INPUT (Even B1-B5,Sync,DE)	Positive	
28	GND	Ground		
29	E_RxCLK-	LVDS Differential Data INPUT (Even Clock)	Negative	
30	E_RxCLK+	LVDS Differential Data INPUT (Even Clock)	Positive	

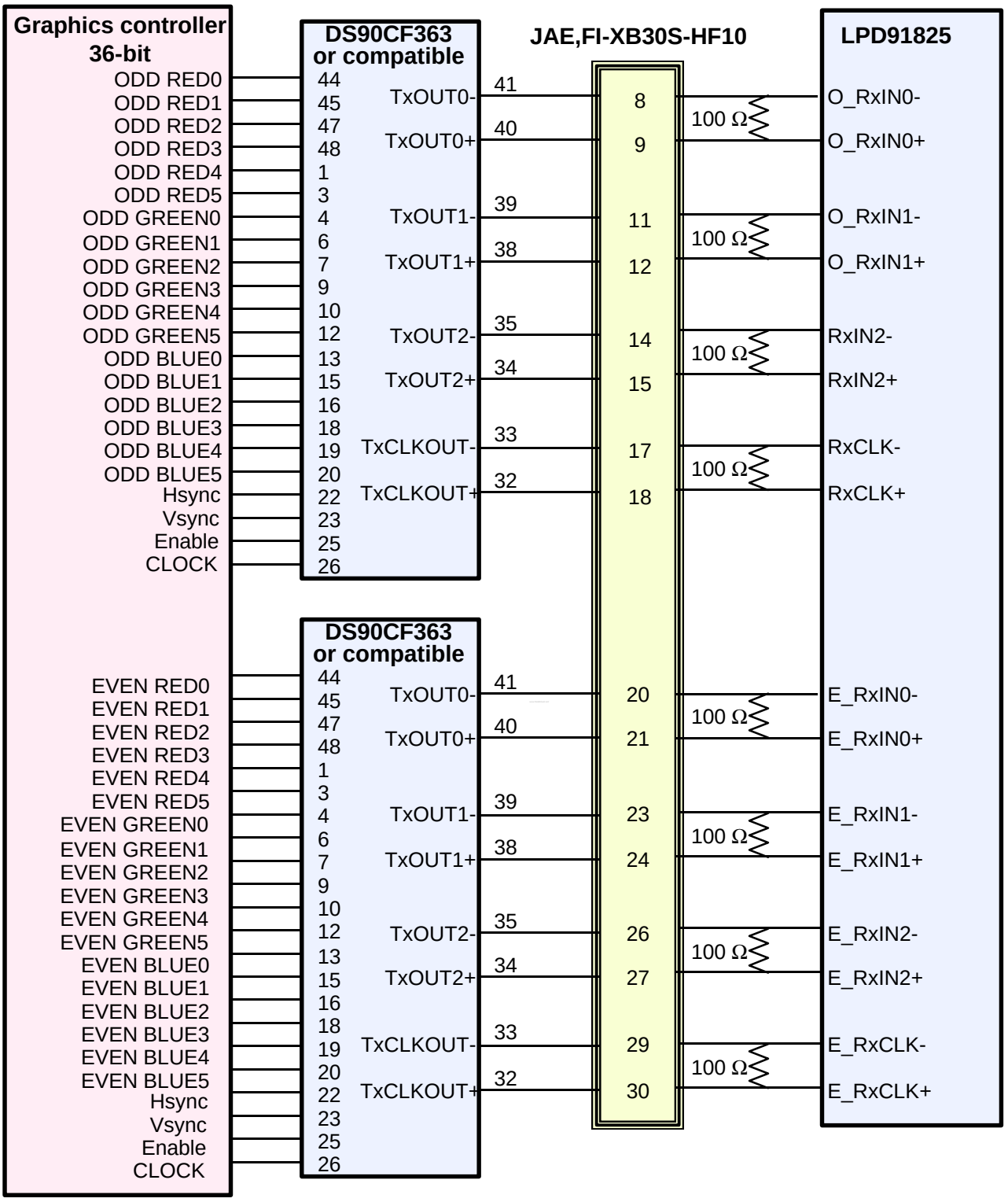
5.2 LVDS Interface : Transmitter DS90CF363 or Compatible

LVDS for Odd pixel

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
44	TxIN0	RO0	12	TxIN11	GO5
45	TxIN1	RO1	13	TxIN12	BO0
47	TxIN2	RO2	15	TxIN13	BO1
48	TxIN3	RO3	16	TxIN14	BO2
1	TxIN4	RO4	18	TxIN15	BO3
3	TxIN5	RO5	19	TxIN16	BO4
4	TxIN6	GO0	20	TxIN17	BO5
6	TxIN7	GO1	22	TxIN18	Hsync
7	TxIN8	GO2	23	TxIN19	Vsync
9	TxIN9	GO3	25	TxIN20	DE
10	TxIN10	GO4	26	TxCLK IN	Clock

LVDS for Even pixel

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
44	TxIN0	RE0	12	TxIN11	GE5
45	TxIN1	RE1	13	TxIN12	BE0
47	TxIN2	RE2	15	TxIN13	BE1
48	TxIN3	RE3	16	TxIN14	BE2
1	TxIN4	RE4	18	TxIN15	BE3
3	TxIN5	RE5	19	TxIN16	BE4
4	TxIN6	GE0	20	TxIN17	BE5
6	TxIN7	GE1	22	TxIN18	Hsync
7	TxIN8	GE2	23	TxIN19	Vsync
9	TxIN9	GE3	25	TxIN20	DE
10	TxIN10	GE4	26	TxCLK IN	Clock



Note : The LCD Module uses a 100ohm resistor between positive and negative lines of each receiver input.

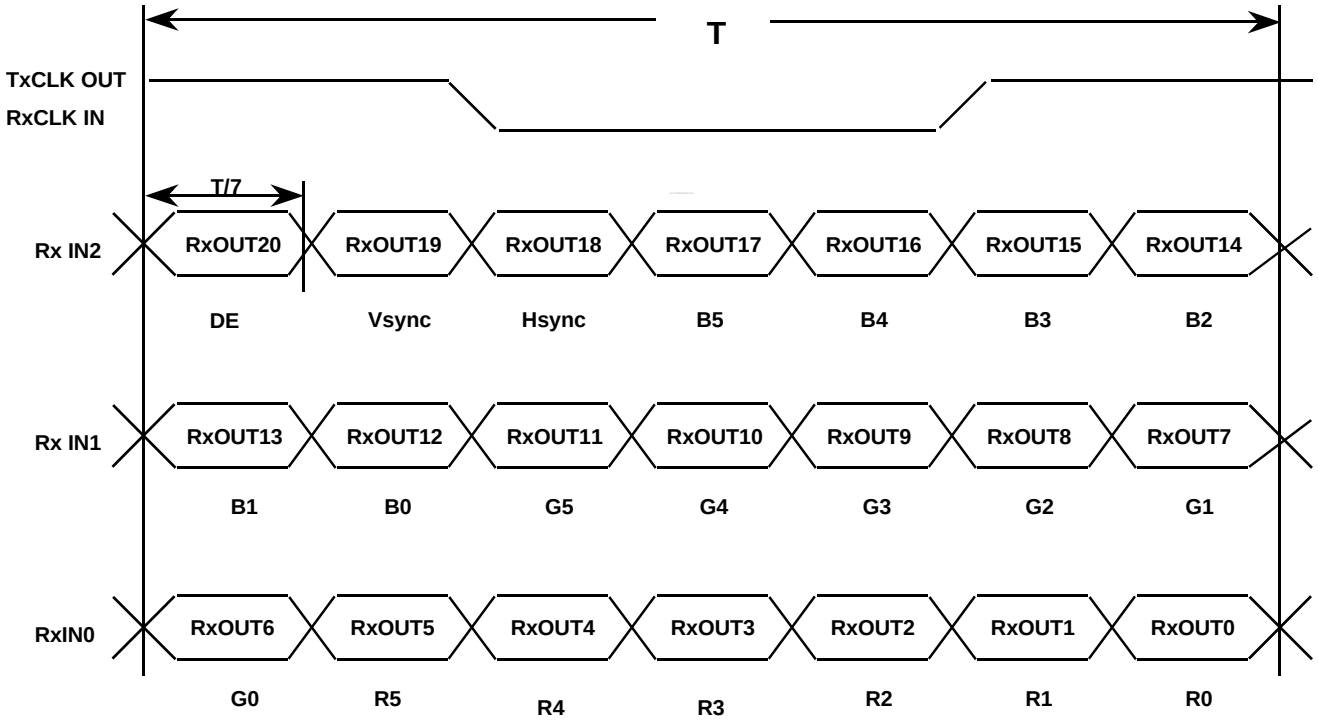
5.3 BACK LIGHT UNIT

Connector : JST BHSR - 02VS -1
Mating Connector : JST SM02B-BHSS-1

Pin NO.	Symbol	Color	Function
1	HOT	PINK	High Voltage
2	COLD	WHITE	Low Voltage

5.4 Timing Diagrams of LVDS For Transmission

LVDS Receiver : LUD98340 or compatible



5.5 INVERTER signals & power

Inverter Connector : JAE, WR-L16S-VF-1

PIN NO	SYMBOL	Voltage	Comments
1	INV_SRC	9.0V to 21V	This power rail should be used as a power rail to drive the back-light DC-AC converter.
2	INV_SRC	9.0V to 21V	This power rail should be used as a power rail to drive the back-light DC-AC converter.
3	GND	0V	Ground
4	INV_SRC	9.0V to 21V	This power rail should be used as a power rail to drive the back-light DC-AC converter.
5	GND	0V	
6	GND	0V	
7	5VSUS	4.85 to 5.2V	This should be used as power source for the control circuitry on the inverter.
8	5VALW	5V	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT.
9	SMB_DAT	-	SMBus interface for sending brightness & contrast information to the inverter/panel
10	SMB_CLK	-	SMBus interface for sending brightness & contrast information to the inverter/panel
11	FPVEE	-	Control signal input into the inverter to turn ON or OFF Lamp. (1 - ON, 0 - OFF)
12	NC	-	
13	PANEL_ID3	-	Output pin, See Note(2)
14	PANEL_ID2	-	Output pin, See Note(2)
15	PANEL_ID1	-	Output pin, See Note(2)
16	PANEL_ID0	-	Output pin, See Note(2)

Note (1) SMBus address Definition

SMBus address definition for brightness & contrast

Inverter SMBus address	A2	A1	A0
Address = 50h	0	0	0

※ Recommend using Dallas Semiconductor DS1803-dual digital potentiometer (or equivalent). Use Wiper '0' for contrast control & Wiper '1' for brightness (backlight) control.

Note (2) Panel ID bit Definition

Panel type	Product ID	ID3	ID2	ID1	ID0
14.1" SXGA+(SPWG) LVDS TFT-LCD	LTN141P2-L01	**1**	**1**	**0**	**0**

5.5 Input Signal,Basic Display Colors and Gray Scale of Each Colors

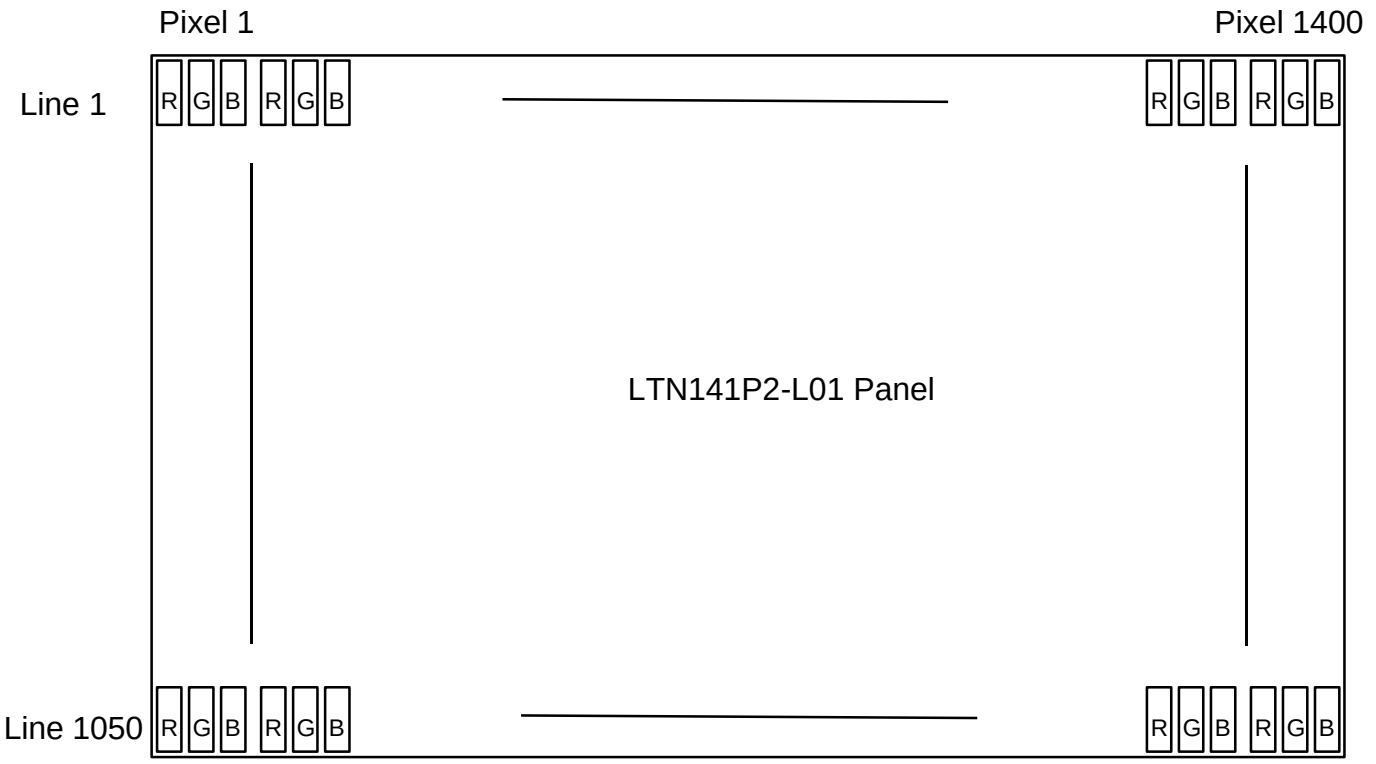
COLOR	DISPLAY	DATA SIGNAL																		GRAY SCALE LEVEL
		RED						GREEN						BLUE						
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5	
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	GREEN	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
	CYAN	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
	RED	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	MAGENTA	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	-
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
GRAY SCALE OF RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	DARK ↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~R60
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓ LIGHT	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
		0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	RED	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
GRAY SCALE OF GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	DARK ↑	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G60
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓ LIGHT	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
		0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	GREEN	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
GRAY SCALE OF BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	DARK ↑	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B60
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓ LIGHT	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

Note

(1) Definition of Gray : Rn : Red Gray, Gn : Green Gray, Bn : Blue Gray (n = Gray level)

(2) Input Signal : 0 = Low level voltage, 1 = High level voltage

5.6 PIXEL FORMAT



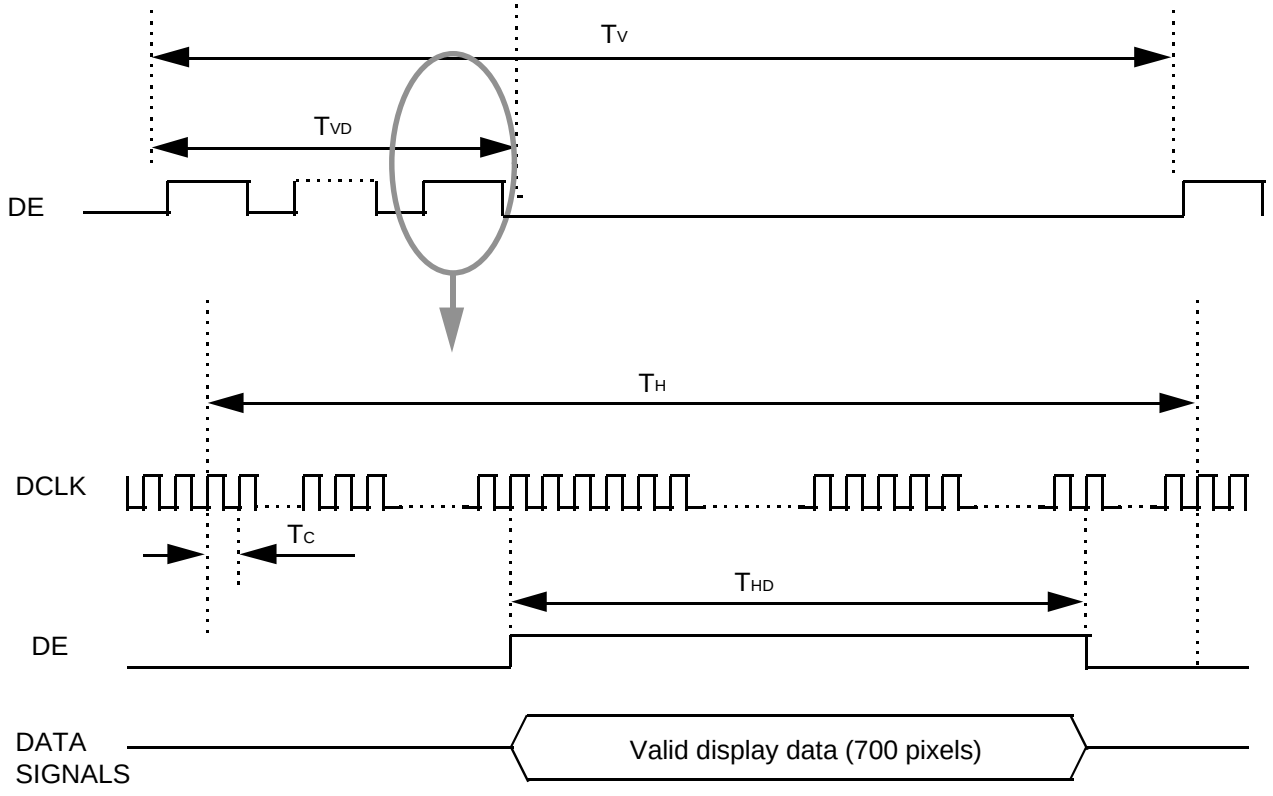
6. INTERFACE TIMING

6.1 Timing Parameters

Signal	Item	Symbol	MIN	TYP	MAX	Unit	Note
Frame Frequency	Cycle	T_V	-	1066	-	lines	
Vertical Active Display Term	Display Period	T_{VD}	-	1050	-	lines	
One Line Scanning Time	Cycle	T_H	-	844	-	clocks	(1)
Horizontal Active Display Term	Display Period	T_{HD}	-	700	-	clocks	

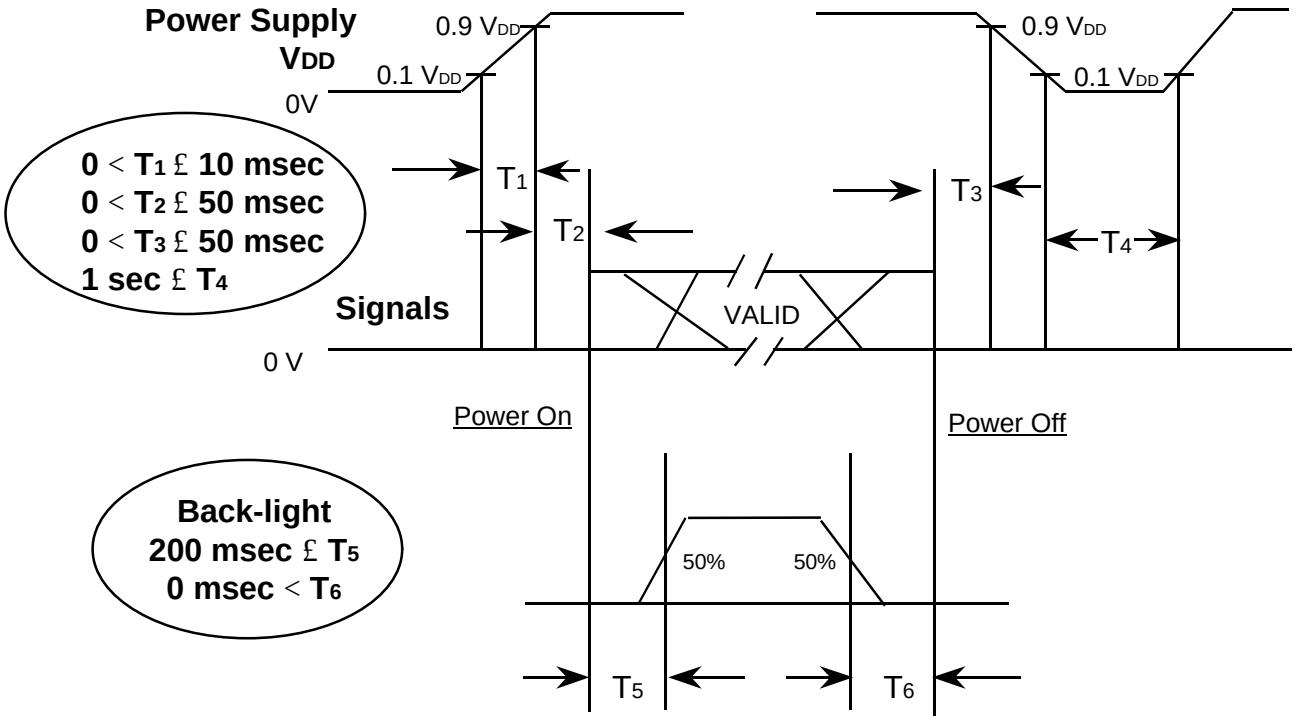
Note (1) The duration of DE [DTMG] signal must be longer than 1 clock period at every horizontal sync. period

6.2 Timing diagrams of interface signal



6.3 Power ON/OFF Sequence

: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

T1 : Vdd rising time from 10% to 90%
T2 : The time from Vdd to valid data at power ON.
T3 : The time from valid data off to Vdd off at power Off.
T4 : Vdd off time for Windows restart
T5 : The time from valid data to B/L enable at power ON.
T6 : The time from valid data off to B/L disable at power Off.

NOTE.

(1) The supply voltage of the external system for the module input should be the same as the definition of V_{DD}.

(2) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become white.

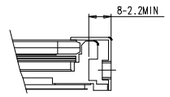
(3) In case of V_{DD} = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

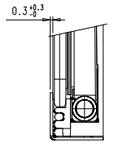
(5) Interface signal shall not be kept at high impedance when the power is on.

FILE NO.

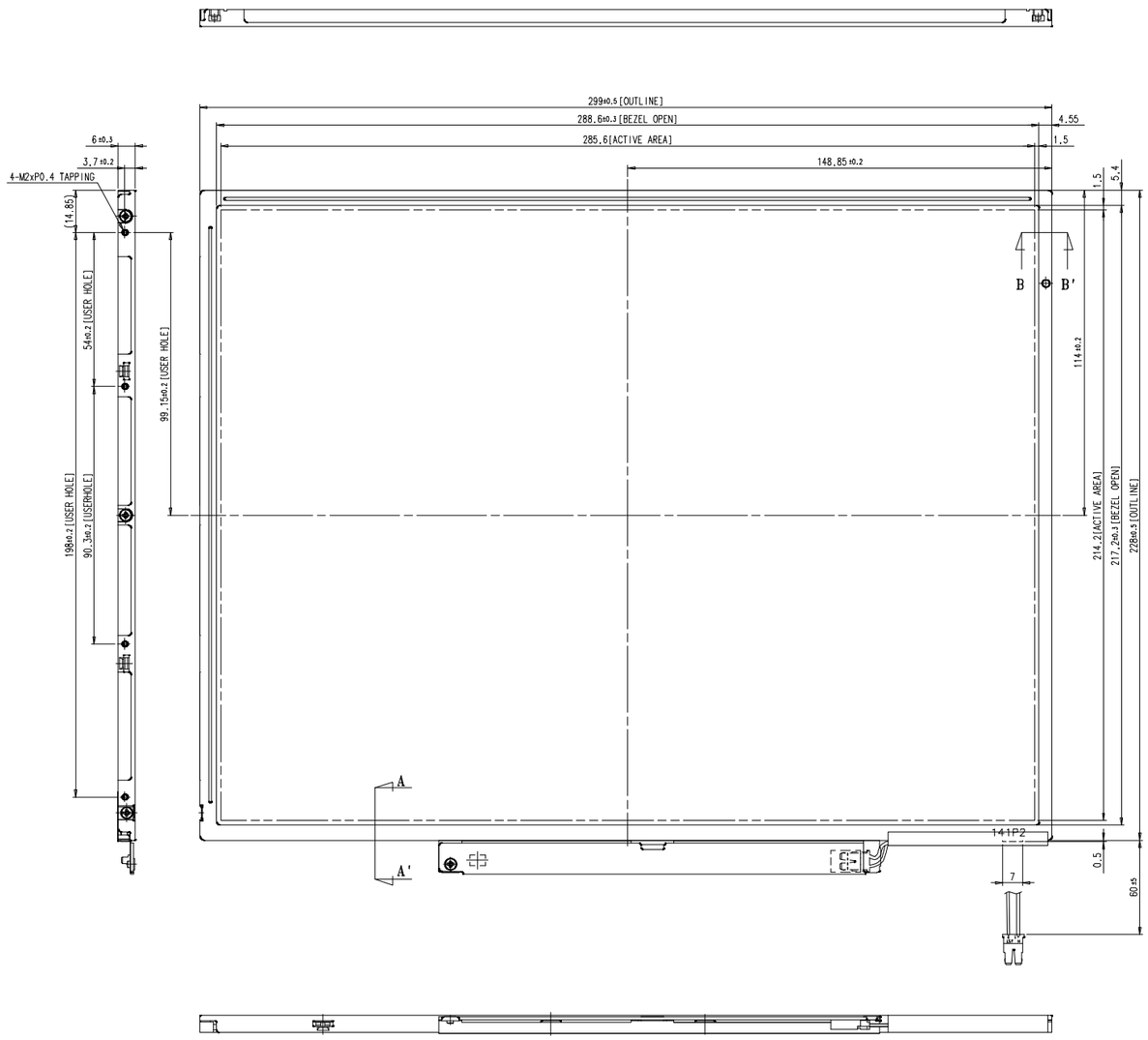
NO	PART NAME	CODE NO	SPECIFICATION	Q'TY	WEIGHT		UNFOLDED DIM. OF. MATERIAL	REMARK
					FINISH	MATERIAL		
	OUTLINE		LTN141P2-L01	1				

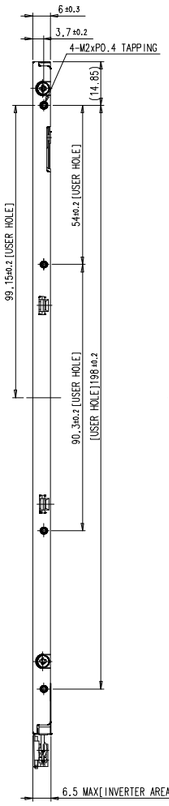


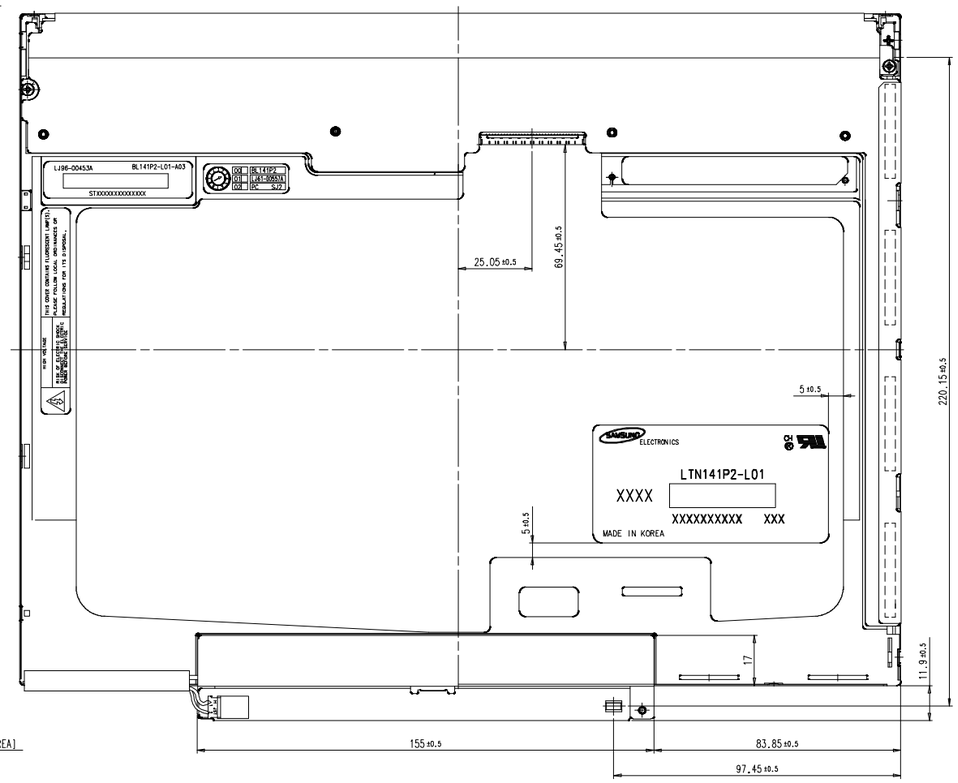
SECTION B-B'(3/1)



SECTION A-A'(3/1)







* NOTE

1. SIGNAL INTERFACE CONNECTOR TO BE SPECIFIED AS BELOW.
   - MAKER : JAE
   - PART NO : F1-XB30S-HF10
2. CCFT CONNECTOR FOR BACKLIGHT TO BE SPECIFIED AS BELOW.
   - MAKER : JST
   - PART NO : BHSR-02VS-1
3. ALLOWED DEPTH OF USERHOLE SCREW INSERTION IS 2.2mm MIN
4. WEIGHT SPEC: 530g±15g

REVISION

GENERAL TOLERANCE			
STEP	LEVEL 1	LEVEL 2	LEVEL 3
0 < X ≤ 4	±0.05	±0.1	±0.2
4 < X ≤ 16	±0.08	±0.15	±0.3
16 < X ≤ 64	±0.12	±0.25	±0.5
64 < X ≤ 256	±0.25	±0.4	±0.8

REV	DATE	DESCRIPTION OF REVISION			
		DRA'N BY	DES'D BY	CHK'D BY	APP'D BY
UNIT	mm				
SCALE	1/1		H.S.CHUN	Y.J.LEE	Y.B.CHU
TOLERANCE					
LEVEL2			2001.05.16	2001.05.17	2001.05.18
SAMSUNG ELECTRONICS					SPEC. NO
					SD04966-000

REASON	CHG'D BY

MODEL NAME	LTN141P2-L01-A03		
PART/SHEET NAME	OUTLINE	SHEET	1/1
CODE NO.		VER.	00

8. PACKING

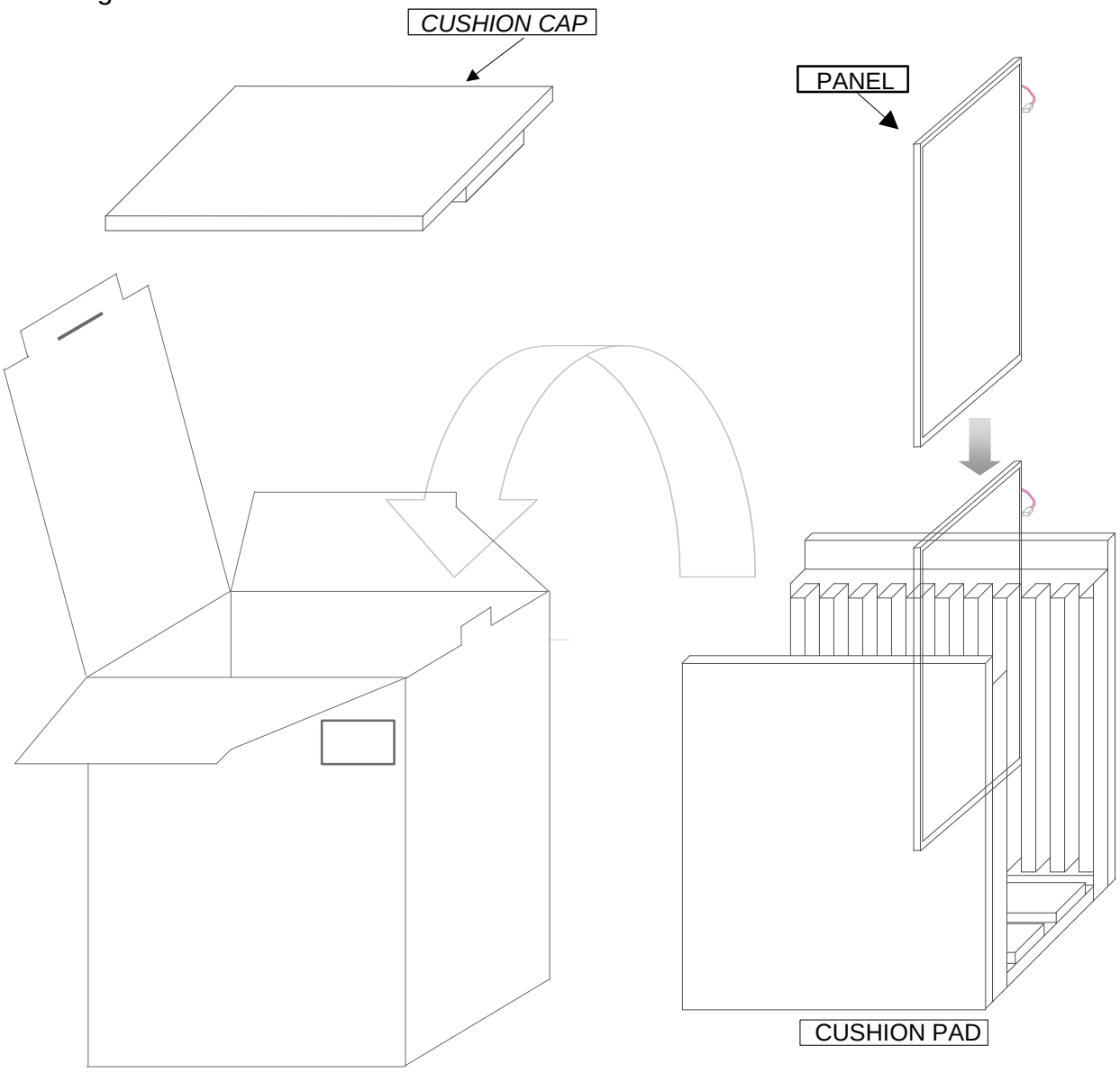
Approval

1. CARTON(Internal Package)

(1) Packing Form

Corrugated Cardboard box and Corrupad form as shock absorber

(2) Packing Method



Note 1)Total Weight : Approximately 8.0 kg

2) Acceptance number of piling : 10 sets

3) Carton size : 317(W)×286(D)×355(H)

4) MAX accumulation quantity : 5 cartons

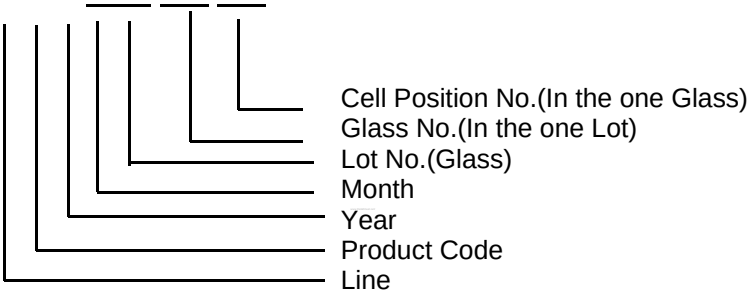
PACKING CASE

No	Part name	Quantity
1	Static electric protective sack	10
2	Packing case(Inner box) included shock absorber	1 set
3	Pictorial marking	2 pics
4	Carton	1 set

9. MARKINGS & OTHERS

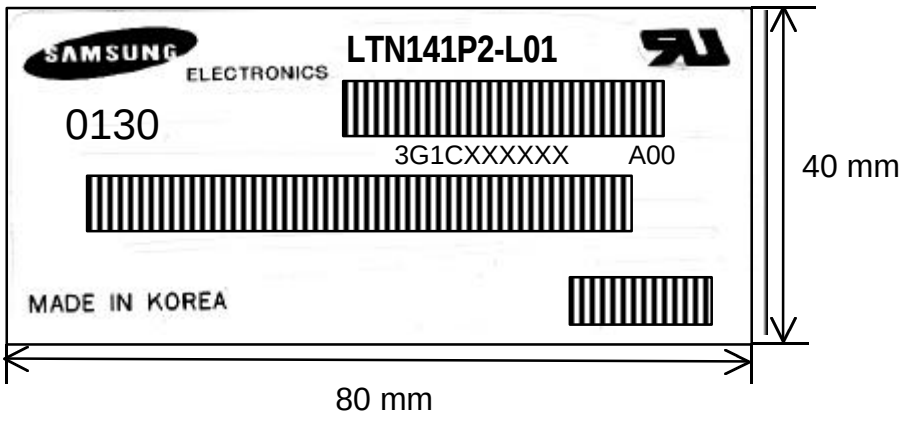
A nameplate bearing followed by is affixed to a shipped product at the specified location on each product.

(1)Parts number : LTN141P2-L01
(2)Revision : One letter
(3)Control code : One letter
(4)Lot number : 3 G 1CXXX XX X



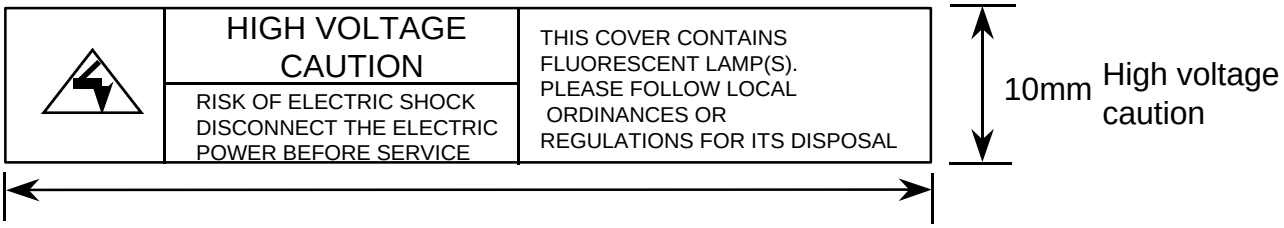
NOTE 1). This code indicating year is omitted in the products of Chun-An site.

(5) Nameplate Indication

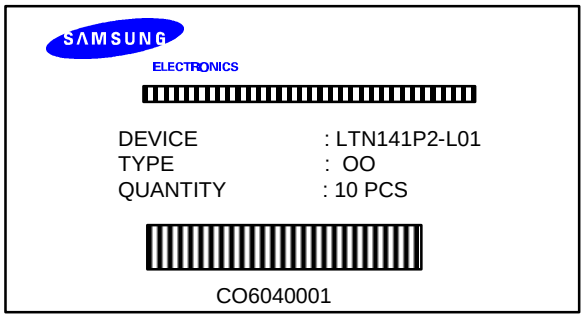


Parts name : LTN141P2 - L01
Lot number : 3G1CXXXXXX
Inspected work week : 0130

High voltage caution label



(6) Packing box attach



(7) Packing box Marking : Samsung TFT-LCD Brand Name

10. GENERAL PRECAUTIONS

Approval

1. Handling

(a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.

(b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and CCFT back-light.

(c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.

(d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(f) The desirable cleaners are water, IPA(Isoprophyl Alcohol) or Hexane.
Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth . In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(h) Protect the module from static , it may cause damage to the C-MOS Gate Array IC.

(i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(j) Do not disassemble the module.

(k) Do not pull or fold the lamp wire.

(l) Do not adjust the variable resistor which is located on the back side.

(m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(n) Pins of I/F connector shall not be touched directly with bare hands.

2. STORAGE

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%.

(b) Do not store the TFT-LCD module in direct sunlight.

(c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

3. OPERATION

(a) Do not connect,disconnect the module in the " Power On" condition.

(b) Power supply should always be turned on/off by following item 6.3 " Power on/off sequence ".

(c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(d) The cable between the back-light connector and its inverter power supply shall be a minimized length and be connected directly . The longer cable between the back-light and the inverter may cause lower luminance of lamp(CCFT) and may require higher startup voltage(Vs).

4. OTHERS

(a) Ultra-violet ray filter is necessary for outdoor operation.

(b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.

(d) If the module displays the same pattern continuously for a long period of time,it can be the situation when the image "sticks" to the screen.

(e) This module has its circuitry PCB' s on the rear side and should be handled carefully in order not to be stressed.