

SAMSUNG**ELECTRONICS**

Approval



TO : DELL

DATE : September. 10. 2008

SAMSUNG TFT-LCD**MODEL NO : LTN160HT02-0**

NOTE : Extension code [-0]
 → LTN160HT02-0
 Surface type [Anti-Glare]

The information described in this SPEC is preliminary and can be changed without prior notice.

APPROVED BY :

K. H. Shin

PREPARED BY :

LCD Application Engineering Part (Mobile)

SAMSUNG ELECTRONICS CO., LTD.**Samsung Secret**

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REVISION HISTORY

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Date	Revision No.	Page	Summary
Jan.4. 2008	P00	All	LTN160HT02-0 model spec was issued first.
Mar. 14. 2008	P01	All	LTN160HT02-0 model spec was updated for RGBLED configuration
Mar. 18. 2008	P02	7, 14 17	Typos are corrected
Jun. 04. 2008	P03	7	Gray to gray response time is updated
Sep. 10. 2008	A00	All	Approval spec was released

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GENERAL DESCRIPTION

DESCRIPTION

LTN160HT02-0 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight system. The resolution of a 16.0" contains 1920 x 1080 pixels and can display up to 262,144 colors. 6 O'clock direction is the Optimum viewing angle.

FEATURES

- Thin and light weight
- High contrast ratio, high aperture structure
- 1920 x 1080 pixels resolution (16:9)
- Fast Response Time
- Low power consumption
- RGB LED BLU Structure
- DE (Data enable) only mode
- 3.3V LVDS Interface
- On board EDID chip
- Pb-free product
- True 8 bit color data
- Multimedia T-CON

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	353.28 (H) x 198.72(V) (16.0" diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	262,144		
Number of pixel	1920 x 1080	pixel	16 : 9
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.184 (H) x 0.184 (V) (TYP.)	mm	
Display Mode	Normally white		
Surface treatment	Haze 40, Hardness 3H		Anti-Glare

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Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal (H)	364.5	365	365.5	mm	
	Vertical (V)	216.5	217	217.5	mm	
	Depth (D)	-	-	6.0	mm	(1)
Weight		-	-	580	g	

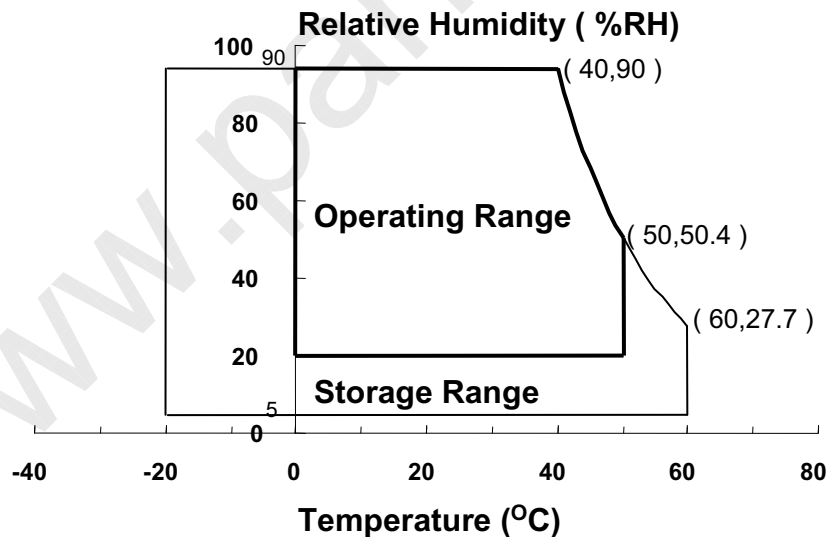
Note (1) Measurement condition of outline dimension
 . Equipment : Vernier Calipers
 . Push Force : 500g · f (minimum)

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	60	°C	(1)
Operating temperate (Temperature of glass surface)	TOPR	0	50	°C	(1)
Shock (non-operating)	Snop	-	240	G	(2),(4)
Vibration (non-operating)	Vnop	-	2.41	G	(3),(4)

Note (1) Temperature and relative humidity range are shown in the figure below.
 95 % RH Max. ($40\text{ }^{\circ}\text{C} \geq T_a$)
 Maximum wet - bulb temperature at $39\text{ }^{\circ}\text{C}$ or less. ($T_a > 40\text{ }^{\circ}\text{C}$) No condensation



- (2) 2ms, half sine wave, one time for $\pm X, \pm Y, \pm Z$.
 (3) 5 - 500 Hz, random vibration, 30min for X, Y, Z.
 (4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.

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1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

 $V_{DD} = 3.3V, V_{SS} = GND = 0V$

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V	(1)
Logic Input Voltage	V_{DD}	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V	(1)

Note (1) Within T_a ($25 \pm 2 \text{ }^\circ\text{C}$)

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2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5).
Measuring equipment : TOPCON SR-3

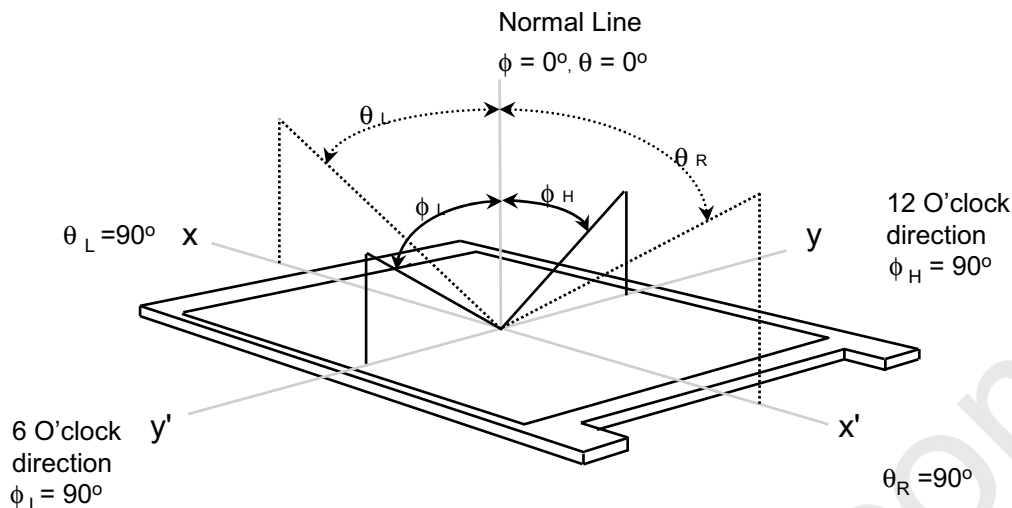
* Ta = 25 ± 2 °C, V_{DD}=3.3V, fv= 60Hz, f_{DCLK} = 153.49 MHz, I_L = 20mA

Item	Symbol	Condition	Min.	Typ.	Max	Unit	Note	
Contrast Ratio (5 Points)	CR	Normal Viewing Angle $\phi = 0$ $\theta = 0$	300	500	-	-	(1), (2), (5)	
Response Time at Ta (Rising + Falling)	T _{RT}		-	8	16	msec	(1), (3)	
Response Time at Ta (Gray 32 to 47)	T _{RT}		-	8	16			
Average Luminance of White (5 Points)	Y _{L,AVE}		250	300	-	cd/m ²	I _L =20mA (1), (4)	
Color Chromaticity (CIE)	Red		R _X	0.675	0.695	0.715	-	
			R _Y	0.280	0.300	0.320		
	Green		G _X	0.150	0.170	0.190		
			G _Y	0.695	0.715	0.735		
	Blue		B _X	0.125	0.145	0.165		
			B _Y	0.045	0.065	0.085		
	White		W _X	0.293	0.313	0.333		
			W _Y	0.309	0.329	0.349		
Viewing Angle	Hor.		θ_L	65	75	-	Degrees	(1), (5) SR-3
		θ_R	65	75	-			
	Ver.	ϕ_H	45	50	-			
		ϕ_L	45	50	-			
Viewing Angle	Hor.	θ_L	30	-	-	Degrees	(1), (5) SR-3	
		θ_R	30	-	-			
	Ver.	ϕ_H	10	-	-			
		ϕ_L	20	-	-			
Color Gamut		-	100	-	%	Adobe		
13 Points White Variation	δ_L		-	-	1.7	-	(6)	

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Note 1) Definition of Viewing Angle : Viewing angle range($10 \leq C/R$)

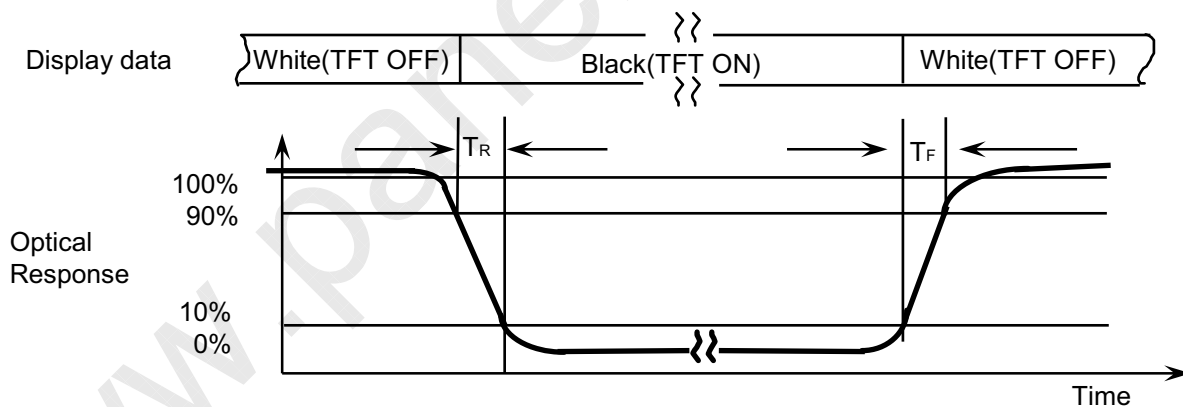


Note 2) Definition of Contrast Ratio (CR) : Ratio of gray max (Gmax) ,gray min (Gmin) at 5 points(4, 5, 7, 9, 10)

$$CR = \frac{CR(4) + CR(5) + CR(7) + CR(9) + CR(10)}{5}$$

Points : (4) , (5) , (7) , (9) , (10) at the figure of Note (6).

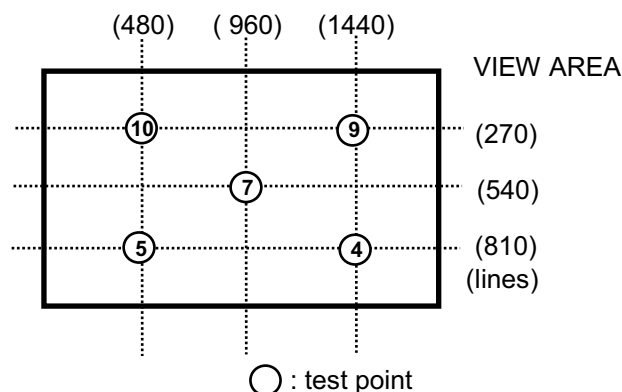
Note 3) Definition of Response time :



Note 4) Definition of Average Luminance of White : measure the luminance of white at 5 points.

Average Luminance of White ($Y_{L,AVE}$)

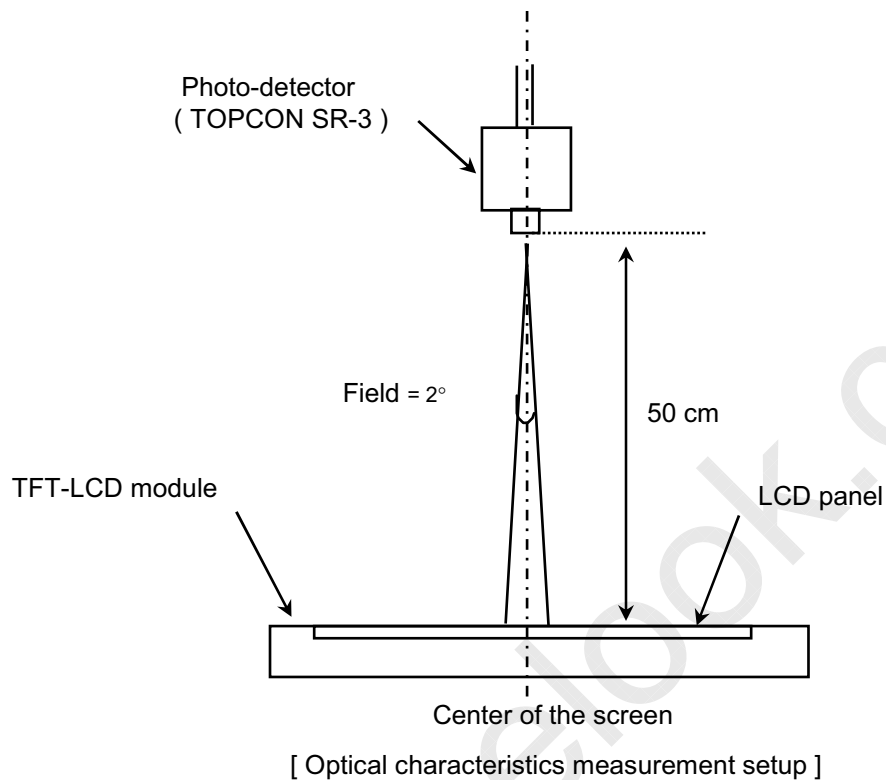
$$Y_{L,AVE} = \frac{Y_{L4} + Y_{L5} + Y_{L7} + Y_{L9} + Y_{L10}}{5}$$



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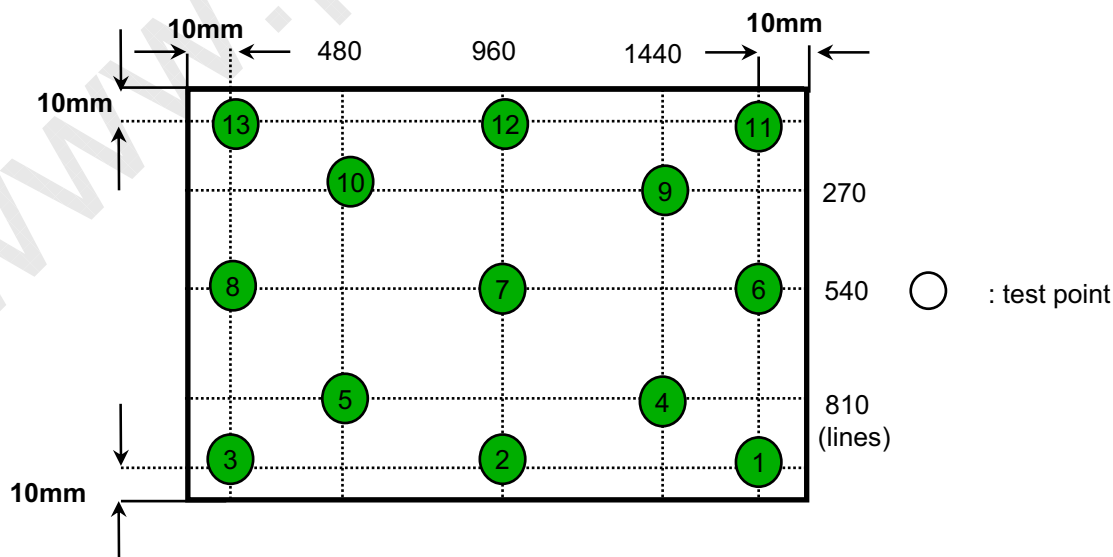
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Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 min , the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. 30 min after lighting the backlight. This should be measured in the center of screen.
 LED current : 20.0mA
 Environment condition : Ta = 25 ± 2 °C



Note 6) Definition of 13 points white variation (δL), [① ~ ⑬]

$$\delta L = \frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}}$$



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3. ELECTRICAL CHARACTERISTICS

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3.1 TFT LCD MODULE

Ta= 25 ± 2°C

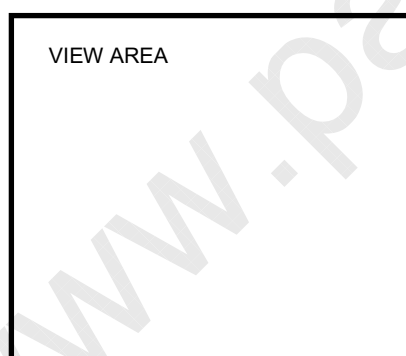
Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Voltage of Power Supply	V _{DD}	3.0	3.3	3.6	V		
Differential Input Voltage for LVDS Receiver Threshold	High	V _{IH}	-	-	+100	mV	V _{CM} = +1.2V
	Low	V _{IL}	-100	-	-	mV	
Vsync Frequency	f _v	-	60	-	Hz		
Hsync Frequency	f _H	-	67.32	-	KHz		
Main Frequency	f _{DCLK}	-	153.49	-	MHz		
Rush Current	I _{RUSH}	-	-	2.5	A	(4)	
Current of Power Supply	White	I _{DD}	-	600	-	mA	(2),(3)*a
	Mosaic		-	750	-	mA	(2),(3)*b
	V. Stripe		-	800	900	mA	(2),(3)*c

Note (1) Display data pins and timing signal pins should be connected.(GND = 0V)

(2) f_v = 60Hz, f_{DCLK} = 153.49 MHz, V_{DD} = 3.3V, DC Current.

(3) Power dissipation pattern

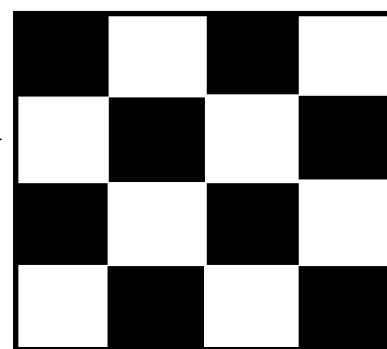
*a) White Pattern



*b) Mosaic Pattern

Display Brightest Gray Level →

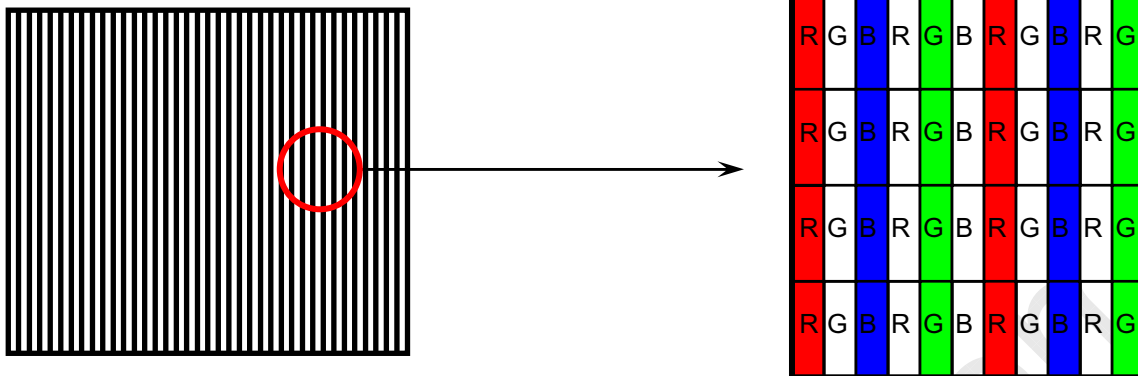
Display Darkest Gray Level →



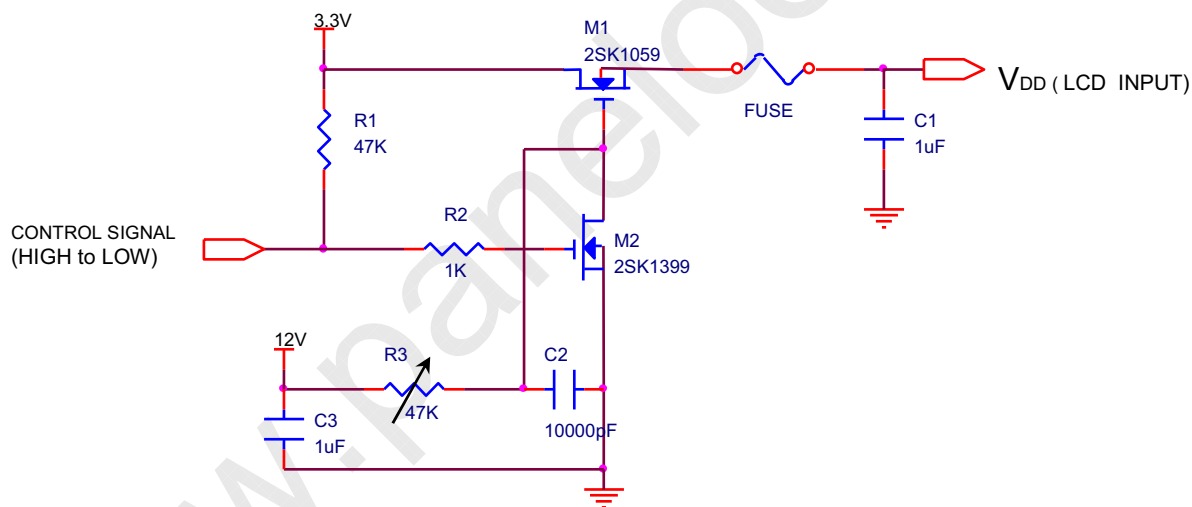
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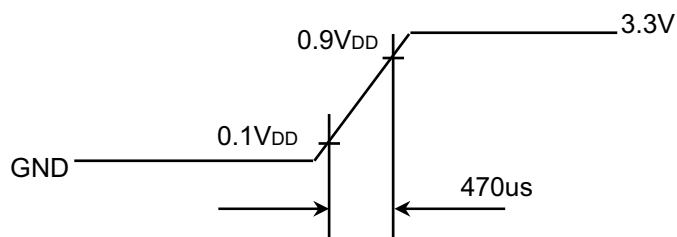
*c) 1dot Vertical stripe pattern



4) Rush current measurement condition



V_{DD} rising time is 470us



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3.2 BACK-LIGHT UNIT

Ta= 25 ± 2 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED Forward Current	Ir	-	0.027	0.030	A	-
	Ig	-	0.035	0.060	A	-
	Ib	-	0.019	0.030	A	-
LED Forward Voltage	Vfr	-	2.2	2.4	V	-
	Vfg		3.3	3.6	V	-
	Vfb		3.3	3.4	V	-
LED Array Voltage	Vpr	-	17.6	19.2	V	Vf * 8LED
	Vpg		26.4	28.8	V	-
	Vpb		26.4	27.2	V	-
Power Consumption	P	-	11.4048	18.72	W	((Ir X Vpr)+(Ig X Vpg)+(Ib X Vpb)) X 6

3.3 LED Driver

- LED Driver Manufacturer : LP8540(National Semiconductor)

Ta= 25 ± 2 °C

Symbol	Item	Min.	Typ.	Max.	Unit	Note
VIN	Input Voltage	8	12	20	V	
IIN	Normal mode supply Current	-	5	-	mA	
VLDO	Internal LDO Voltage	4.5	5.0	5.5	V	
ILDO	Internal LDO External loading			5.0	mA	
PIN	Input Power		0.06		W	
f SW	Switching Frequency		1.25		MHz	
fLED	LED Switching Frequency		0.20 0.54 2.44 19.5		MHz	PWM_FREQ<0:1> = 00b PWM_FREQ<0:1> = 01b PWM_FREQ<0:1> = 10b PWM_FREQ<0:1> = 11b
f SW	Switching Frequency		1.25		MHz	
FPWM	PWM frequency range	0.2		25	kHz	
ILOAD	Maximum Continuous Load Current	400 210		-	mA	10.0V ≤ VIN, VOUT = 40V 6.0V ≤ VIN, VOUT = 40V

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5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (LVDS, Connector : JAE FI-VHP50S-A-HF11)

Pin	Signal	Description
1	Test Loop	Test Loop (only to pin 30)
2	VEEDID	EDID 3.3V power
3	VSS	Ground (Panel logic, BL logic)
4	CLK EEDID	EDID clock
5	DATA EEDID	EDID data
6	VSS	Ground (Panel logic, BL logic)
7	Odd_Rin0-	- LVDS differential data input (R0-R5, G0)
8	Odd_Rin0+	+ LVDS differential data input (R0-R5, G0)
9	VSS1	Ground – Shield LVDS Ch1
10	Odd_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels)
11	Odd_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels)
12	VSS2	Ground – Shield LVDS Ch2
13	Odd_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
14	Odd_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
15	VSS3	Ground – Shield LVDS Ch3
16	Odd_ClkIN-	- LVDS differential clock input (odd pixels)
17	Odd_ClkIN+	+ LVDS differential clock input (odd pixels)
18	VSS4	Ground – Shield LVDS Ch4
19	Even_Rin0-	- LVDS differential data input (R0-R5, G0) (even pixels)
20	Even_Rin0+	+ LVDS differential data input (R0-R5, G0) (even pixels)
21	VSS5	Ground – Shield LVDS Ch5
22	Even_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (even pixels)
23	Even_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (even pixels)
24	VSS6	Ground – Shield LVDS Ch6
25	Even_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)

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5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (LVDS, Connector : JAE FI-VHP50S-A-HF11)

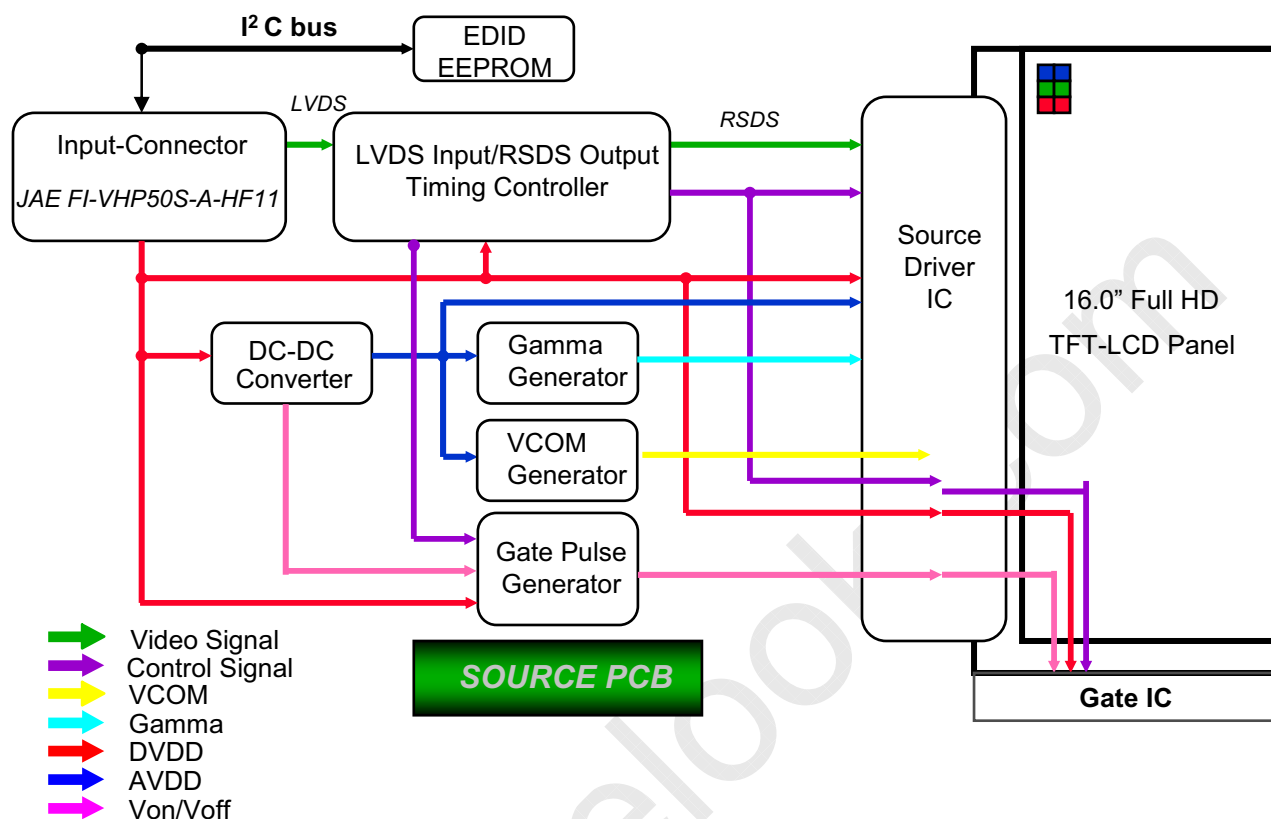
Pin	Signal	Description
26	Even_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
27	VSS7	Ground – Shield LVDS Ch7
28	Even_CkIN-	- LVDS differential clock input (even pixels)
29	Even_CkIN+	+ LVDS differential clock input (even pixels)
30	Test Loop	Test Loop (only to pin 1)
31	CONNTST	Connector test (this pin connected to pin 50 only)
32~33	VDD	Logic power 3.3V (Panel logic, BL logic)
34	TEST (BIST_EN)	Panel Self Test
35	+5V_ALW	
36~37	VSS	
38	PWM_BL	PWM brightness control
39~42	VBL-	LED power return
43	NC	no connect
44~47	VBL+	7V - 20V LED power
48	SMB_DATA	SMBus Data
49	SMB_CLK	SMBus Clk
50	CONNTST	Connector test (this pin to be connected to pin 31 only)

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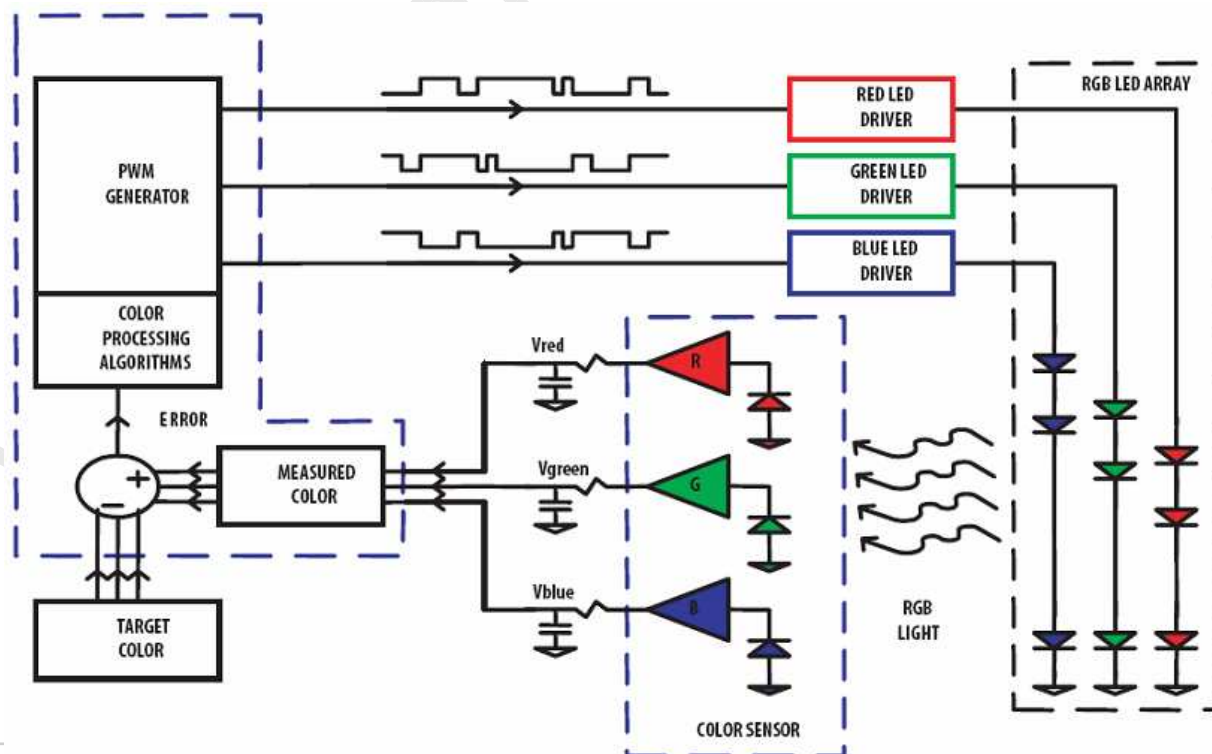
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4. BLOCK DIAGRAM

4.1 TFT LCD Module



4.2 LED Backlight Unit



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5.2 LVDS Interface : Transmitter DS90CF365 or Compatible

LVDS for Odd pixel

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
44	TxIN0	RO0	12	TxIN11	GO5
45	TxIN1	RO1	13	TxIN12	BO0
47	TxIN2	RO2	15	TxIN13	BO1
48	TxIN3	RO3	16	TxIN14	BO2
1	TxIN4	RO4	18	TxIN15	BO3
3	TxIN5	RO5	19	TxIN16	BO4
4	TxIN6	GO0	20	TxIN17	BO5
6	TxIN7	GO1	22	TxIN18	Hsync
7	TxIN8	GO2	23	TxIN19	Vsync
9	TxIN9	GO3	25	TxIN20	DE
10	TxIN10	GO4	26	TxCLK IN	Clock

LVDS for Even pixel

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
44	TxIN0	RE0	12	TxIN11	GE5
45	TxIN1	RE1	13	TxIN12	BE0
47	TxIN2	RE2	15	TxIN13	BE1
48	TxIN3	RE3	16	TxIN14	BE2
1	TxIN4	RE4	18	TxIN15	BE3
3	TxIN5	RE5	19	TxIN16	BE4
4	TxIN6	GE0	20	TxIN17	BE5
6	TxIN7	GE1	22	TxIN18	N/C
7	TxIN8	GE2	23	TxIN19	N/C
9	TxIN9	GE3	25	TxIN20	N/C
10	TxIN10	GE4	26	TxCLK IN	Clock

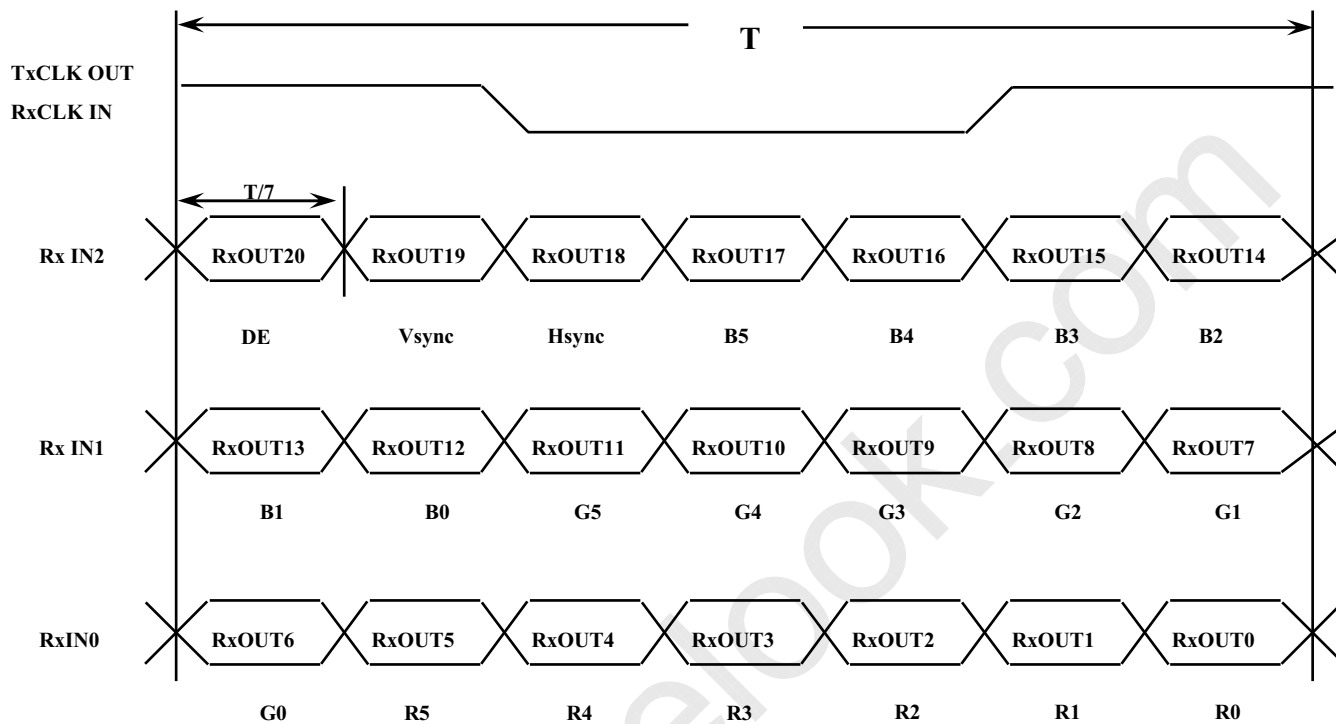
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5.3 Timing Diagrams of LVDS For Transmission

LVDS Receiver : Integrated T-CON

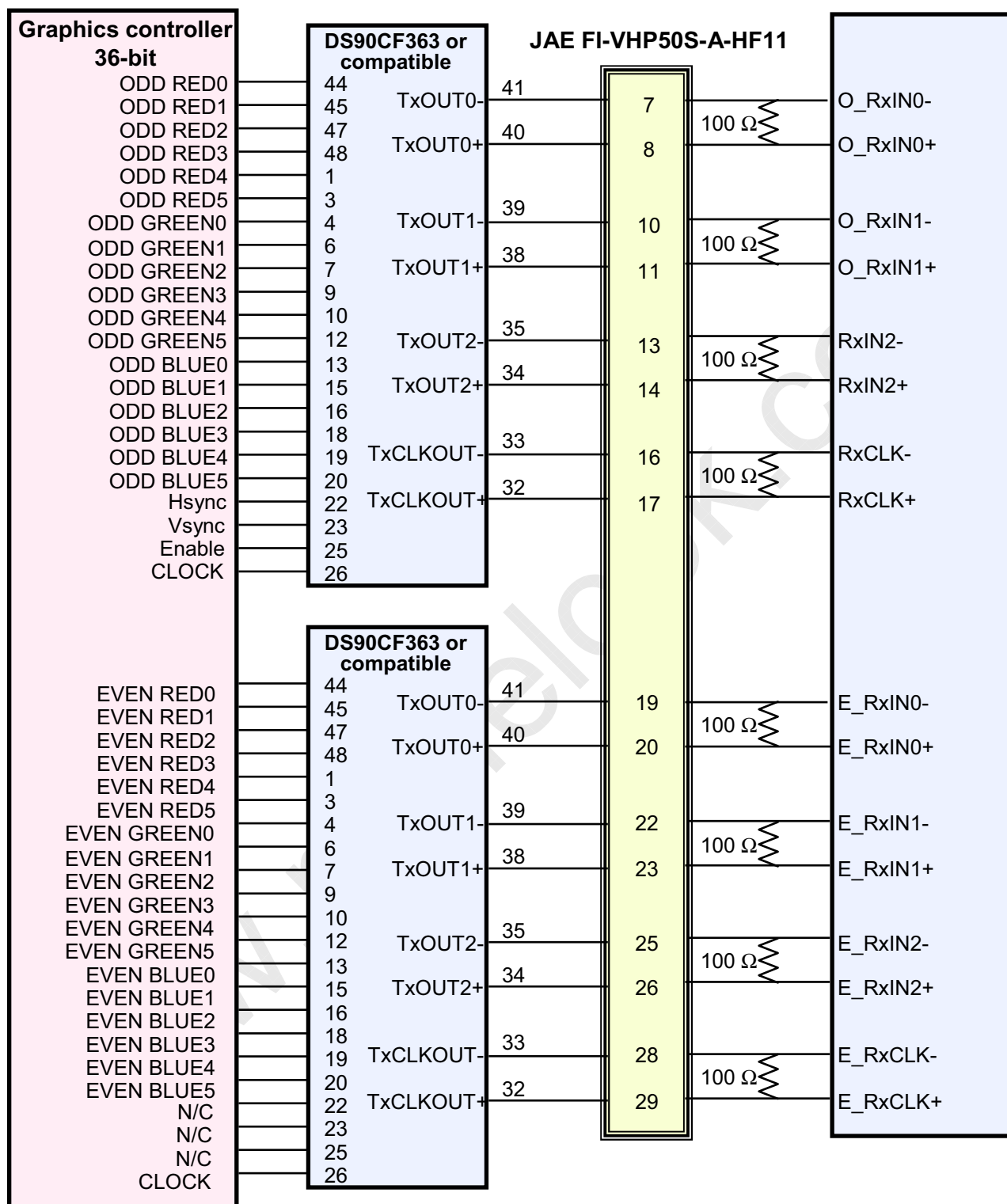


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LVDS Interface



Note : The LCD Module uses a 100ohm resistor between positive and negative lines of each receiver input.

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5.4 Input Signals, Basic Display Colors and Gray Scale of Each Color

Color	Display	Data Signal																Gray Scale Level	
		Red					Green					Blue							
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3		B4
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	-
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	-
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	-
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
Gray Scale Of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3-R60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R61
	Light	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R62
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R63
Gray Scale Of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	G2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3-G60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	G62
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	G63
Gray Scale Of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	B2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3-B60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	B61
	Light	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	B62
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B63

Note 1) Definition of gray :

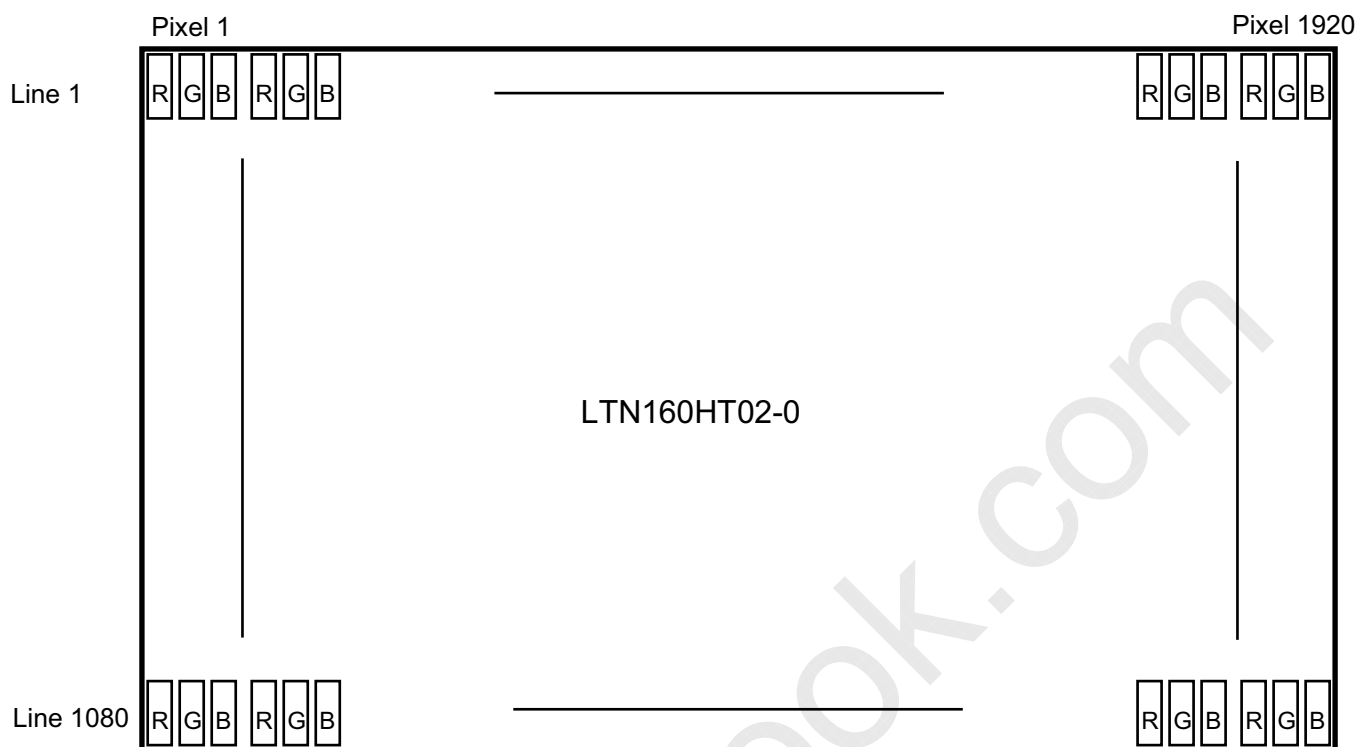
Rn: Red gray, Gn: Green gray, Bn: Blue gray (n=gray level)

Note 2) Input signal: 0 =Low level voltage, 1=High level voltage

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5.5 Pixel Format in the display



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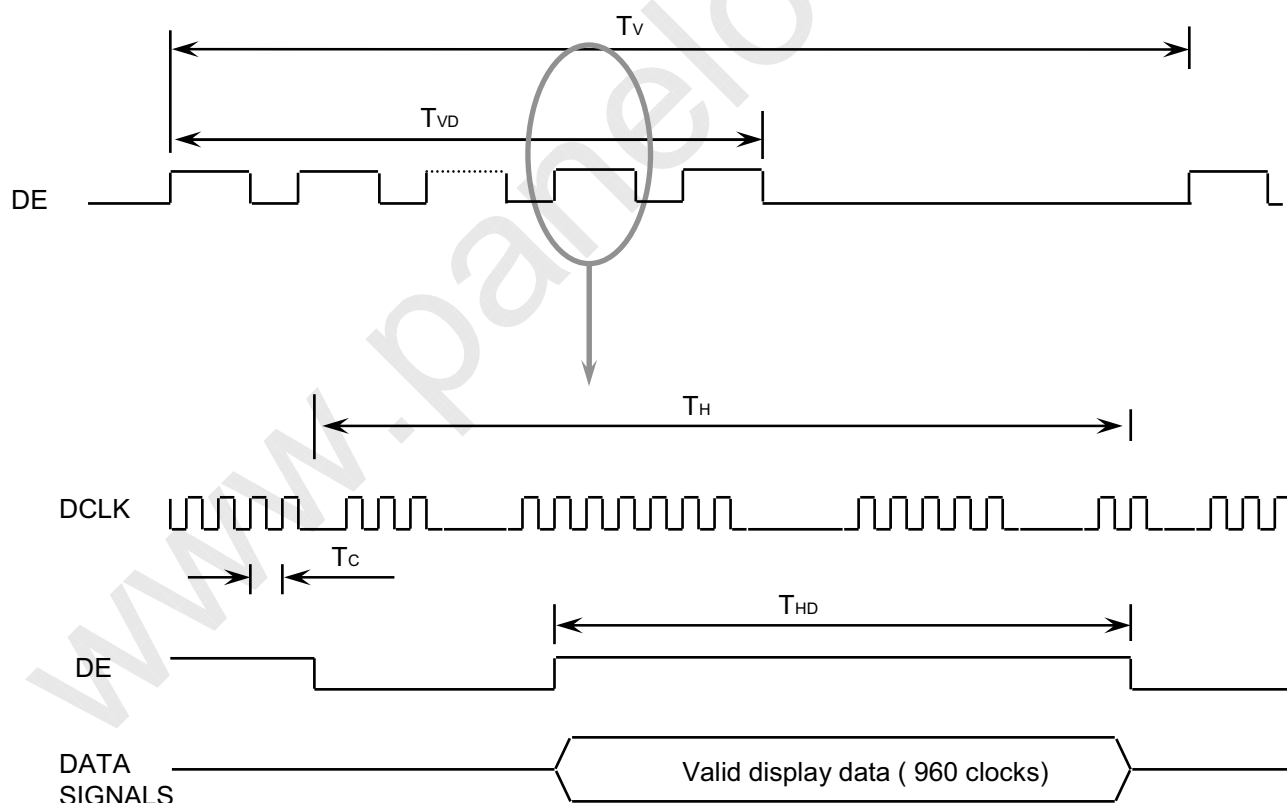
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6. INTERFACE TIMING

6.1 Timing Parameters

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frame Frequency	Cycle	TV	-	1111	-	Lines	-
Vertical Active Display Term	Display Period	TVD	-	1080	-	Lines	-
One Line Scanning Time	Cycle	TH	-	1040	-	Clocks	-
Horizontal Active Display Term	Display Period	THD	-	960	-	Clocks	-

6.2 Timing diagrams of interface signal



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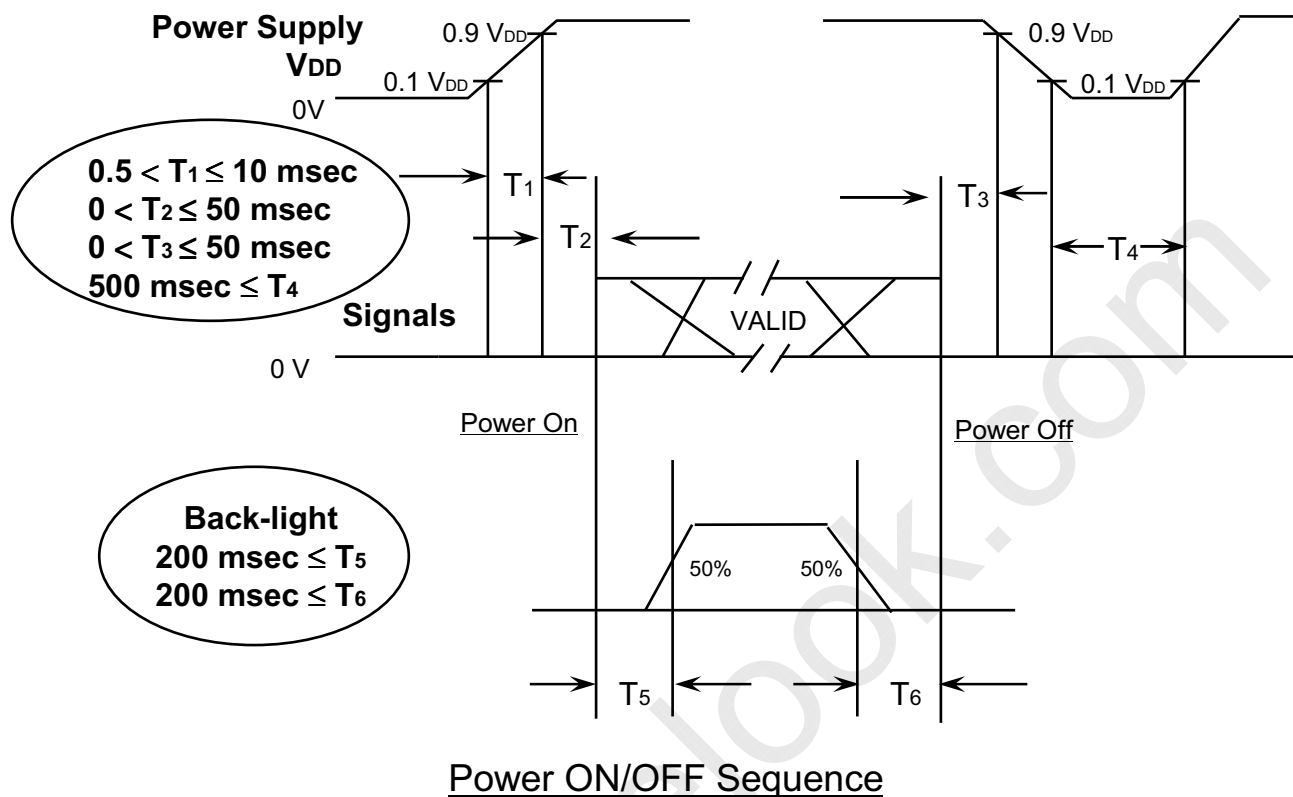
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6.3 Power ON/OFF Sequence

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: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



- T1 : Vdd rising time from 10% to 90%
 T2 : The time from Vdd to valid data at power ON.
 T3 : The time from valid data off to Vdd off at power Off.
 T4 : Vdd off time for Windows restart
 T5 : The time from valid data to B/L enable at power ON.
 T6 : The time from valid data off to B/L disable at power Off.

NOTE.

- (1) The supply voltage of the external system for the module input should be the same as the definition of VDD.
- (2) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become white.
- (3) In case of VDD = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

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7. MECHANICAL OUTLINE DIMENSION

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It will be attached with PDF file

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8. PACKING

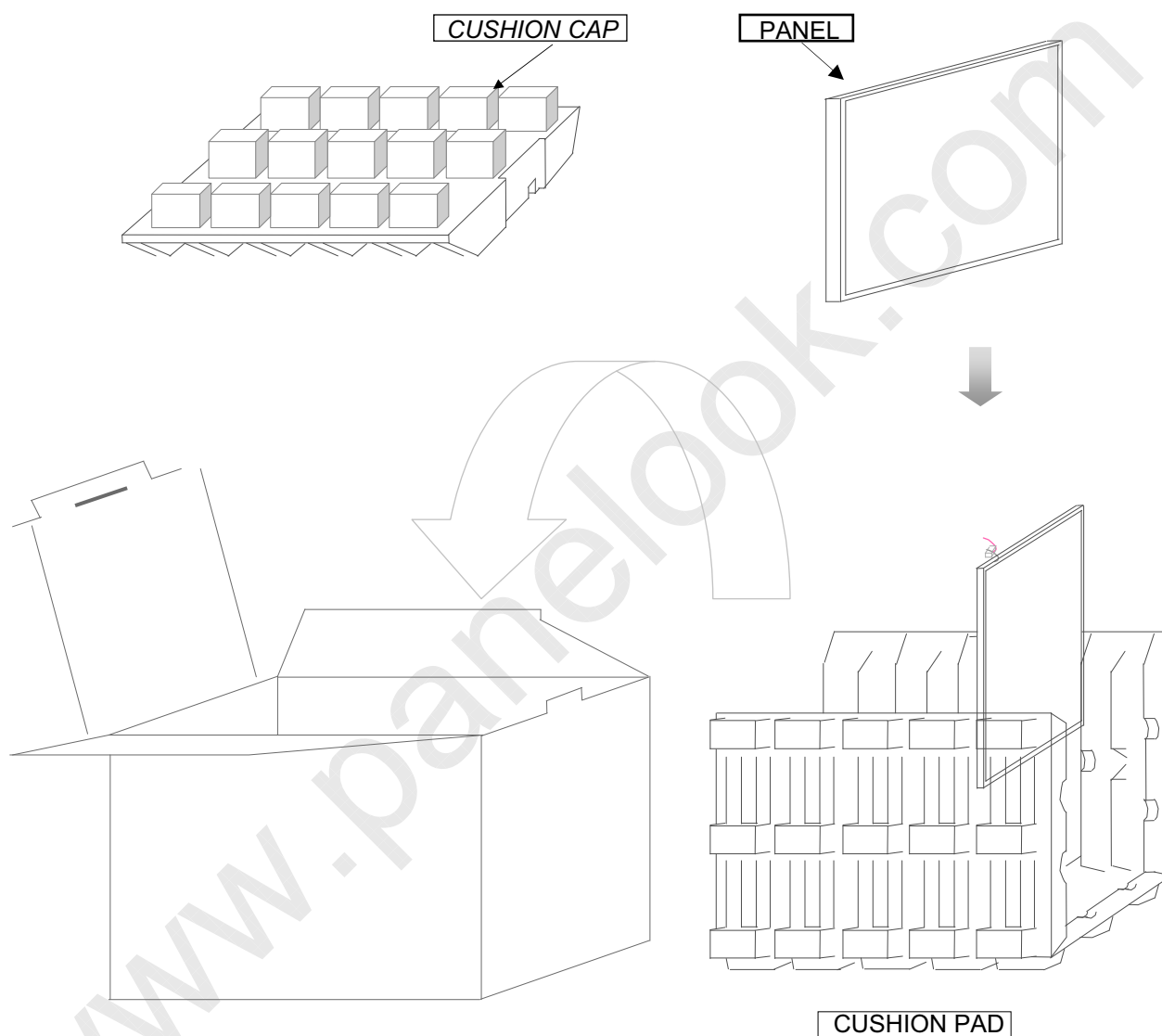
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1. CARTON(Internal Package)

(1) Packing Form

Corrugated Cardboard box and Corrupad form as shock absorber

(2) Packing Method



Note 1) Total Weight : Approximately 10 kg

2) Acceptance number of piling : 5 sets

3) Carton size : 463(W) x 359(L) x 333(H) mm

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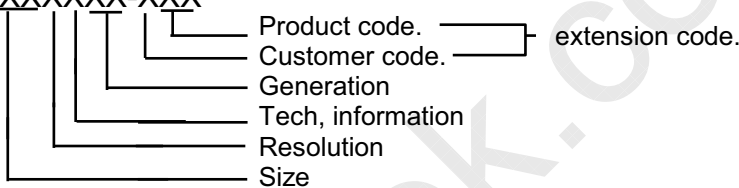
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No	Part name	Quantity
1	Static electric protective sack	10
2	Packing case (Inner box) included shock absorber	1 set
3	Pictorial marking	2 pcs
4	Carton	1 set

9. MARKINGS & OTHERS

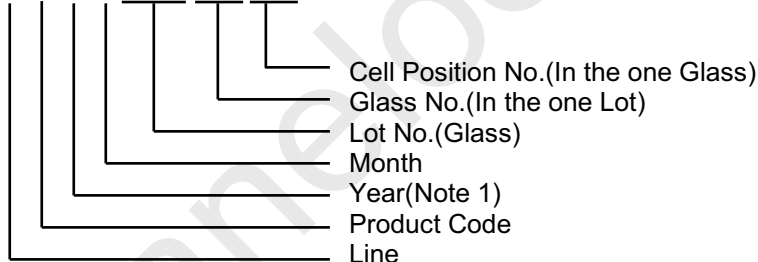
A nameplate bearing followed by is affixed to a shipped product at the specified location on each product.

(1) Parts number : LTNXXXXXXXX-XXX



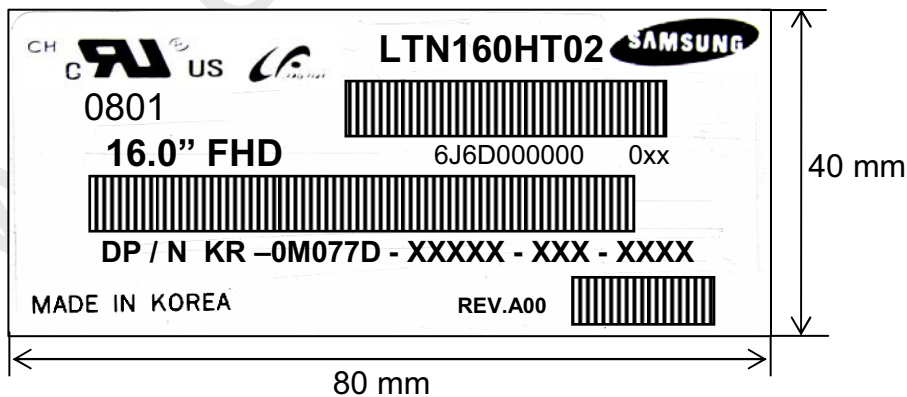
(2) Revision : Three letters

(3) Lot number : X Y 7 A XXX XX X



NOTE 1). This code indicating year is omitted in the products of KIHENG site.

(5) Nameplate Indication(Following example is only for reference)

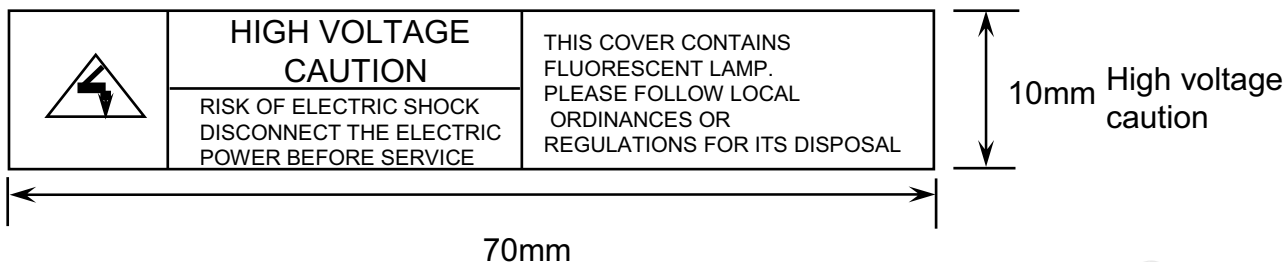


Parts name : LTN160HT02-0
 Lot number : 6J6D000000
 Inspected work week : 0801 Number ("0M077D" is for 160HT02-0)
 DP/N : Dell Part
 REV.A00 : Product Revision Code

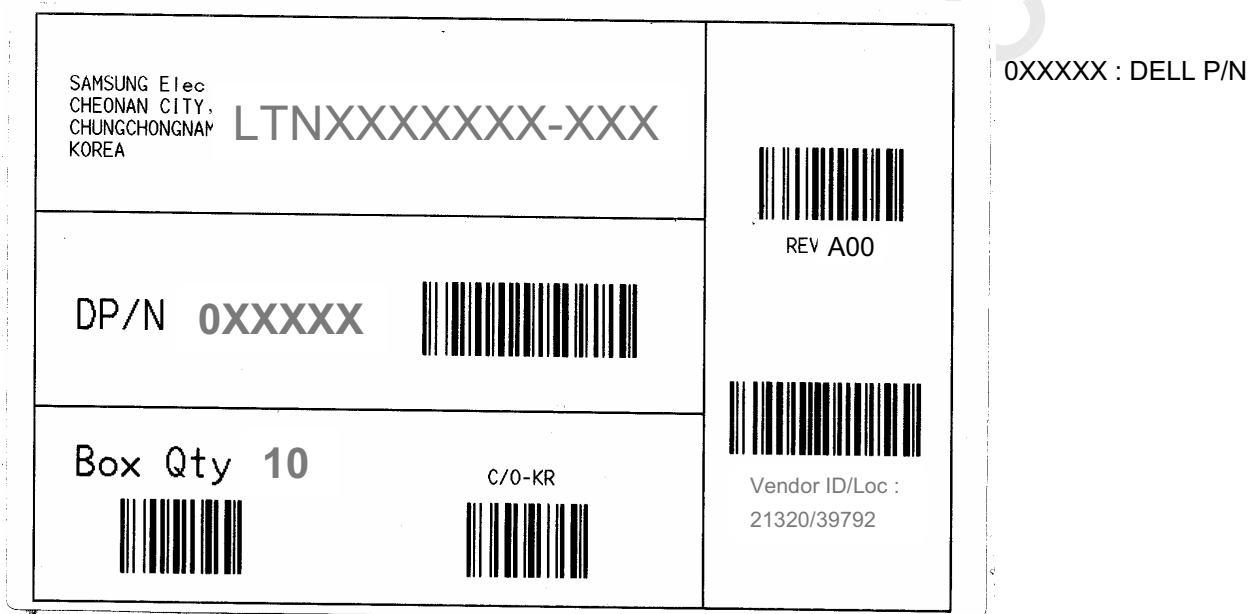
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This HIGH VOLTAGE CAUTION is carved in mold frame



(6) Packing small box attach (Following example is only for reference)



(7) Packing box Marking : Samsung TFT-LCD Brand Name



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10. GENERAL PRECAUTIONS

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1. Handling

- (a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.
- (b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module.
- (c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.
- (d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (f) The desirable cleaners are water, IPA (Isoprophyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (h) Protect the module from static, it may cause damage to the C-MOS Gate Array IC.
- (i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (j) Do not disassemble the module.
- (k) Do not pull or fold the lamp wire.
- (l) Do not adjust the variable resistor which is located on the back side.
- (m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (n) Pins of I/F connector shall not be touched directly with bare hands.

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2. STORAGE

- (a) Do not leave the module in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%.
- (b) Do not store the TFT-LCD module in direct sunlight.
- (c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

3. OPERATION

- (a) Do not connect,disconnect the module in the " Power On" condition.
- (b) Power supply should always be turned on/off by following item 6.3 " Power on/off sequence " .
- (c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (d) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, SEC is not to be held reliable for the defective operations. It is strongly recommended to contact SEC to find out fitness for a particular purpose.

4. OTHERS

- (a) Ultra-violet ray filter is necessary for outdoor operation.
- (b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, so on)
Otherwise the module may be damaged.
- (d) If the module displays the same pattern continuously for a long period of time,it can be the situation when the image "sticks" to the screen.
- (e) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

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	Byte	Field Name and Comments	Value	Value
	(hex)		(hex)	(binary)
Header	0	Header	00	00000000
	1	Header	FF	11111111
	2	Header	FF	11111111
	3	Header	FF	11111111
	4	Header	FF	11111111
	5	Header	FF	11111111
	6	Header	FF	11111111
	7	Header	00	00000000
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	4C	01001100
	9	EISA manufacture code (Compressed ASCII)	A3	10100011
	0A	Panel Supplier Reserved - Product Code	48	01001000
	0B	Panel Supplier Reserved - Product Code	54	01010100
	0C	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
	0D	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
	0E	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
	0F	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
	10	Week of manufacture	00	00000000
	11	Year of manufacture	12	00010010
	12	EDID structure version # = 1	01	00000001
	13	EDID revision # = 3	03	00000011
	Display Parameters	14	Video I/P definition = Digital I/P	90
15		Max H image size = (Rounded to cm)	23	00100011
16		Max V image size = (Rounded to cm)	14	00010100
17		Display gamma = (gamma × 100) - 100 = Example: (2.2 × 100) - 100 = 120	78	01111000
18		Feature support (no DPMS, Active off, RGB, timing BLK 1)	0A	00001010
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	87	10000111
	1A	Blue/White Low bit (BxBY/WxWy)	F5	11110101
	1B	Red X Rx = 0.xxx	94	10010100
	1C	Red Y Ry = 0.xxx	57	01010111
	1D	Green X Gx = 0.xxx	4F	01001111
	1E	Green Y Gy = 0.xxx	8C	10001100
	1F	Blue X Bx = 0.xxx	27	00100111
	20	Blue Y By = 0.xxx	27	00100111
	21	White X Wx = 0.xxx	50	01010000
	22	White Y Wy = 0.xxx	54	01010100
Established Timings	23	Established timings 1 (00h if not used)	00	00000000
	24	Established timings 2 (00h if not used)	00	00000000
	25	Manufacturer's timings (00h if not used)	00	00000000

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Standard Timing ID	26	Standard timing ID1 (01h if not used)	01	00000001
	27	Standard timing ID1 (01h if not used)	01	00000001
	28	Standard timing ID2 (01h if not used)	01	00000001
	29	Standard timing ID2 (01h if not used)	01	00000001
	2A	Standard timing ID3 (01h if not used)	01	00000001
	2B	Standard timing ID3 (01h if not used)	01	00000001
	2C	Standard timing ID4 (01h if not used)	01	00000001
	2D	Standard timing ID4 (01h if not used)	01	00000001
	2E	Standard timing ID5 (01h if not used)	01	00000001
	2F	Standard timing ID5 (01h if not used)	01	00000001
	30	Standard timing ID6 (01h if not used)	01	00000001
	31	Standard timing ID6 (01h if not used)	01	00000001
	32	Standard timing ID7 (01h if not used)	01	00000001
	33	Standard timing ID7 (01h if not used)	01	00000001
	34	Standard timing ID8 (01h if not used)	01	00000001
	35	Standard timing ID8 (01h if not used)	01	00000001
Timing Descriptor #1	36	Pixel Clock/10,000 (LSB)	F5	11110101
	37	Pixel Clock/10,000 (MSB)	3B	00111011
	38	Horizontal Active = xxx pixels (lower 8 bits)	80	10000000
	39	Horizontal Blanking (Thbp) = xxx pixels (lower 8 bits)	68	01101000
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	71	01110001
	3B	Vertical Active = xxx lines	38	00111000
	3C	Vertical Blanking (Tvbp) = xxx lines (DE Blanking typ. for DE only panels)	2A	00101010
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40	01000000
	3E	Horizontal Sync, Offset (Thfp) = xxx pixels	30	00110000
	3F	Horizontal Sync, Pulse Width = xxx pixels	20	00100000
	40	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	25	00100101
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000
	42	Horizontal Image Size =xxx mm	61	01100001
	43	Vertical image Size = xxx mm	C6	11000110
	44	Horizontal Image Size / Vertical image size	10	00010000
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no stereo, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition Referenced Default = 1Ah	1A	00011010
	Timing Descriptor #2	48	Pixel Clock/10,000 (LSB)	F5
49		Pixel Clock/10,000 (MSB)	3B	00111011
4A		Horizontal Active = xxx pixels (lower 8 bits)	80	10000000
4B		Horizontal Blanking (Thbp) = xxx pixels (lower 8 bits)	68	01101000
4C		Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	71	01110001
4D		Vertical Active = xxx lines	38	00111000
4E		Vertical Blanking (Tvbp) = xxx lines (DE Blanking typ. for DE only panels)	2A	00101010
4F		Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40	01000000
50		Horizontal Sync, Offset (Thfp) = xxx pixels	30	00110000
51		Horizontal Sync, Pulse Width = xxx pixels	20	00100000
52		Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	25	00100101
53		Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000
54		Horizontal Image Size =xxx mm	61	01100001
55		Vertical image Size = xxx mm	C6	11000110
56		Horizontal Image Size / Vertical image size	10	00010000
57		Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
58		Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
59		Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no stereo, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition Referenced Default = 1Ah	1A	00011010

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Timing Descriptor #3 Dell specific information	5A	Flag	00	00000000
	5B	Flag	00	00000000
	5C	Flag	00	00000000
	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FE	11111110
	5E	Flag	00	00000000
	5F	Dell P/N 1 st Character	4D	01001101
	60	Dell P/N 2 nd Character	30	00110000
	61	Dell P/N 3 rd Character	37	00110111
	62	Dell P/N 4 th Character	37	00110111
	63	Dell P/N 5 th Character	44	01000100
	64	LCD Supplier EEDID Revision # Bit[7] : 0=X, 1=A Bit[6:0] : 00, 01, 02... for SST 10, 11, 12... for PT 20, 21, 22... for ST 00, 01, 02... for X-Build (if Bit[7]=1)	80	10000000
	65	Manufacturer P/N	31	00110001
	66	Manufacturer P/N	36	00110110
	Timing Descriptor #4	67	Manufacturer P/N	30
68		Manufacturer P/N	48	01001000
69		Manufacturer P/N	54	01010100
6A		Manufacturer P/N	0A	00001010
6B		Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
6C		Flag	00	00000000
6D		Flag	00	00000000
6E		Flag	00	00000000
6F		Data Type Tag: Manufacturer Specified Data 00	00	00000000
70		Flag	00	00000000
71		SMBUS Value = XX nits	00	00000000
72		SMBUS Value = XX nits	00	00000000
73		SMBUS Value = XX nits	00	00000000
74		SMBUS Value = XX nits	00	00000000
75	SMBUS Value = XX nits	00	00000000	
76	SMBUS Value = XXX nits	00	00000000	
77	SMBUS Value = XXX nits	00	00000000	
78	SMBUS Value = max nits (Typically = 00h, XXX nits)	00	00000000	
79	Bit[7:3] Reserved Bit[2] 0: No RTC support, 1: RTC support Bit[1:0] 00: reserved, 01: single LVDS, 10: dual LVDS, 11: reserved 01h single channel LVDS, no RTC support 02h dual channel LVDS, no RTC support 05h single channel LVDS, with RTC support 06h dual channel LVDS, with RTC support	06	00000110	
7A	BIST Enable: Yes = '01' No = '00'	01	00000001	
7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	
7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	
7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	9B	10011011

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