SAMSUNG ELECTRONICS

Preliminary

TO :

DATE : June. 29, 2009.

SAMSUNG TFT-LCD

MODEL NO. : LTN170CT10-***

NOTE : Surface type [Glare]

Any Modification of Spec is not allowed without SEC' permission

SAMSUNG ELECTRONICS CO., LTD.

wise view™

Samsung Secret

CONTENTS

REVISION HISTORY

Preliminary

Date	Revision No.	Page	Summary
June. 29. 2009	P00	All	LTN170CT10-G01 Model spec was issued first.

GENERAL DESCRIPTION

DESCRIPTION

LTN170CT10-G01 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight system. The resolution of a 17.0" contains 1920 x 1200 pixels and can display up to 262,144 colors. 6 O'clock direction is the optimum viewing angle.

FEATURES

- High contrast ratio
- Wide UXGA (1920x1200 pixels) resolution
- Low power consumption
- DE (Data enable) only mode.
- 3.3V LVDS Interface
- On board EDID chip
- LED BLU Structure
- Pb free / Halogen free / As free

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	367.2(H) x 229.5(V) (17.0”diagonal)	mm	
Driver element	a-si TFT active matrix		
Display colors	262,144		
Number of pixel	1920 x 1200 (Wide UXGA)	pixel	
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.19125(H) x 0.19125(V)	mm	
Display Mode	Normally White		
Surface treatment	Haze 0, HARD-COATING 3H		ARC7

Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal (H)	379.0	379.3	379.6	mm	
	Vertical (V)	244.3	244.6	244.9	mm	
	Depth (D)	-	3.9	4.2	mm	(1)
Weight		-	560	565	g	

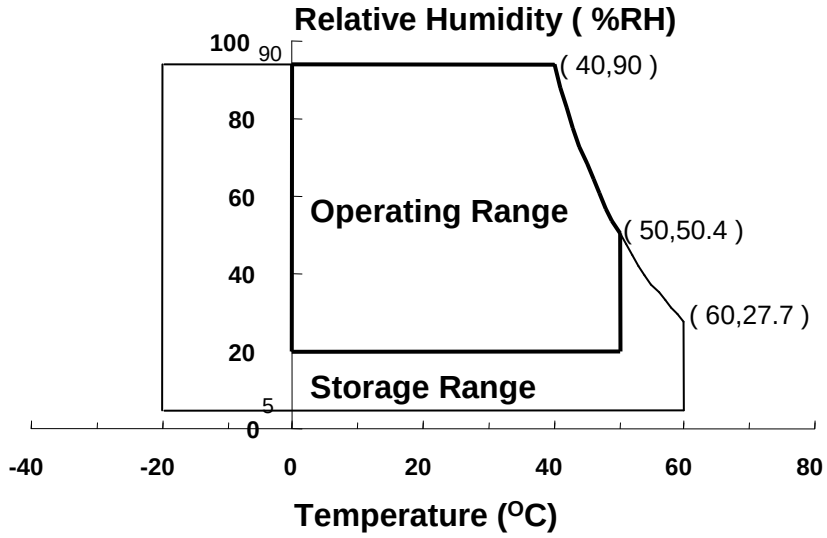
Note (1) Measurement condition of outline dimension
. Equipment : Vernier Calipers
. Push Force : 500g ·f (minimum)

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	T_{STG}	-20	60	°C	(1)
Operating temperate (Temperature of glass surface)	T_{OPR}	0	50	°C	(1)
Shock (non-operating)	Snop	-	240	G	(2),(4)
Vibration (non-operating)	Vnop	-	2.41	G	(3),(4)

Note (1) Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 °C ≥ Ta)
Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation



(2) 2ms, half sine wave, one time for ±X, ±Y, ± Z.
(3) 5 - 500 Hz, random vibration, 30min for X, Y, Z.
(4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.
(5) If product is used for extended time excessively or exposed to high temperatures for extended time, there is a possibility of wide viewing angle film damage which could affect visual characteristics.

1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

V_{DD} =3.3V, V_{SS} = GND = 0V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	V_{DD} - 0.3	V_{DD} + 0.3	V	(1)
Logic Input Voltage	V_{IN}	V_{DD} - 0.3	V_{DD} + 0.3	V	(1)

Note (1) Within Ta (25 ± 2 °C)

(2) BACK-LIGHT UNIT

Ta = 25 ± 2 °C

Item	Symbol	Min.	Max.	Unit	Note
LED Current	I_L	-	22.5	mA	(1)
LED Voltage	V_L	2.8	3.6	V	(1)

Note 1) Permanent damage to the device may occur if maximum values are exceeded
Functional operation should be restricted to the conditions described under normal operating conditions.

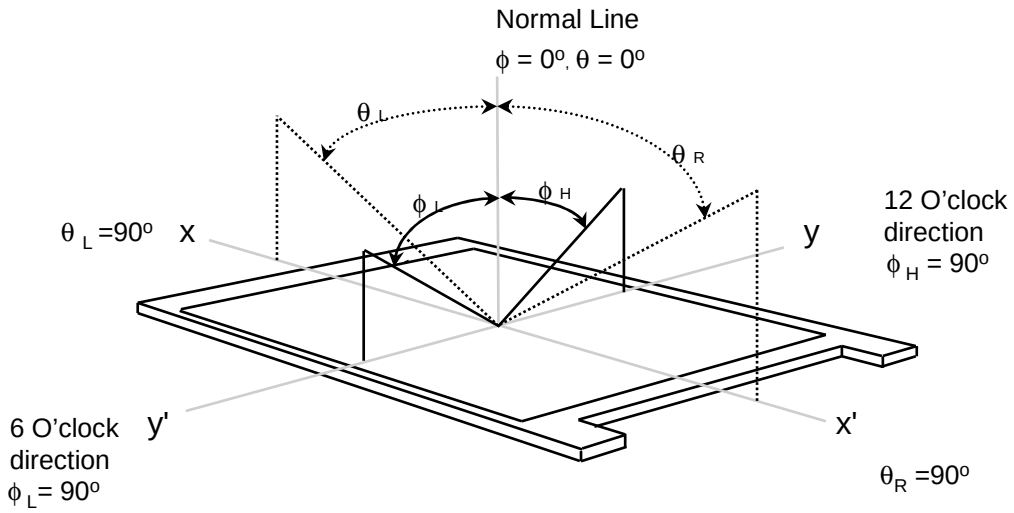
2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5).
Measuring equipment : TOPCON SR-3

* Ta = 25 ± 2 °C, V_{DD}=3.3V, fv= 60Hz, f_{DCLK} = 78.97MHz, I_L = 22.5mA

Item		Symbol	Condition	Min.	Typ.	Max	Unit	Note
Contrast Ratio (center)		CR		400	600	-	-	(1), (2), (5)
Response Time at Ta (Rising + Falling)		T_{RT}			16	20		(1), (3)
Average Luminance of White (160 Points)		$Y_{L,AVE}$	Normal Viewing Angle $\phi = 0$ $\theta = 0$	230	250	-	cd/m^2	I_L=22.5mA (1), (4)
Color Chromaticity (CIE)	Red	R_X		0.620	0.640	0.660	-	(1), (5) SR-3
		R_Y		0.310	0.337	0.357		
	Green	G_X		0.290	0.310	0.330		
		G_Y		0.595	0.615	0.635		
	Blue	B_X		0.130	0.150	0.170		
		B_Y		0.040	0.060	0.080		
	White	W_X		0.297	0.313	0.329		
		W_Y		0.313	0.329	0.345		
Viewing Angle	Hor.	θ_L	CR ≥ 10	65	70		Degrees	(1), (5) SR-3
		θ_H		65	70			
	Ver.	ϕ_H		50	60			
		ϕ_L		50	60			
160 Points White Variation		δ_L			TBD	-	%	(6)

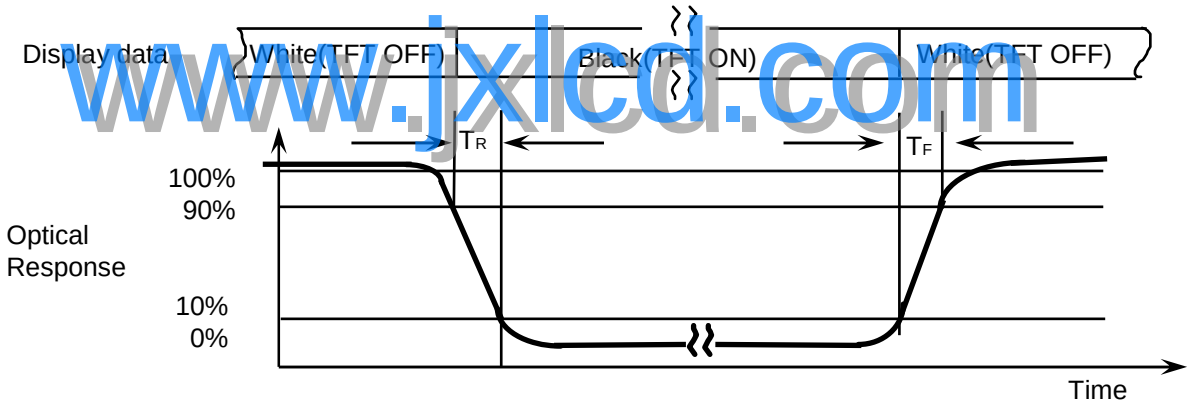
Note 1) Definition of Viewing Angle : Viewing angle range(10 ≤ C/R)



Note 2) Definition of Contrast Ratio (CR) : Ratio of gray max (Gmax) ,gray min (Gmin) at center points (7)

CR = Luminance at Gmax / Luminance at Gmin

Note 3) Definition of Response time :

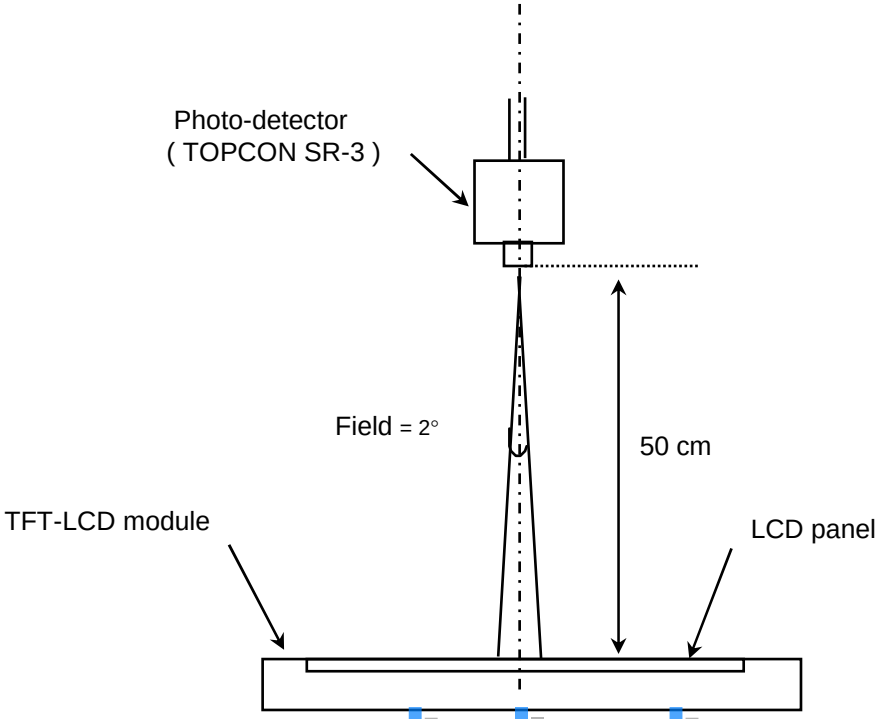


Note 4) Definition of Average Luminance of White

$Y_{L,AVE}$ = SUM(L1:L160) / 160

where L1 to L160 are the luminance values measured at point #1 to #160.

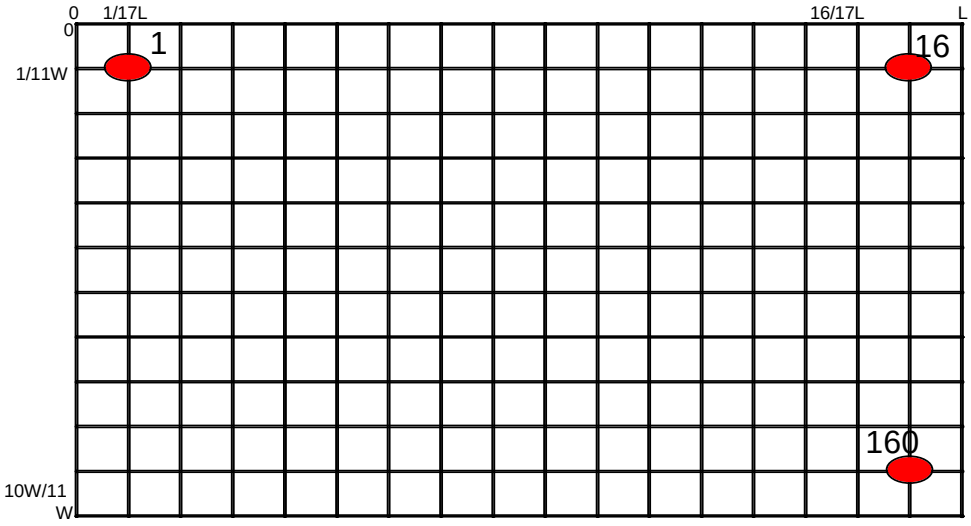
Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 min , the measurement should be executed. Measurement should be executed in a stable, windless,and dark room.
30 min after lighting the backlight. This should be measured in the center of screen.
Lamp current : 6.0mA (Inverter : SIC-130T)
Environment condition : Ta = 25 ± 2 °C



[Optical characteristics measurement setup]

Note 6) Definition of 160 points white variation (δ L)

δ L = 100% - (Lmax-Lmin)/Lmax
where, Lmax = max {Luminance values at 160 points},
Lmin = min {Luminance values at 160 points}



3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta= 25 ± 2°C

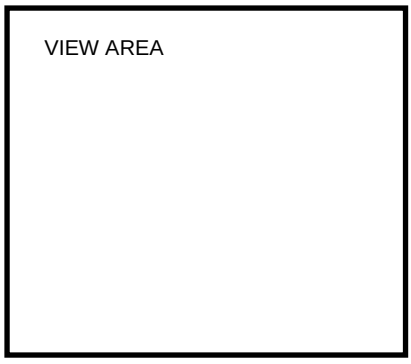
Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply		V_{DD}	3.0	3.3	3.6	V	
Differential Input Voltage for LVDS Receiver Threshold	High	V_{IH}	-	-	+100	mV	V_{CM} = +1.2V
	Low	V_{IL}	-100	-	-	mV	
Vsync Frequency		fv	-	60	-	Hz	
Hsync Frequency		f_H	-	75	-	KHz	
Main Frequency		f_{DCLK}	-	78.97	-	MHz	
Rush Current		I_{RUSH}	-	-	1.5	A	(4)
Current of Power Supply	White	I_{DD}	350	390	430	mA	(2),(3)*a
	Mosaic		450	500	550	mA	(2),(3)*b
	Black		570	630	690	mA	
	1 dot inv.		590	655	720	mA	(2),(3)*c

Note (1) Display data pins and timing signal pins should be connected. (GND = 0V)

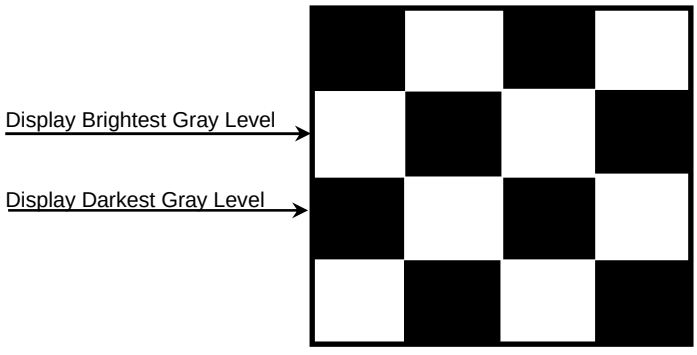
(2) f_V = 60Hz, f_{DCLK} = 80.81MHZ, V_{DD} = 3.3V , DC Current.

(3) Power dissipation pattern

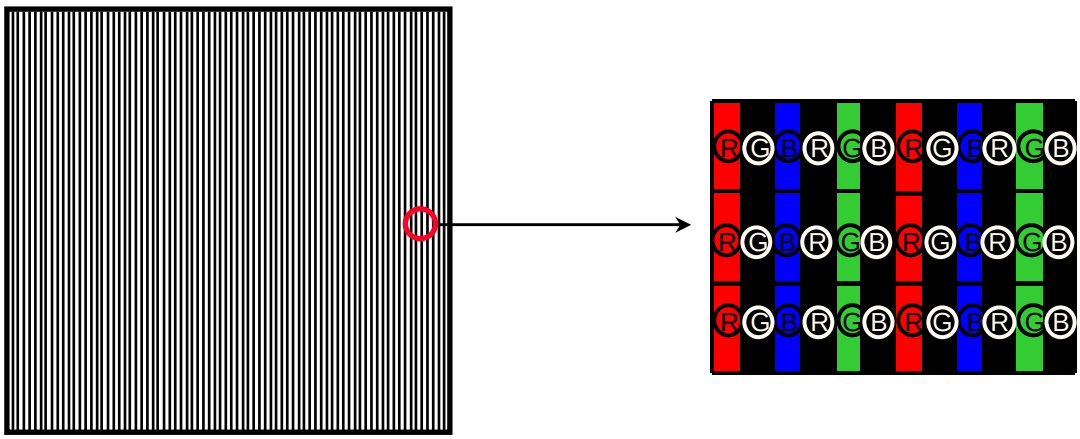
*a) White Pattern



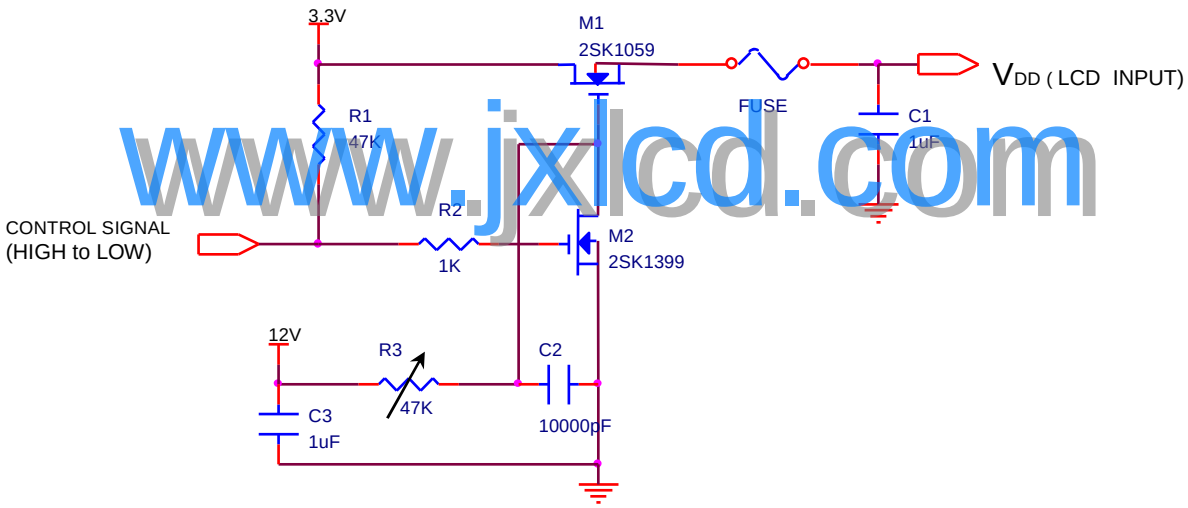
*b) Mosaic Pattern



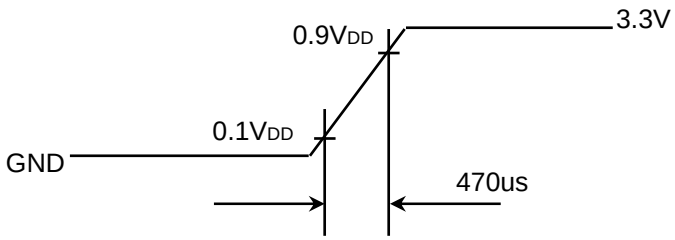
*c) 1dot Vertical stripe pattern



4) Rush current measurement condition



VDD rising time is 470us



3.2 BACK-LIGHT UNIT

Ta= 25 ± 2 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED Forward Current	IF	-	22.5	-	mA	
LED Forward Voltage	VF	-	3.2	3.4	V	
LED Array Voltage	VP	-	44.8	47.6	V	Vf X 14 LEDs
Power Consumption	P	-	-	6.73	W	If X Vf X 84 LEDs

3.3 LED Connection

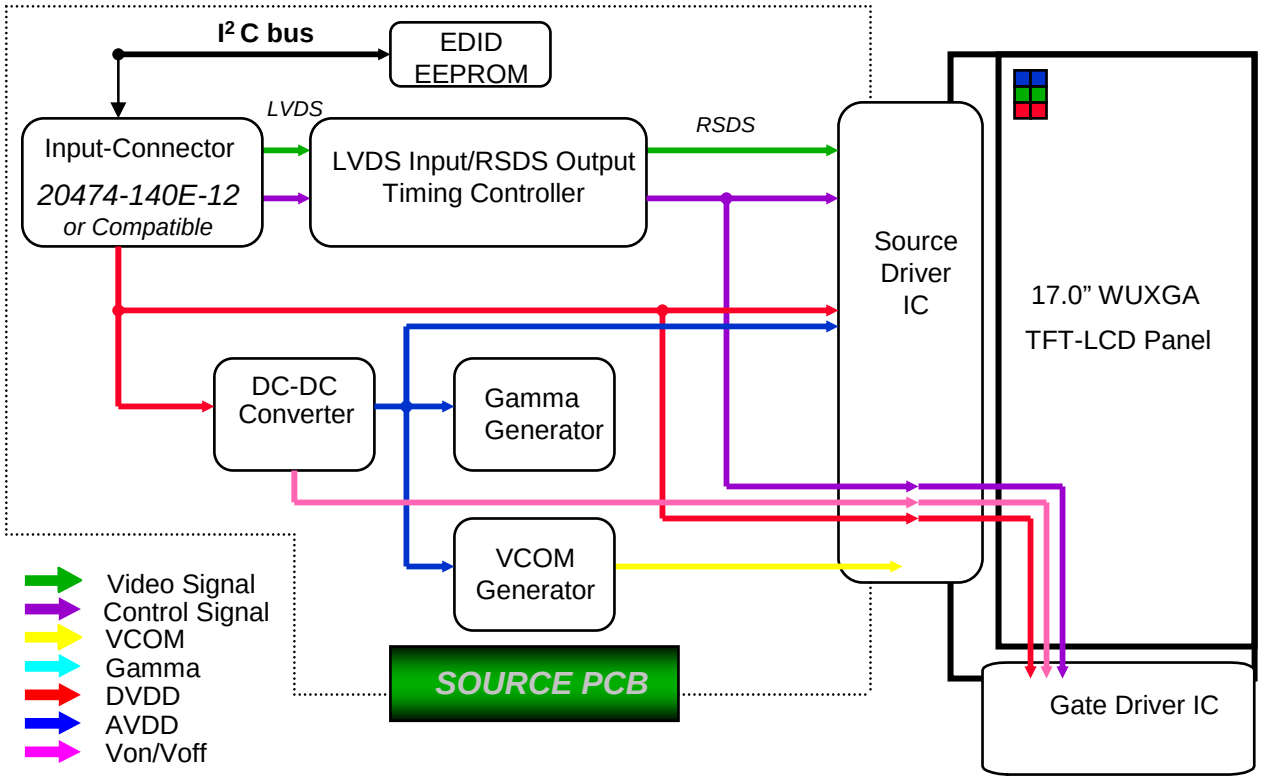
	LED 1	LED 2	LED 3	LED 4	LED 5	LED 6	LED 7	LED 8	LED 9	LED 10	LED 11	LED 12	LED 13	LED 14
1	1	7	13	19	25	31	37	43	49	55	61	67	73	79
2	2	8	14	20	26	32	38	44	50	56	62	68	74	80
3	3	9	15	21	27	33	39	45	51	57	63	69	75	81
4	4	10	16	22	28	34	40	46	52	58	64	70	76	82
5	5	11	17	23	29	35	41	47	53	59	65	71	77	83
6	6	12	18	24	30	36	42	48	54	60	66	72	78	84

3.4 BLU Connection

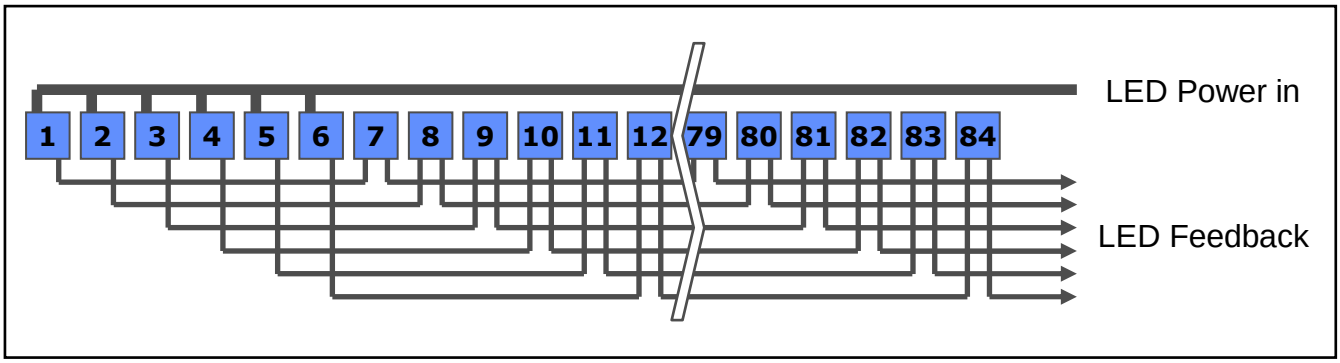
- Refer to the pin assignment (pin 31~40pin)

4. BLOCK DIAGRAM

4.1 TFT LCD Module



4.2 Back light Unit (Wooyoung - LED)



5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power LVDS, Connector : (I-PEX, 20474-140E-12 or Compatible)

No.	Symbol	Function	Polarity	Remarks
1	GND	Ground		
2	VDD	POWER SUPPLY +3.3V		
3	VDD	POWER SUPPLY +3.3V		
4	VEEDID	DDC 3.3V Power		
5	Vcc	POWER SUPPLY +3.3V		
6	CLKEDID	DDC Clock		
7	DATAEDID	DDC data		
8	O_RxIN0-	LVDS Differential Data INPUT (Odd R0-R5,G0)	Negative	
9	O_RxIN0+	LVDS Differential Data INPUT (Odd R0-R5,G0)	Positive	
10	GND	Ground		
11	O_RxIN1-	LVDS Differential Data INPUT (Odd G1-G5,B0-B1)	Negative	
12	O_RxIN1+	LVDS Differential Data INPUT (Odd G1-G5,B0-B1)	Positive	
13	GND	Ground		
14	O_RxIN2-	LVDS Differential Data INPUT (Odd B2-B5,Sync,DE)	Negative	
15	O_RxIN2+	LVDS Differential Data INPUT (Odd B2-B5,Sync,DE)	Positive	
16	GND	Ground		
17	O_RxCLK-	LVDS Differential Data INPUT (Odd Clock)	Negative	
18	O_RxCLK+	LVDS Differential Data INPUT (Odd Clock)	Positive	
19	GND	Ground		
20	E_RxIN0-	LVDS Differential Data INPUT (Even R0-R5,G0)	Negative	
21	E_RxIN0+	LVDS Differential Data INPUT (Even R0-R5,G0)	Positive	
22	GND	Ground		
23	E_RxIN1-	LVDS Differential Data INPUT (Even G1-G5,B0-B1)	Negative	
24	E_RxIN1+	LVDS Differential Data INPUT (Even G1-G5,B0-B1)	Positive	
25	GND	Ground		
26	E_RxIN2-	LVDS Differential Data INPUT (Even B2-B5,Sync,DE)	Negative	
27	E_RxIN2+	LVDS Differential Data INPUT (Even B2-B5,Sync,DE)	Positive	
28	GND	Ground		
29	E_RxCLK-	LVDS Differential Data INPUT (Even Clock)	Negative	
30	E_RxCLK+	LVDS Differential Data INPUT (Even Clock)	Positive	

5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power LVDS, Connector : (I-PEX, 20474-140E-12 or Compatible)

No.	Symbol	Function	Polarity	Remarks
31	Vdc1	LED Cathode (Negative)		
32	Vdc2	LED Cathode (Negative)		
33	Vdc3	LED Cathode (Negative)		
34	Vdc4	LED Cathode (Negative)		
35	Vdc5	LED Cathode (Negative)		
36	Vdc6	LED Cathode (Negative)		
37	NC	NC		
38	Vdc (1~2)	LED Anode (Negative)		
39	Vdc (3~4)	LED Anode (Negative)		
40	Vdc (5~6)	LED Anode (Negative)		

5.2 LVDS Interface : Transmitter DS90CF363 or Compatible

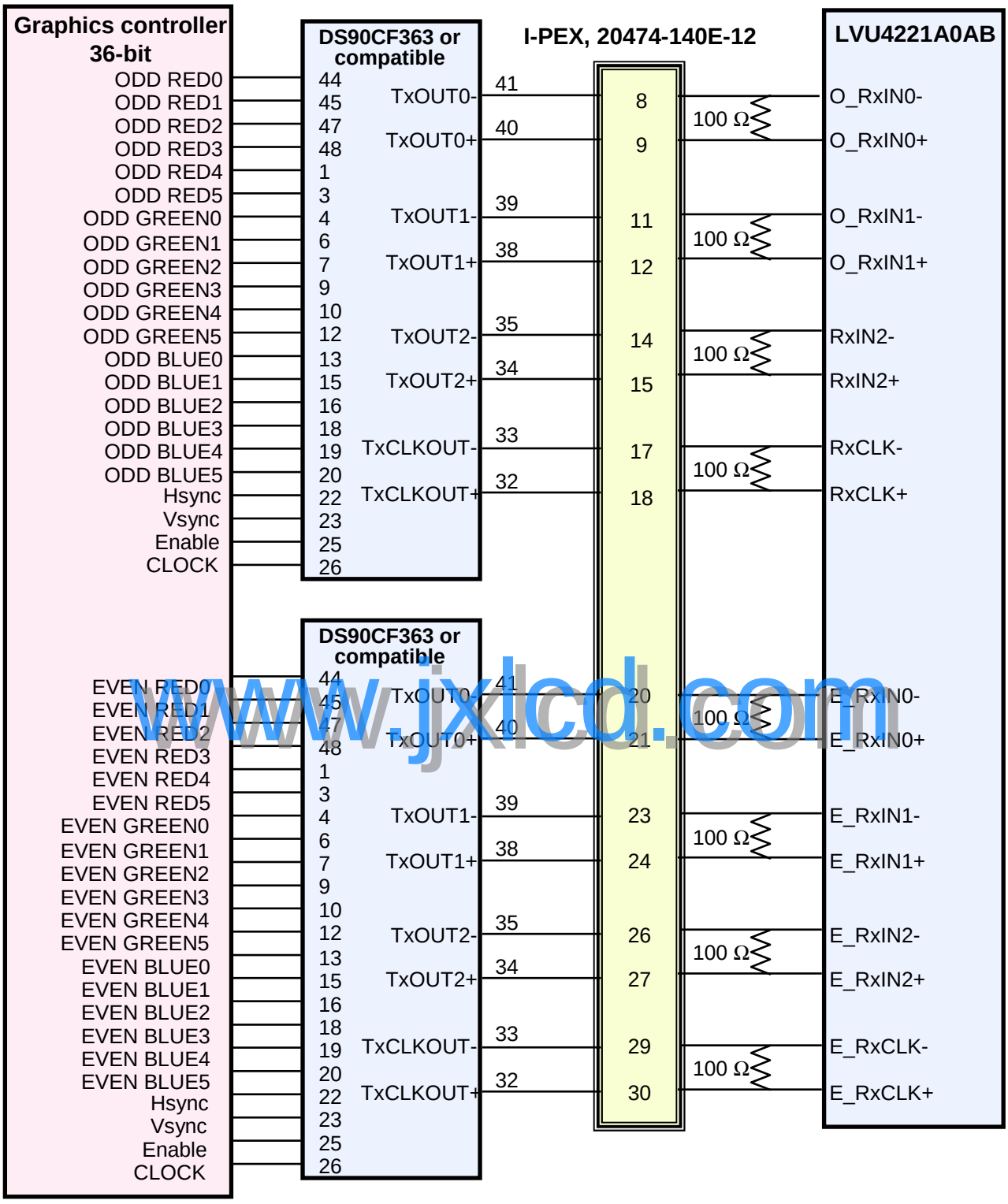
LVDS for Odd pixel

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
44	TxIN0	RO0	12	TxIN11	GO5
45	TxIN1	RO1	13	TxIN12	BO0
47	TxIN2	RO2	15	TxIN13	BO1
48	TxIN3	RO3	16	TxIN14	BO2
1	TxIN4	RO4	18	TxIN15	BO3
3	TxIN5	RO5	19	TxIN16	BO4
4	TxIN6	GO0	20	TxIN17	BO5
6	TxIN7	GO1	22	TxIN18	Hsync
7	TxIN8	GO2	23	TxIN19	Vsync
9	TxIN9	GO3	25	TxIN20	DE
10	TxIN10	GO4	26	TxCLK IN	Clock

LVDS for Even pixel

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
44	TxIN0	RE0	12	TxIN11	GE5
45	TxIN1	RE1	13	TxIN12	BE0
47	TxIN2	RE2	15	TxIN13	BE1
48	TxIN3	RE3	16	TxIN14	BE2
1	TxIN4	RE4	18	TxIN15	BE3
3	TxIN5	RE5	19	TxIN16	BE4
4	TxIN6	GE0	20	TxIN17	BE5
6	TxIN7	GE1	22	TxIN18	Hsync
7	TxIN8	GE2	23	TxIN19	Vsync
9	TxIN9	GE3	25	TxIN20	DE
10	TxIN10	GE4	26	TxCLK IN	Clock

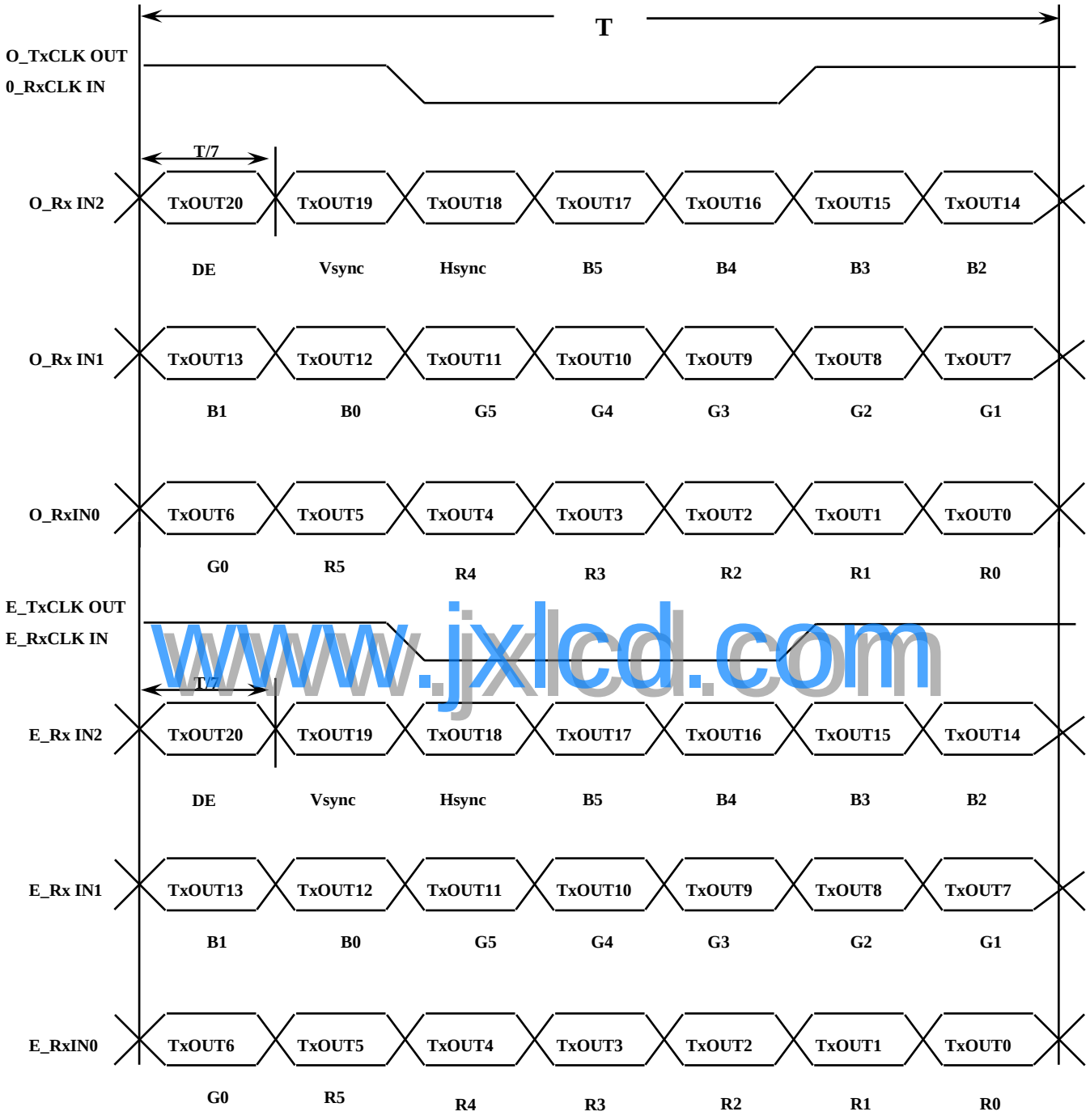
LVDS Interface



Note : The LCD Module uses a 100ohm resistor between positive and negative lines of each receiver input.

5.3 Timing Diagrams of LVDS For Transmission

LVDS Receiver : Integrated T-CON

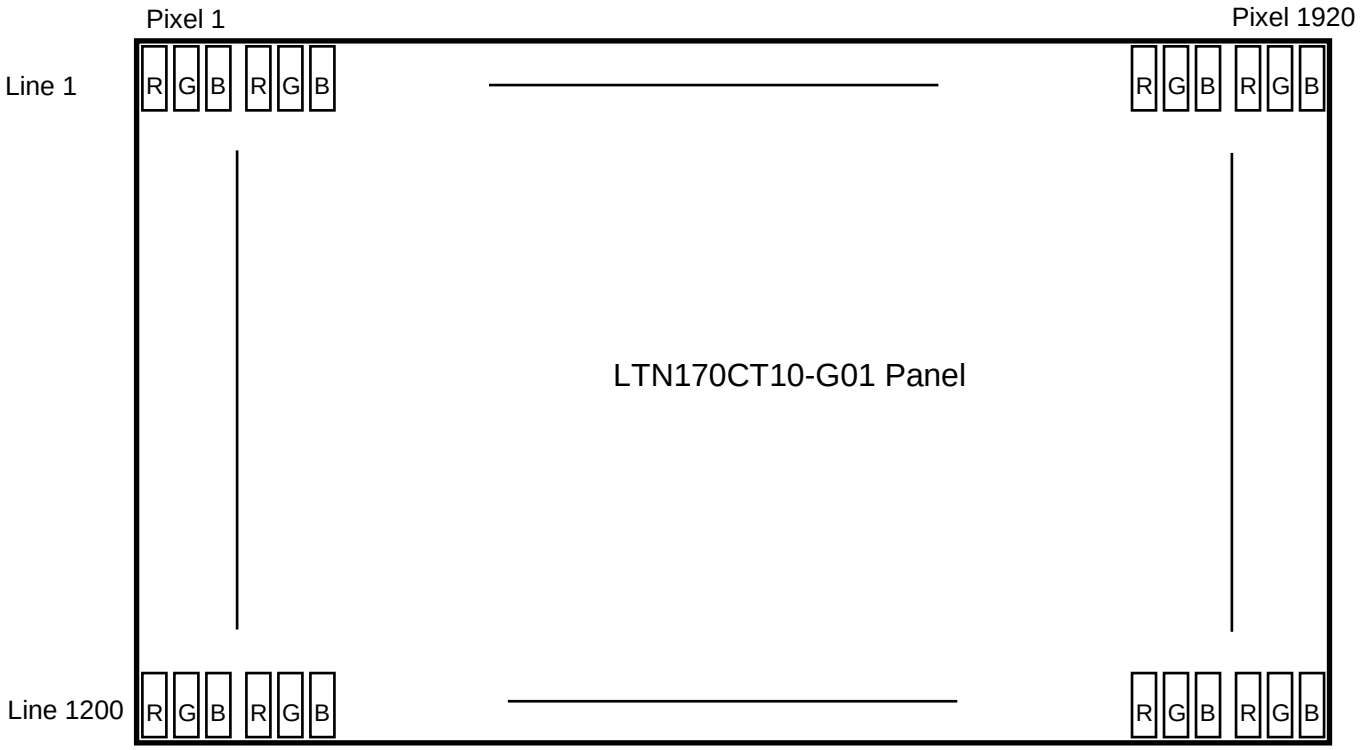


5.4 Input Signals, Basic Display Colors and Gray Scale of Each Color

Color	Display	Data Signal																		Gray Scale Level
		Red						Green						Blue						
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	45	B5	
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
Gray Scale Of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~R60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
	Light	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
Gray Scale Of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
Gray Scale Of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
	Light	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

Note 1) Definition of gray :
Rn: Red gray, Gn: Green gray, Bn: Blue gray (n=gray level)
Note 2)Input signal: 0 =Low level voltage, 1=High level voltage

5.5 Pixel Format in the display

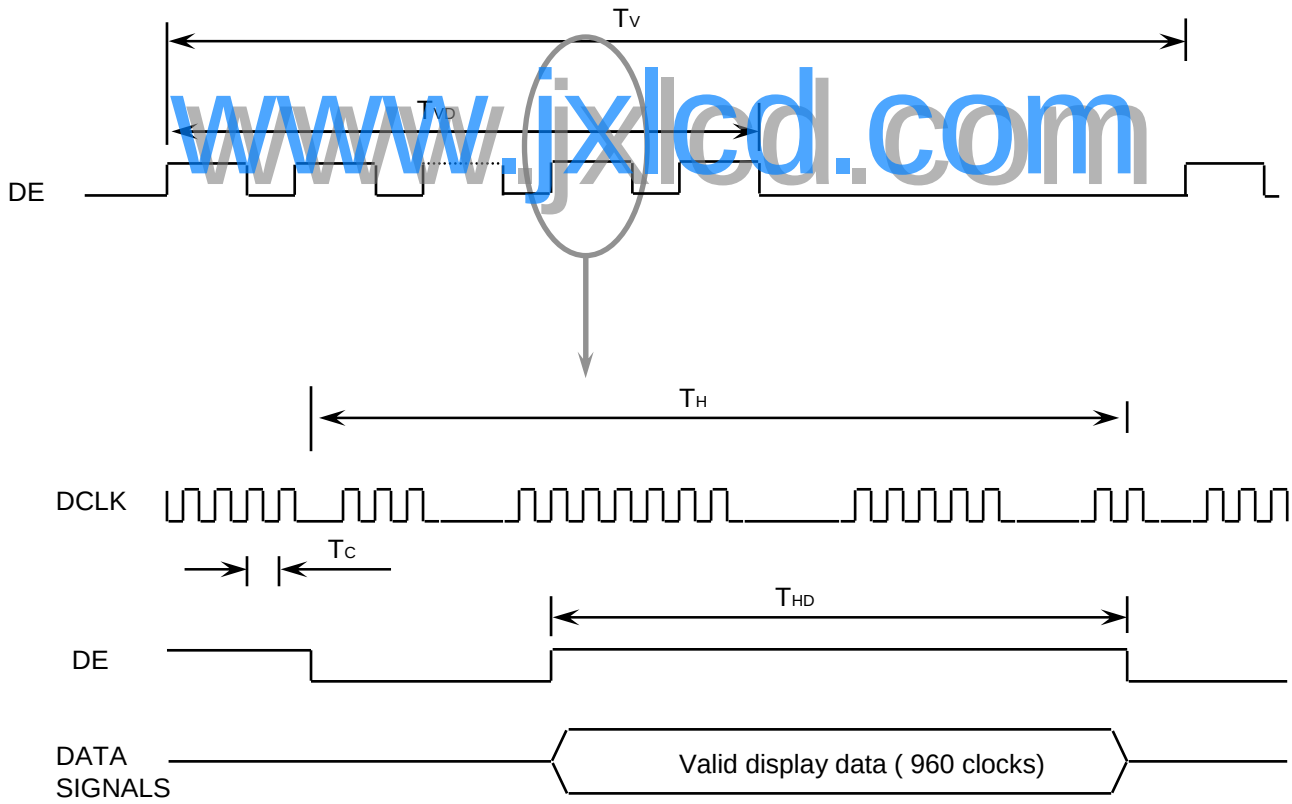


6. INTERFACE TIMING

6.1 Timing Parameters

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frame Frequency	Cycle	T_V	-	1200	-	Lines	-
Vertical Active Display Term	Display Period	T_{VD}	-	51	-	Lines	-
One Line Scanning Time	Cycle	T_H	-	960	-	Clocks	-
Horizontal Active Display Term	Display Period	T_{HD}	-	184	-	Clocks	-

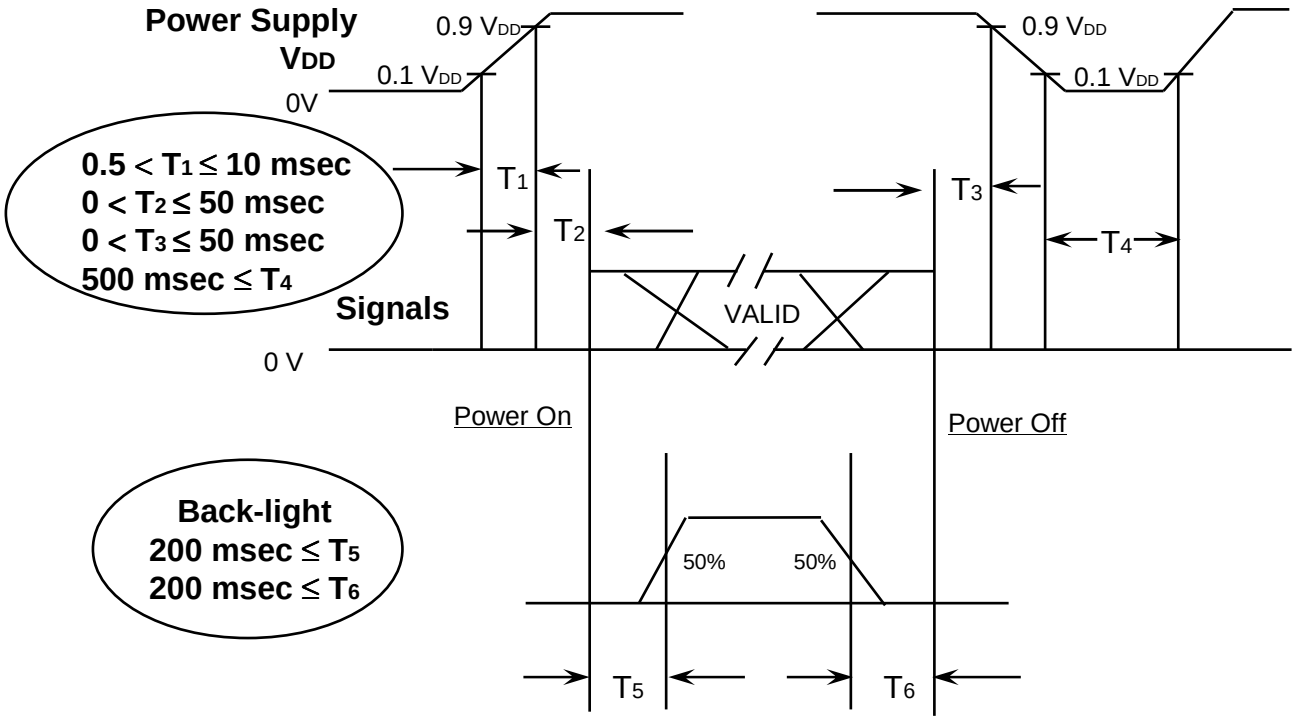
6.2 Timing diagrams of interface signal



Note : All input condition(level&timing) for LVU4221A0AB are the same with those of DS90CF363 or compatible.

6.3 Power ON/OFF Sequence

: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

T1 : Vdd rising time from 10% to 90%
T2 : The time from Vdd to valid data at power ON.
T3 : The time from valid data off to Vdd off at power Off.
T4 : Vdd off time for Windows restart
T5 : The time from valid data to B/L enable at power ON.
T6 : The time from valid data off to B/L disable at power Off.

NOTE.

(1) The supply voltage of the external system for the module input should be the same as the definition of V_{DD}.

(2) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become white.

(3) In case of V_{DD} = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. MECHANICAL OUTLINE DIMENSION

Preliminary

[Refer to the next page]

Samsung Secret

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994. IT IS EXPECTED THAT THE SUPPLIER UNDERSTAND AND COMPLY WITH ALL TOLERANCES AS DESCRIBED IN THIS STANDARD AND APPLIED TO THIS DRAWING.

2. PART MUST COMPLY WITH THE REGULATED SUBSTANCES REQUIREMENTS:
   - EUROPEAN ROHS DIRECTIVE 2002/95/EC
   - APPLE ROHS COMPLIANCE SPECIFICATION 069-1111
   - APPLE REGULATED SUBSTANCES SPECIFICATIONS 069-0135
   - APPLE HALOGEN-FREE SPECIFICATION 069-1857

3. TOLERANCES DESIGNATED WITH THE SYMBOL (SPC C) SHALL BE PRODUCED WITH STATISTICAL TOLERANCE PROCESS CONTROLS. IN ORDER TO USE THE TOLERANCE ON A FEATURE, THE STATISTICAL PROCESS (CP, CPK, ETC) OF THE PART MUST BE VALIDATED AND APPROVED BY APPLE SQE.

[4] AREA INSIDE THE VIEWABLE BOUNDARY MUST BE FREE OF ANY COSMETIC DEFECT. THIS INCLUDES THE ABILITY TO SEE THE EDGE OF POLARIZER FILM OR ANY OTHER LAYER, OR A DEFECT OF IN THE EDGE QUALITY OF POLARIZER FILM OR ANY OTHER LAYER. SEE APPLE SPECIFICATION 062-7003.

5. TAPE HOLDING M-CHASSIS TO LCD GLASS TO BE 0.10MM MAXIMUM.

6. THE COSMETIC REQUIREMENT IS TO NOT ALLOW PARTICLES 50 um OR LARGER ANYWHERE IN THE VIEWABLE AREA OF THE DISPLAY. ASSEMBLY SHOULD BE BAGGED INSIDE THE CLEAN ROOM IN AIRTIGHT DUST PROOF SEALED BAG WHEN SHIPPED AFTER PARTICLE REQUIREMENT HAS BEEN MET.

[7] REFER TO 3D CAD FOR METAL CHASSIS CORNER HOLE REQUIREMENTS.

8. LT4 COATING-LOW-REFLECTION GLOSS SURFACE-1% REFLECTANCE, >3H HARDNESS

[9] MAXIMUM ALLOWABLE FLEX BONDING AREAS.

10. DISPLAY GLASS TO HAVE A REMOVIBLE PROTECTIVE COVER.

11. DISPLAY PANEL TO MEET ALL REQUIREMENTS OF APPLE PANEL RF TEST REQUIREMENTS AND DESIGN GUIDE SPECIFICATION, 069-2794.

12. MASS = 565G MAXIMUM (FAI 134) (SPC B)

13. PANEL MCO CANNOT DEVIATE FROM SIZE OR FLATNESS SPECIFIED DIMENSIONS AFTER SUBJECTION TO THE FOLLOWING APPLE ENVIRONMENTAL TEST PROCEDURES:

    A. 080-1653 - STORAGE TEST
    B. 080-1654 - HEAT SOAK
    C. 080-1655 - THERMAL CYCLING
    D. 080-1656 - TEMPERATURE AND HUMIDITY CYCLING

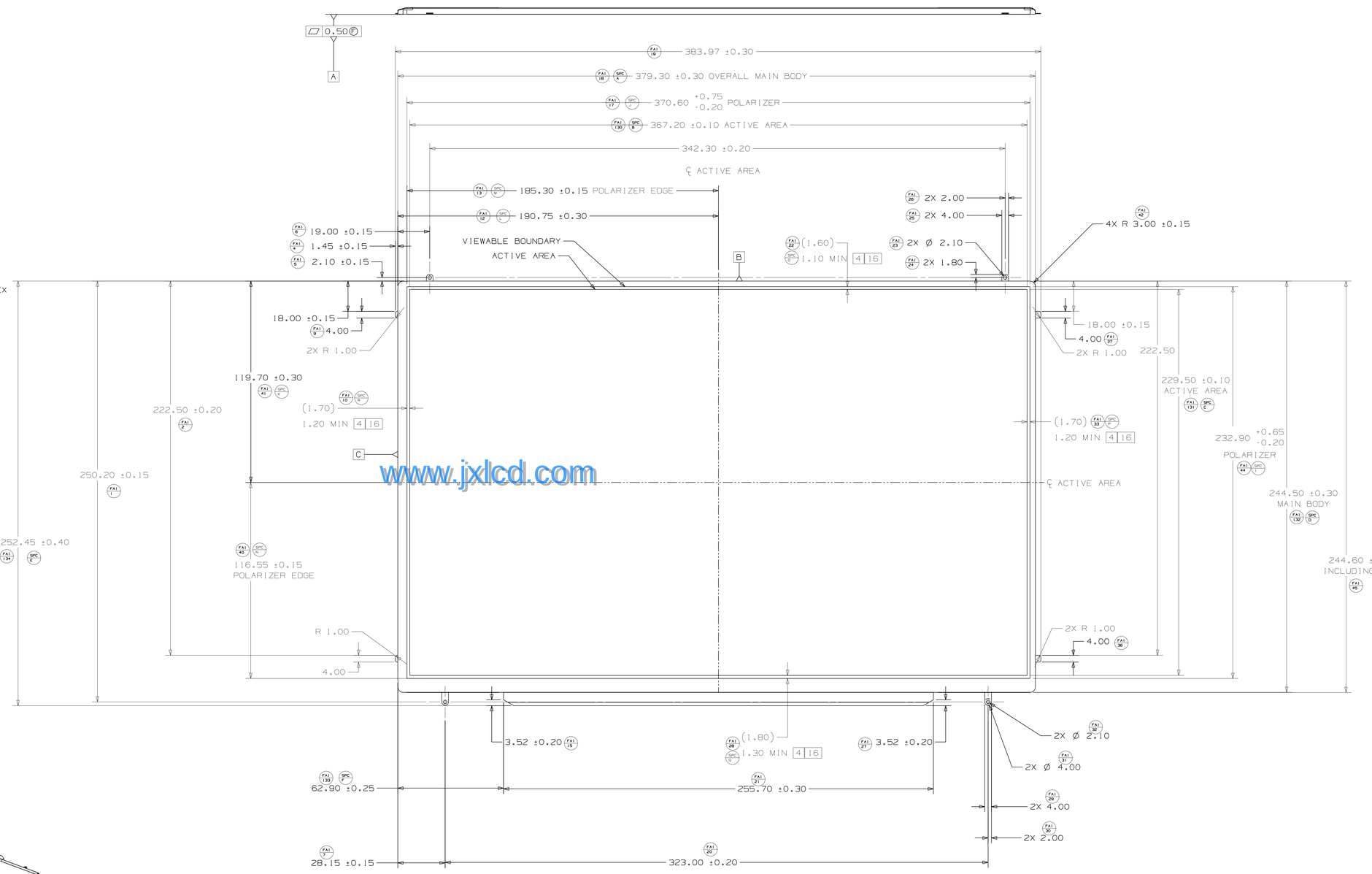
    ASSEMBLIES MUST BE INSTALLED INTO TEST SUPPORT FIXTURES PER 3D DESIGN SHOWN ON PAGE 6 OF 6 OF THIS MCO DOCUMENT, AND THEN SUBJECTED TO THE ABOVE TEST METHODS. INSPECTION OF FLATNESS AND OVER ALL SIZE DIMENSIONS SHOULD SHOW NO DIMENSIONS OUT OF SPECIFIED TOLERANCES. THESE DIMENSIONS INCLUDE FAI'S: 1, 3, 12, AND 110 THROUGH 133.

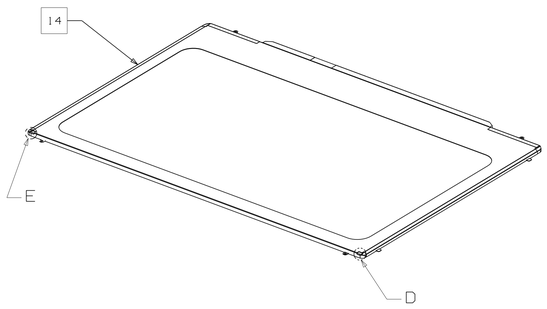
[14] MATERIAL: METAL CHASSIS STAINLESS STEEL 304 1/2 HARD 0.30 THICK OR APPLE PRODUCT DESIGN APPROVED EQUIVALENT

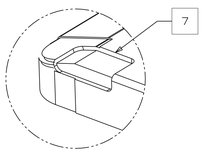
[15] MUST BE MEASURED IN U-SHAPED GO/NO GO FIXTURE WITH NO DAMAGE FOR LOOPED FLEX

[16] DIMENSION APPLIES TO ENTIRE EDGE

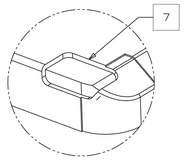
REV	RFA#	DESCRIPTION OF REVISION
09		REMOVED 1.20 FROM EACH END OF THE BOARD RH 07/30/08
11	XXXXXX	UPDATE 2D DRAWING ALVIN LIN 08/08/08
12	616456	UPDATED RFA NUMBER P. AUGENBERGS 8/11/08
13	620791	ADDED SPC TO CONNECTOR CENTERLINE P. AUGENBERGS 8/21/08
14	631741	ADDED .25 RADIUS ON TABS. RESIZED DRAWING TO E SIZE. A.SANTOS 9/23/08
15	636086	UPDATED SIDE TABS, POLARIZER SIZE, AND FLEX DIMENSIONING P. AUGENBERGS 10/8/08
16	653337	UPDATED DIMENSIONING SCHEME FOR ACTIVE AREA, POLARIZER EDGE. ADDED SPC K,L,M,N P. AUGENBERGS 11/18
17	XXXXXX	SPEC RELIEF ON FAI 19, 45, 63, 92, 132. INCREASED MYLAR OPENING, ADDED FAI 144, 145. UPDATED FAI 64 TO BOARD EDGE. TIGHTENED TOLERANCES ON FAI 17, 13, 22, 33, 44, 28, 10, 40, 131 P. AUGENBERGS 12/8/08
18	662562	ADDED NOTE 16. RELIEVED SPEC ON POLARIZER SIZE, LOCATION TOLERANCE P. AUGENBERGS 1/8/09







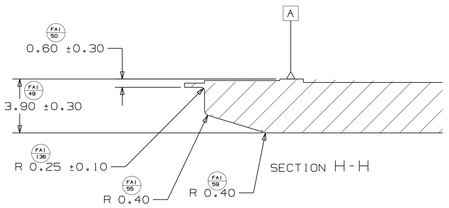
DETAIL E

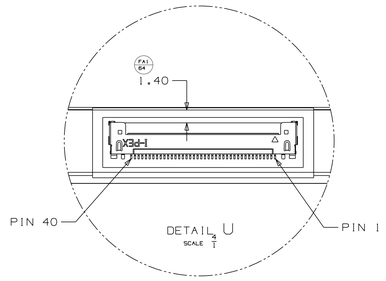


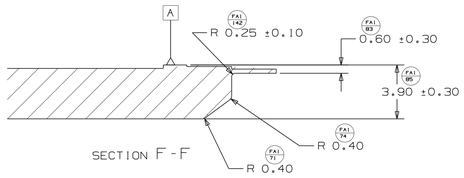
DETAIL D

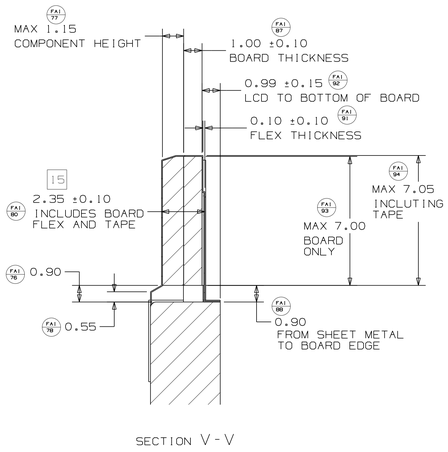
METRIC	Apple Inc.
DRAFTER: W. SCHMIDT — DATE: 6/10/08	NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: (i) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (ii) NOT TO REPRODUCE OR COPY IT (iii) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART (iv) ALL RIGHTS RESERVED
DESIGNER: R. HOPKINSON — DATE: 6/10/08	
DIMENSIONS ARE IN MILLIMETERS TOLERANCES X.X ±0.4 X.XX ±0.20 X.XXX ±0.100 ANGLES ±0.5° DO NOT SCALE DRAWINGS	TITLE: MCO, LCD, K20
THIRD ANGLE PROJECTION — SIZE: E	DRAWING NUMBER: 069-3225 — REV.: 18
	SCALE: NONE — SHT 1 OF 5

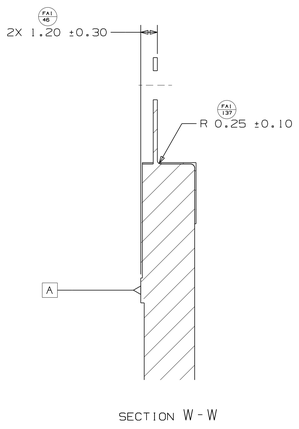
NX GENERATED

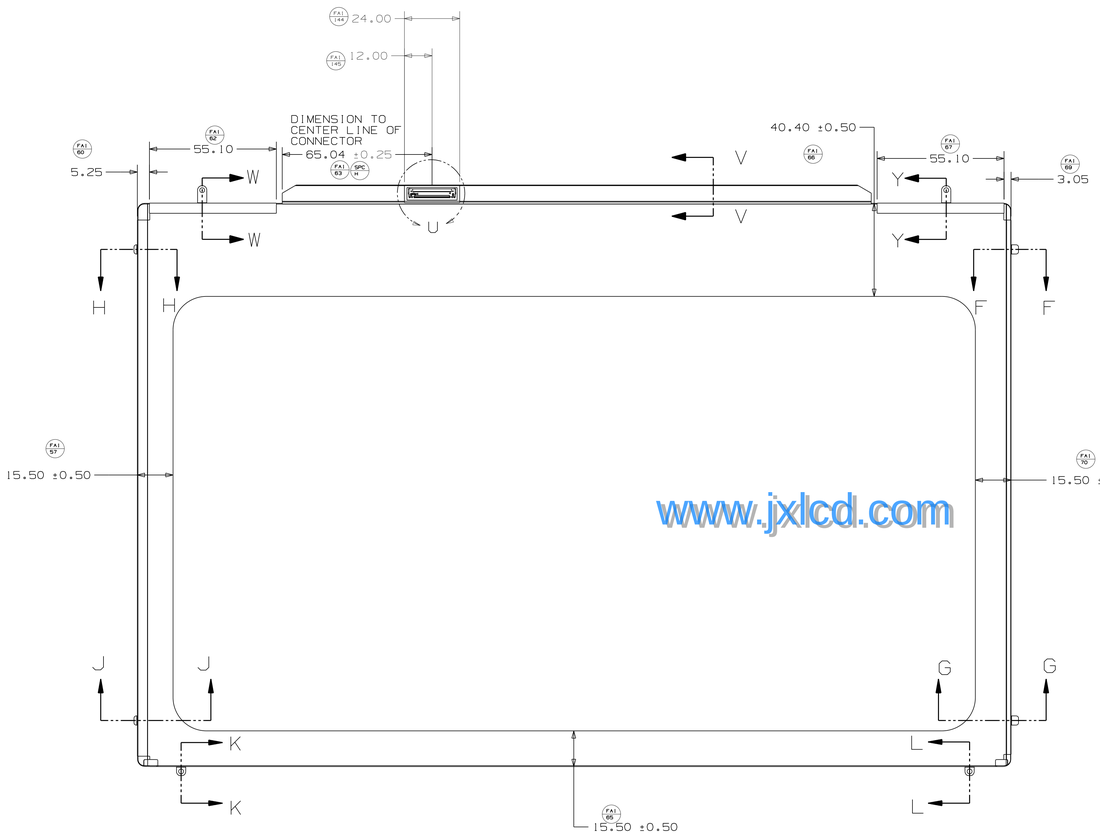


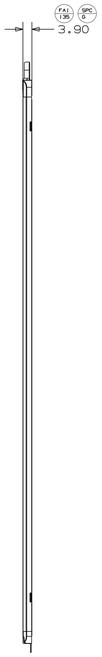


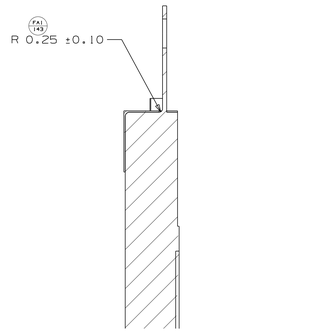


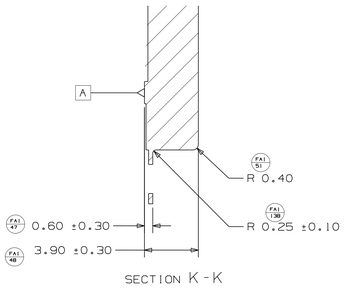


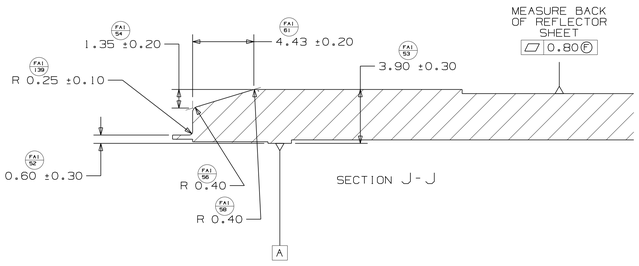


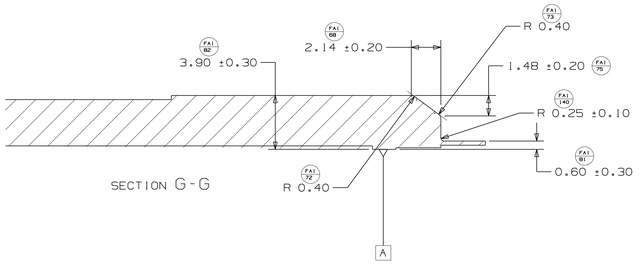


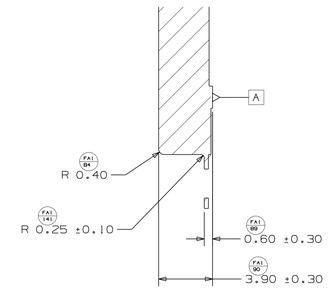






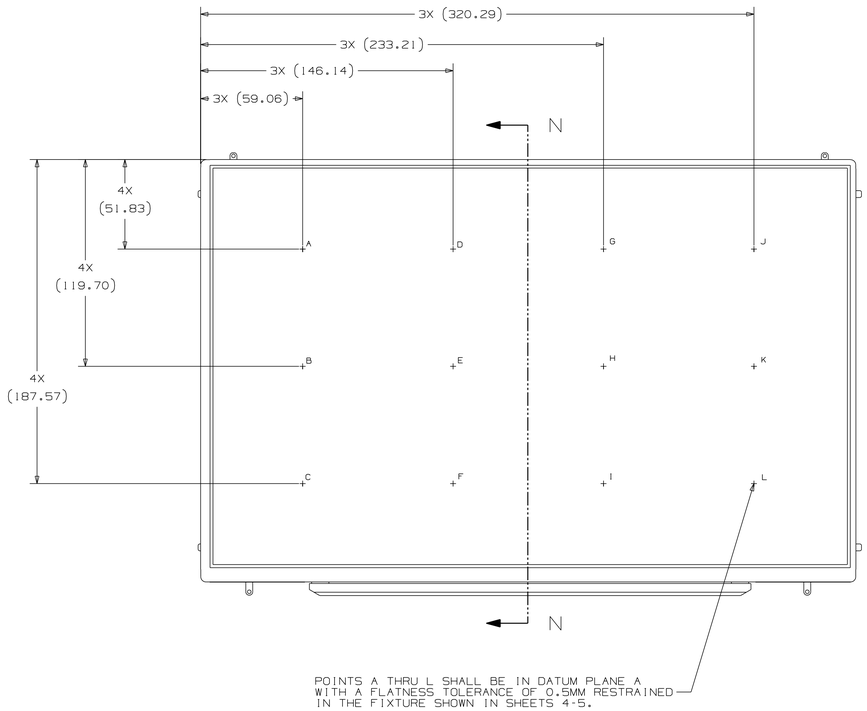




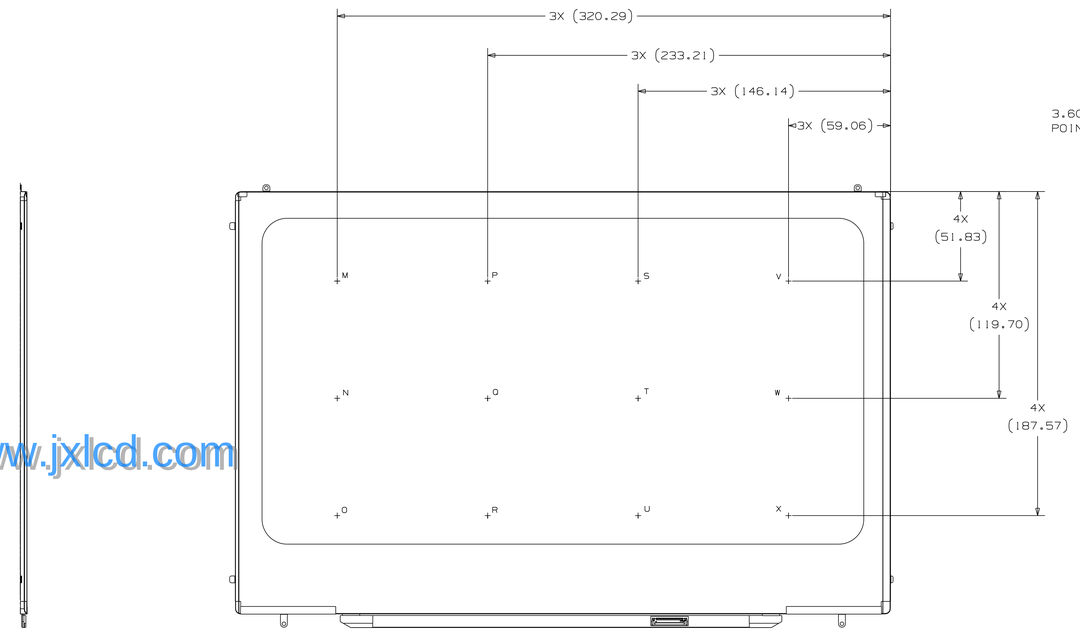


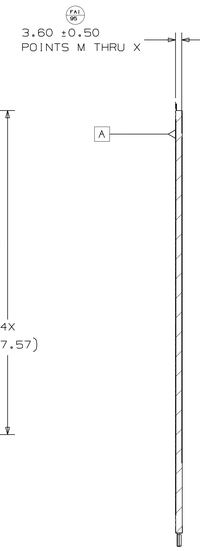
Apple Inc.

SIZE	DRAWING NUMBER	REV.
E	069-3225	18
SCALE	NONE	SHT 2 OF 5



POINTS A THRU L SHALL BE IN DATUM PLANE A WITH A FLATNESS TOLERANCE OF 0.5MM RESTRAINED IN THE FIXTURE SHOWN IN SHEETS 4-5.





SECTION N-N

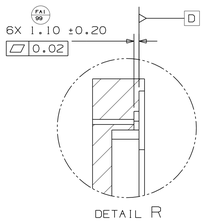
Apple Inc.

SIZE	DRAWING NUMBER	REV.
E	069-3225	18

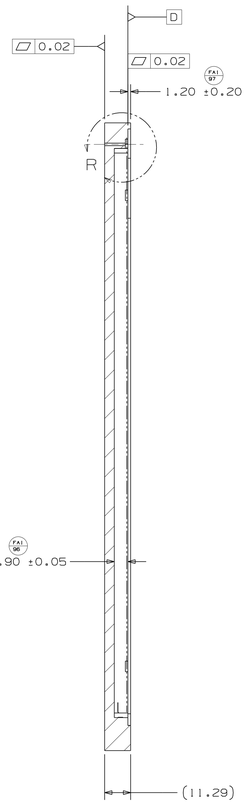
SCALE: NONE SHT 3 OF 5

NOTES: (UNLESS OTHERWISE SPECIFIED)

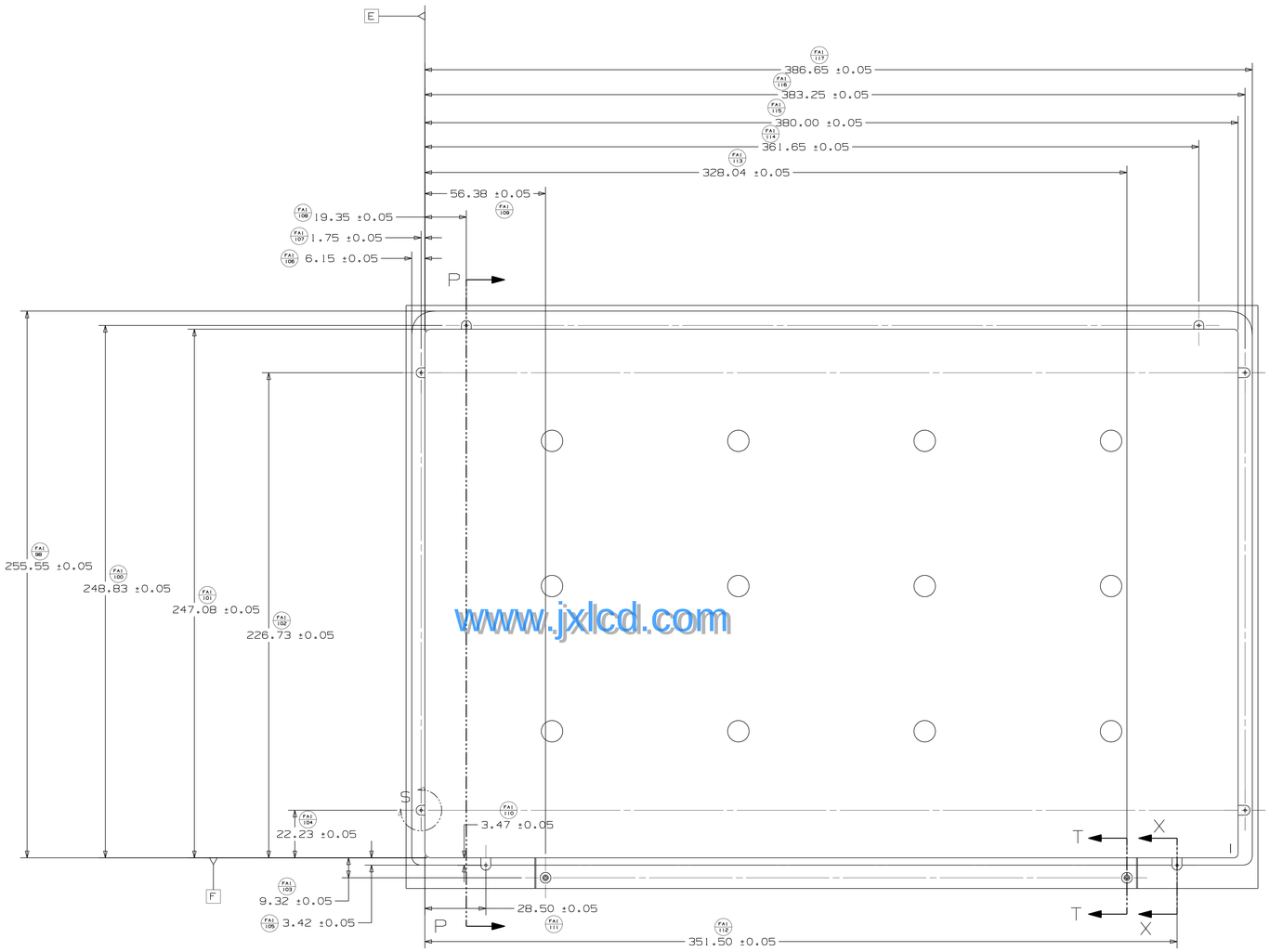
1. MATERIAL: AL 6061 T6
2. INSPECTION FIXTURE AL SURFACES ⌓ 0.05 D E F



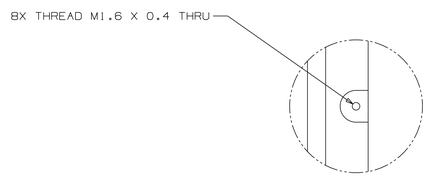
DETAIL R



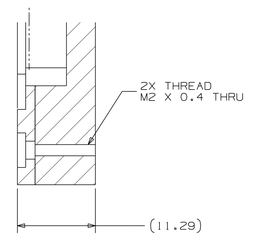
SECTION P-P



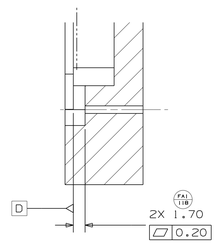
FIXTURE DESIGN GUIDE



DETAIL S



SECTION T-T



SECTION X-X

Apple Inc.

SIZE	DRAWING NUMBER	REV.
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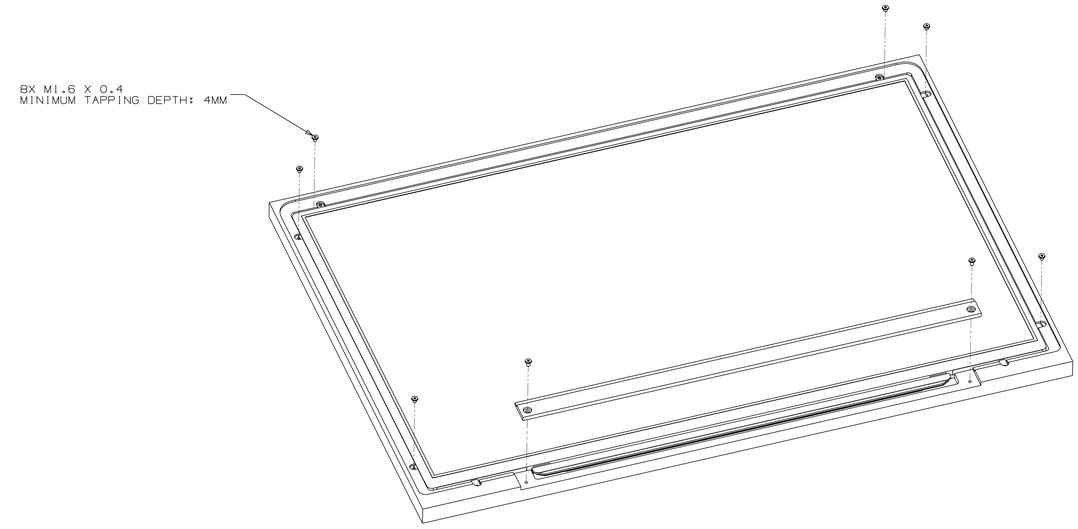

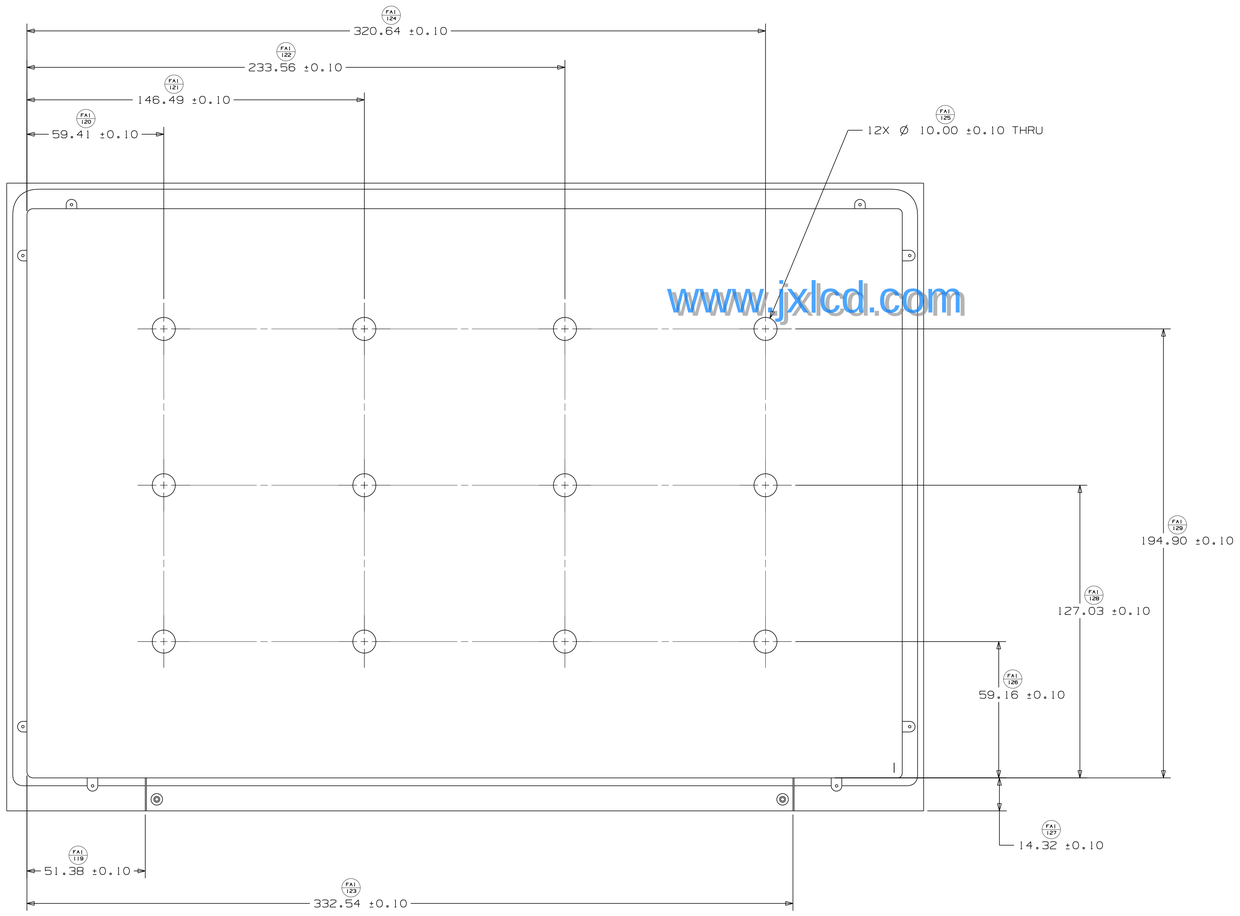

Apple Inc.

SIZE	DRAWING NUMBER	REV.
B	069-3225	18
SCALE: NONE	SHT 5 OF 5	

10. GENERAL PRECAUTIONS

Preliminary

1. Handling

(a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.

(b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and CCFT back-light.

(c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.

(d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(f) The desirable cleaners are water, IPA (Isoprophyl Alcohol) or Hexane.
Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth . In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(h) Protect the module from static , it may cause damage to the C-MOS Gate Array IC.

(i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(j) Do not disassemble the module.

(k) Do not pull or fold the lamp wire.

(l) Do not adjust the variable resistor which is located on the back side.

(m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(n) Pins of I/F connector shall not be touched directly with bare hands.

2. STORAGE

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%.

(b) Do not store the TFT-LCD module in direct sunlight.

(c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

3. OPERATION

(a) Do not connect,disconnect the module in the " Power On" condition.

(b) Power supply should always be turned on/off by following item 6.3 " Power on/off sequence ".

(c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(d) The cable between the back-light connector and its inverter power supply shall be a minimized length and be connected directly . The longer cable between the back-light and the inverter may cause lower luminance of lamp(CCFT) and may require higher startup voltage (Vs).

(e) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, SEC is not to be held reliable for the defective operations. It is strongly recommended to contact SEC to find out fitness for a particular purpose.

4. OTHERS

(a) Ultra-violet ray filter is necessary for outdoor operation.

(b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.

(d) If the module displays the same pattern continuously for a long period of time,it can be the situation when the image "sticks" to the screen.

(e) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

EDID Table (LTN170CT10-G01)			2008.7.03		
Address (Decimal)	Address (HEX)	Field Name & Comments	Value (HEX)	Value (BIN)	Value (DEC)
0	0	Header	00	00000000	0
1	1		FF	11111111	255
2	2		FF	11111111	255
3	3		FF	11111111	255
4	4		FF	11111111	255
5	5		FF	11111111	255
6	6		FF	11111111	255
7	7		00	00000000	0
8	8	EISA Manuf. Code LSB (3 character ID = APP)	06	00000110	6
9	9	Compressed ASCII	10	00010000	16
10	0A	Product Code = 99	99	10011001	153
11	0B	hex, LSB first = 9C	9C	10011100	156
12	0C	32-bit serial #	00	00000000	0
13	0D		00	00000000	0
14	0E		00	00000000	0
15	0F		00	00000000	0
16	10	Week of manufacture (week 1)	01	00000001	1
17	11	Year of manufacture (2009)	13	00010011	19
18	12	EDID Structure Ver # = 1	01	00000001	1
19	13	EDID revision # = 3	03	00000011	3
20	14	Video input definition = Digital input, Non TMDS CRGB	80	10000000	128
21	15	Max H image size = 37 Cm	25	00100101	37
22	16	Max V image size = 23 Cm	17	00010111	23
23	17	Display Gamma = 2.2	78	01111000	120
24	18	Feature support (DPMS) = Active off, RGB color	0A	00001010	10
25	19	Red/green low bits	E5	11100101	229
26	1A	Blue/white low bits	85	10000101	133
27	1B	Red x , Red x = 0.640	A3	10100011	163
28	1C	Red y , Red y = 0.330	54	01010100	84
29	1D	Green x , Green x = 0.310	4F	01001111	79
30	1E	Green y , Green y = 0.610	9C	10011100	156
31	1F	Blue x , Blue x = 0.150	26	00100110	38
32	20	Blue y , Blue y = 0.055	0E	00001110	14
33	21	White x , White x = 0.313	50	01010000	80
34	22	White y , White y = 0.329	54	01010100	84
35	23	Established timing 1	00	00000000	0
36	24	Established timing 2	00	00000000	0
37	25	Manufacturer's timings	00	00000000	0
38	26	Standard timing #1 was not used	01	00000001	1
39	27		01	00000001	1
40	28	Standard timing #2 was not used	01	00000001	1
41	29		01	00000001	1
42	2A	Standard timing #3 was not used	01	00000001	1
43	2B		01	00000001	1
44	2C	Standard timing #4 was not used	01	00000001	1
45	2D		01	00000001	1
46	2E	Standard timing #5 was not used	01	00000001	1
47	2F		01	00000001	1
48	30	Standard timing #6 was not used	01	00000001	1
49	31		01	00000001	1
50	32	Standard timing #7 was not used	01	00000001	1
51	33		01	00000001	1
52	34	Standard timing #8 was not used	01	00000001	1
53	35		01	00000001	1

EDID Table (LTN170CT10-G01)			2008.7.03		
Address (Decimal)	Address (HEX)	Field Name & Comments	Value (HEX)	Value (BIN)	Value (DEC)
54	36	Pixel Clock/10,000 (LSB) => main clock = 154.00MHz	28	00101000	40
55	37	Pixel Clock/10,000 (MSB) / 1920 x 1200 @ 60Hz pixel clock = 78.97MHz	3C	00111100	60
56	38	Horizontal Active = 1920 pixels	80	10000000	128
57	39	Horizontal Blanking = 160 pixels	A0	10100000	160
58	3A	Horizontal Active : Horizontal Blanking	70	01110000	112
59	3B	Vertical Avtive = 1200 lines	B0	10110000	176
60	3C	Vertical Blanking = 35 lines	23	00100011	35
61	3D	Vertical Active : Vertical Blanking	40	01000000	64
62	3E	Horizontal Sync. Offset = 48 pixels	30	00110000	48
63	3F	Horizontal Sync Pulse Width = 32 pixels	20	00100000	32
64	40	Vertical Sync Offset = 3 lines : Sync Width = 6 lines	36	00110110	54
65	41	Horizontal Vertical Sync Offset/Width upper 2bits = 0	00	00000000	0
66	42	Horizontal Image Size = 36.7cm(367)	6F	01101111	111
67	43	Vertical Image Size = 22.9cm(230)	E6	11100110	230
68	44	Horizontal & Vertical Image Size	10	00010000	16
69	45	Horizontal Border = 0	00	00000000	0
70	46	Vertical Border = 0	00	00000000	0
71	47	Non-interlaced,Normal display,no stereo,Digital separate sync,H/V pol negatives	19	00011001	25
72	48	Detailed timing/monitor	00	00000000	0
73	49	descriptor #3	00	00000000	0
74	4A		00	00000000	0
75	4B		01	00000001	1
76	4C	Version	00	00000000	0
77	4D	Apple edid signature	06	00000110	6
78	4E	Apple edid signature	10	00010000	16
79	4F	Link Type (LVDS Link,MSB justified)	30	00110000	48
80	50	Pixel and link component format (6-bit panel interface)	00	00000000	0
81	51	Panel features (No inverter)	00	00000000	0
82	52		00	00000000	0
83	53		00	00000000	0
84	54		00	00000000	0
85	55		00	00000000	0
86	56		00	00000000	0
87	57		00	00000000	0
88	58		0A	00001010	10
89	59		20	00100000	32
90	5A	Detailed timing/monitor	00	00000000	0
91	5B	descriptor #3	00	00000000	0
92	5C	LTN170CT10-G01	00	00000000	0
93	5D		FE	11111110	254
94	5E		00	00000000	0
95	5F	L	4C	01001100	76
96	60	T	54	01010100	84
97	61	N	4E	01001110	78
98	62	1	31	00110001	49
99	63	7	37	00110111	55
100	64	0	30	00110000	48
101	65	C	43	01000011	67
102	66	T	54	01010100	84
103	67	1	31	00110001	49
104	68	0	30	00110000	48
105	69		00	00000000	0
106	6A		0A	00001010	10
107	6B		20	00100000	32

EDID Table (LTN170CT10-G01)				2008.7.03	
Address (Decimal)	Address (HEX)	Field Name & Comments	Value (HEX)	Value (BIN)	Value (DEC)
108	6C	Detailed timing/monitor	00	00000000	0
109	6D	descriptor #4	00	00000000	0
110	6E	Color LCD	00	00000000	0
111	6F		FC	11111100	252
112	70		00	00000000	0
113	71	C	43	01000011	67
114	72	o	6F	01101111	111
115	73	l	6C	01101100	108
116	74	o	6F	01101111	111
117	75	r	72	01110010	114
118	76	space	20	00100000	32
119	77	L	4C	01001100	76
120	78	C	43	01000011	67
121	79	D	44	01000100	68
122	7A		0A	00001010	10
123	7B		20	00100000	32
124	7C		20	00100000	32
125	7D		20	00100000	32
126	7E	Extension Flag = 00	00	00000000	0
127	7F	Checksum	B7	10110111	183