LITEON®
OPTOELECTRONICS

Optical Sensor
Product Data Sheet
LTR-778ALS-BE

Spec No. :DS86-2018-0014
Effective Date: 05/18/2018
Revision: -

LITE-ON DCC

RELEASE

BNS-OD-FC001/A4

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OPTICAL SENSOR
LTR-778ALS-BE

Description

The LTR-778ALS-BE is an integrated low voltage I2C digital light sensor [ALS] and proximity sensor [PS] with built-in emitter, in a single miniature chipled lead-free surface mount package. This sensor converts light intensity to a digital output signal capable of direct I2C interface. It provides a linear response over a wide dynamic range (0.005 lux to 12k lux) and is well suited to applications under high ambient brightness. With built-in proximity sensor (VCSEL emitter and detector), LTR-778ALS-BE offers the feature to detect object at a user configurable distance. This sensor features 2-level fault detection that allows further protection against un-intended VCSEL current trigger or surge caused by short circuit.

The sensor supports an interrupt feature that removes the need to poll the sensor for a reading which improves system efficiency. The sensor also supports several features that help to minimize the occurrence of false triggering. This CMOS design and factory-set one time trimming capability ensure minimal sensor-to-sensor variations for ease of manufacturability to the end customers.

Application

To control display backlight and/or object detection in

- Back-lighting Control in mobile/portable devices
- Touch Panel Control in mobile/portable devices

Features

- I2C interface (Fast Mode: 400kbit/s)
- Ultra-small ChipLed package
- Built-in temperature compensation circuit
- Low active power consumption with standby mode
- Supply voltage range from 2.7V to 3.6V capable of 1.7V logic voltage
- Operating temperature range from -30 ºC to +70ºC
- RoHS and Halogen free compliant
- **Light Sensor**
  - Close to human eye spectral response
  - Immunity to IR / UV Light Source
  - Automatically rejects 50 / 60 Hz lightings flicker
  - 6 dynamic ranges (ALS gain settings)
  - 16-bit effective resolution
- **Proximity Sensor**
  - Built-in VCSEL driver, VCSEL emitter and detector with 2-level fault detection for VCSEL.
  - Programmable VCSEL drive settings
  - 11-bit effective resolution
  - High ambient light suppression
  - PS offset capability to cancel cross-talk

Ordering Information

Part Number	Packaging Type	Package	Quantity
LTR-778ALS-BE	Tape and Reel	8-pins Chip-Led package	8000

OPTICAL SENSOR
LTR-778ALS-BE

1. Outline Dimensions and Pins Configuration

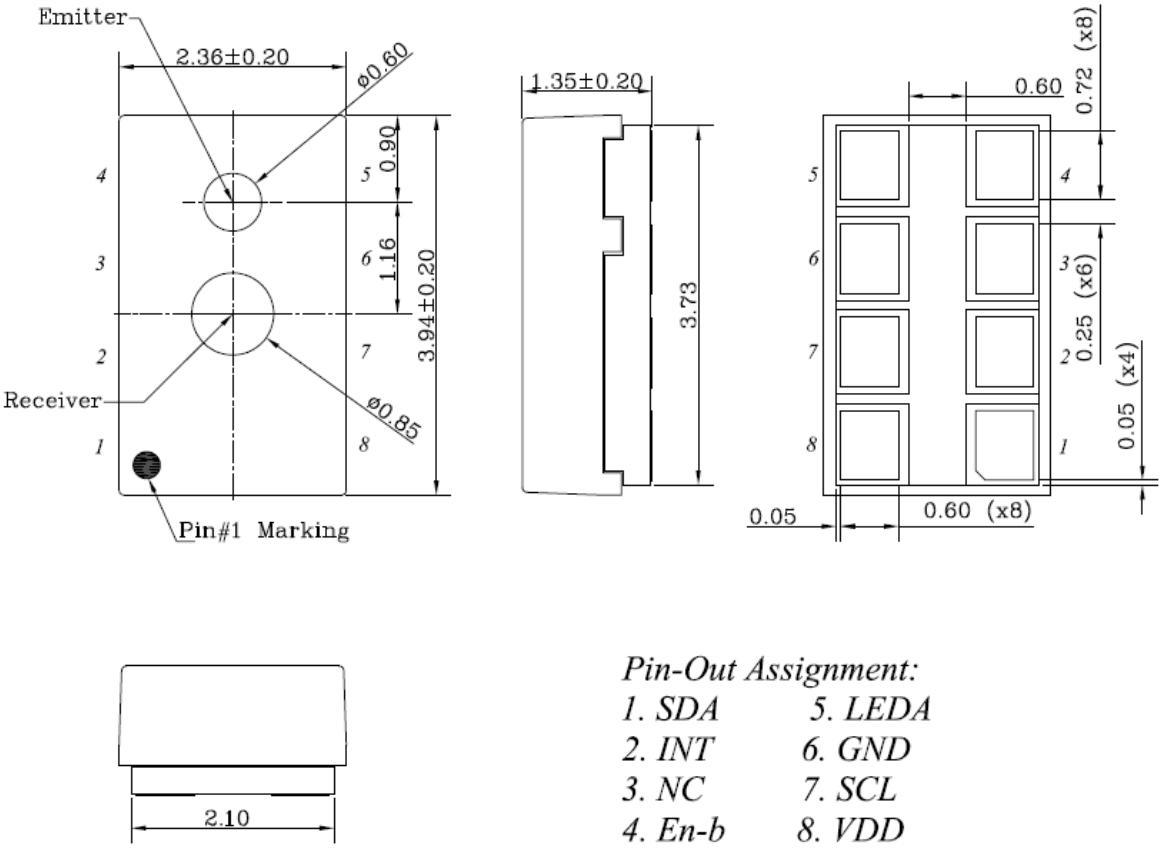
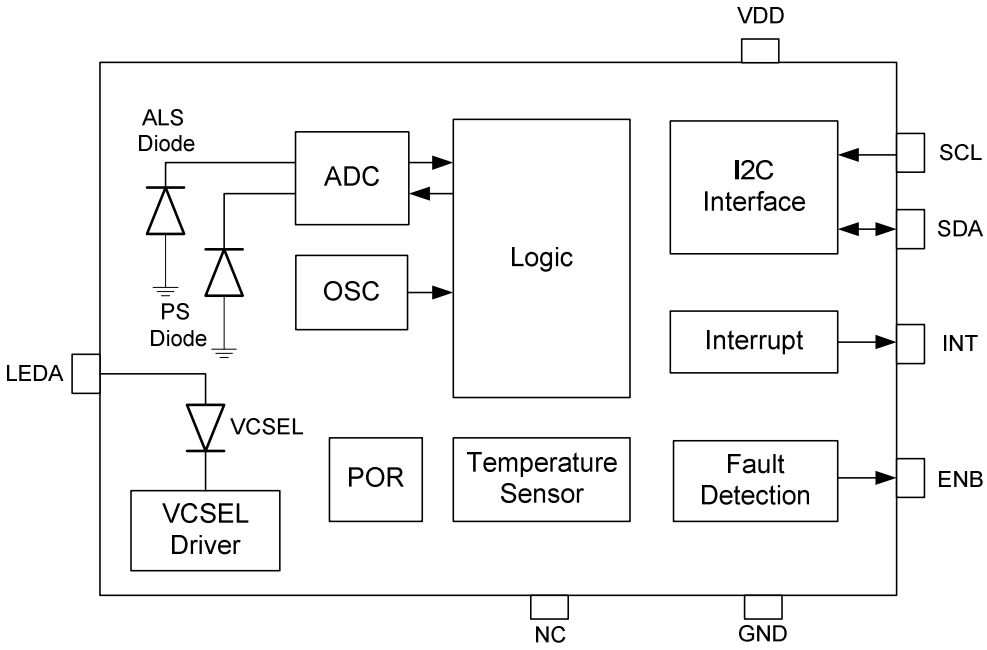


Figure 1 : Outline Dimensions and Pins

Note:

1. All dimensions are in millimeters

2. Functional Block Diagram



The LTR-778ALS provides an All-In-One solution for Ambient Light sensing and Proximity sensing by incorporating a Visible plus IR photodiode (Ch0) & a Visible-Only photodiode (Ch1), an on-board VCSEL emitter, Integrating ADCs, Oscillator, Control Logics, LED Driver, Interrupt Output and an I2C Interface, all in a single ChipLED module.

The Integrating ADCs convert the photodiode current to a digital value, providing up to 16-bits of resolution for Ambient light sensing and 11-bits of data for Proximity sensing. Separate ADCs ensure that conversion time is kept to the minimum. Once the ADC conversion cycle is completed, the result is transferred to the respective data registers. Data registers can then be read by a microprocessor via I2C (up to Fast mode of 400 kHz) for processing.

For Ambient light sensing, the illuminance in Lux can be derived from the ADC data using an empirical formula to approximate the human eye response. For Proximity sensing, the generated ADC count is a representation of object detection at various distances. An on-board 850nm VCSEL emitter provides the pulses required for Proximity sensing.

The Interrupt Output option ensures that consumption of the microprocessor's resource is kept to minimum as it alleviates the need of the microprocessor polling the LTR-778ALS for data. When the user-programmable interrupt thresholds are set, the Interrupt pin (INT) will output a level-type Interrupt signal when these thresholds are exceeded. Persistency control registers are also available for user to program the level of persistence required for the Interrupt.

An internal oscillator generates a 1.31MHz (typical) clock. Timing related settings are generated from the internal clock.

On-chip temperature compensation is designed to account for the VCSEL's output power temperature characteristics, where,

VCSEL_Power = (VCSEL_Current – Threshold_Current) x VCSEL_Power_Efficiency

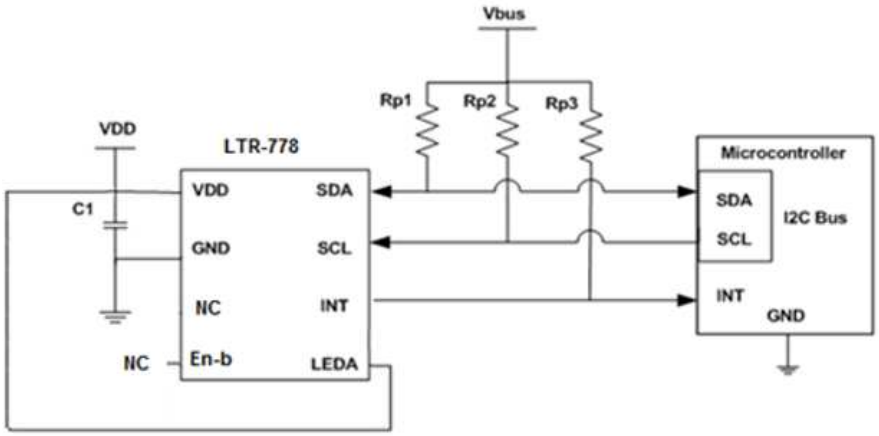
The temperature compensation of the PS works by considering the Power vs temperature characteristics of the VCSEL and the photodiode conversion efficiency. The VCSEL_Current temperature of the VCSEL driver and internally generated reference current (Iref) temperature characteristics are then designed to compensate for the VCSEL and photodiode conversion efficiency temperature characteristics.

Fault detection feature is incorporated to ensure power to the VCSEL can be turned off or generate an Interrupt when conditions that may increase the output power of the VCSEL beyond eye-safety limit is detected.

POR (Power-On-Reset) ensures the digital logic controller is properly reset upon power on of the supply.

3. Application Circuit

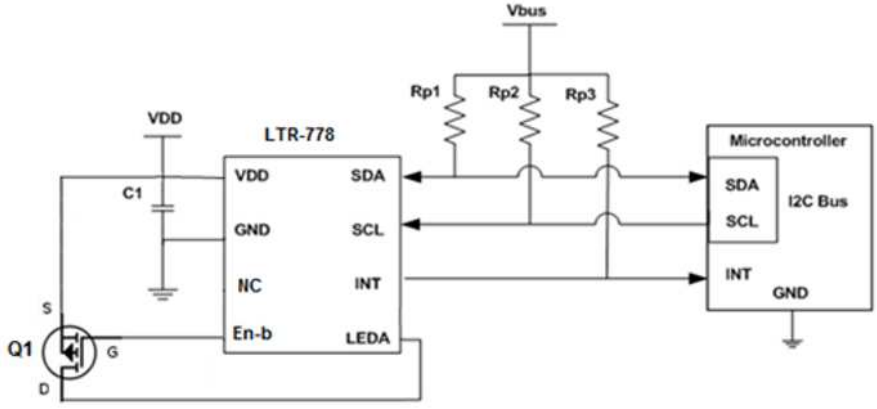
3.1 For Level 1 VCSEL Fault Detection implementation :



Recommended Application Circuit Components

Component	Recommended Value
Rp1, Rp2, Rp3 [1]	1 kΩ to 10 kΩ
C1	1uF ± 20%, X7R Ceramic

3.2 For Level 1 & Level 2 (Full Levels) VCSEL Fault Detection implementation :



Recommended Application Circuit Components

Component	Recommended Value
Rp1, Rp2, Rp3 [1]	1 kΩ to 10 kΩ
C1	1uF ± 20%, X7R Ceramic
Q1	External PMOS transistor Ron<0.45Ω@VGS = −2.7V, Cin≤150pF, Example : NTA4151PT1G

Notes: [1] Selection of pull-up resistors value is dependent on bus capacitance values. For more details, please refer to I2C Specifications: http://www.nxp.com/documents/user_manual/UM10204.pdf

I/O Pins Configuration Table

Pin	I/O Type	Symbol	Description
1	IN/OUT	SDA	I^2C serial data.
2	OUT	INT	Level Interrupt Pin. This pin is an open drain output.
3	NC	NC	No Connect.
4	OUT	En-b	Controlling external power switch for fault detection use. This is a digital output pin (not open drain). Under normal operation this output pin will be at logic low so as to turn on the external PMOS switch which is connected to the VCSEL. When fault is detected this output pin will be at logic high and will shutdown the external PMOS and also the VCSEL.
5	IN	LED A	VCSEL LED Anode.
6	Ground	GND	Ground
7	IN	SCL	I^2C serial clock.
8	Supply	VDD	Power Supply Voltage

4. Rating and Specification

4.1 Absolute Maximum Rating at Ta=25℃

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	3.8	V
Digital Voltage Range	SCL, SDA, INT	-0.5 to 3.8	V
Digital Output Current	SCL, SDA, INT	-1 to 20	mA
Storage Temperature	T_{stg}	-40 to 85	°C
VCSEL Forward DC Current	I_f	15	mA
Electrostatic Discharge Protection (Human Body Model JESD22-A114)[1]	V_{HBM}	2000	V

Notes:

[1] V_{HBM} for LEDA PAD is 200V due to VCSEL behavior.

Exceeding these ratings could cause damage to the sensor. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

4.2 Recommended Operating Conditions (VDD= 3V, Ta = +25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	2.7		3.6	V
Interface Bus Power Supply Voltage	VIO	1.7		3.6	V
I2C Bus Input Pin High Voltage	VIH_SCL, VIH _SDA	1.2			V
I2C Bus Input Pin Low Voltage	VIL_SCL, VIL_SDA			0.6	V
Operating Temperature	T_{ope}	-30		70	°C

4.3 Electrical & Optical Specifications

All specifications are at VDD = 3.0V, T_{ope} = 25°C, unless otherwise noted.

Parameter	Min.	Typ.	Max.	Unit	Condition
Supply Current		150		uA	ALS & PS both in active mode ALS integration time = 100ms ALS measurement repeat rate = 400ms (Excluding VCSEL current)
Standby Current			5	uA	Standby / Sleep Mode
Initial Startup Time			50	ms	Min wait time after power up (supply ramp-up to 2.4V) before sending I2C commands
Wakeup Time from Standby			10	ms	Max wait time after turning device from stand-by to active before measurements starts
Leakage Current	-5		5	uA	SDA, SCL, INT pins

4.4 Characteristics Ambient Light Sensor

Parameter	Min.	Typ.	Max.	Unit	Condition
ALS Resolution		16		bit	
Full ADC count			65535	count	Full Scale ADC Count
Dark Count			5	count	Lux = 0
ADC Count		44k		count	CH0 Lux=100 White LED Gain 128X
ALS Lux Accuracy	-15		+15	%	
Min. Integration time	50		400	ms	With 50/60Hz Rejection
50/60 Hz flicker noise error		5		%	

4.5 Characteristics Proximity Sensor

Parameter	Min.	Typ.	Max.	Unit	Condition
PS Resolution		11 bit			
Full ADC count			2047	count	
Detection Distance		100		mm	6mA, 48 pulses, 18% Gray Card
No of VCSEL Pulse	1		64	pulses	
Peak Wavelength, λP	840	850	860	nm	IF = 9mA
Ambient Light Suppression			50k	lux	Direct Sunlight

4.6 Typical Device Parameter
(VDD = 3.0V, Ta=25℃, default power-up settings, un less otherwise noted)

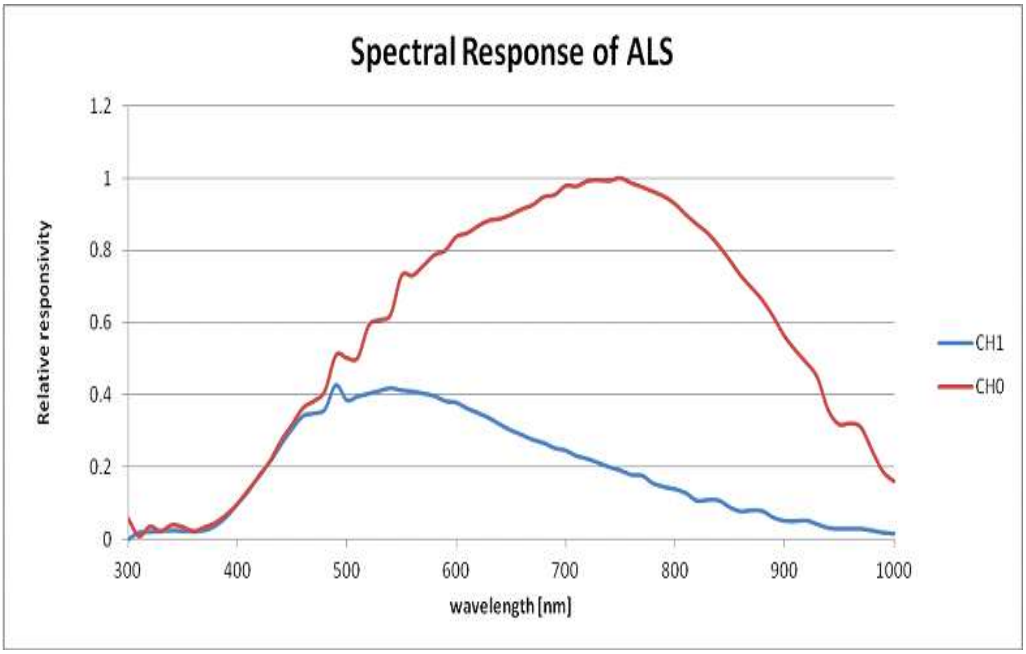


Figure 4.6.1 : Spectral response for ALS

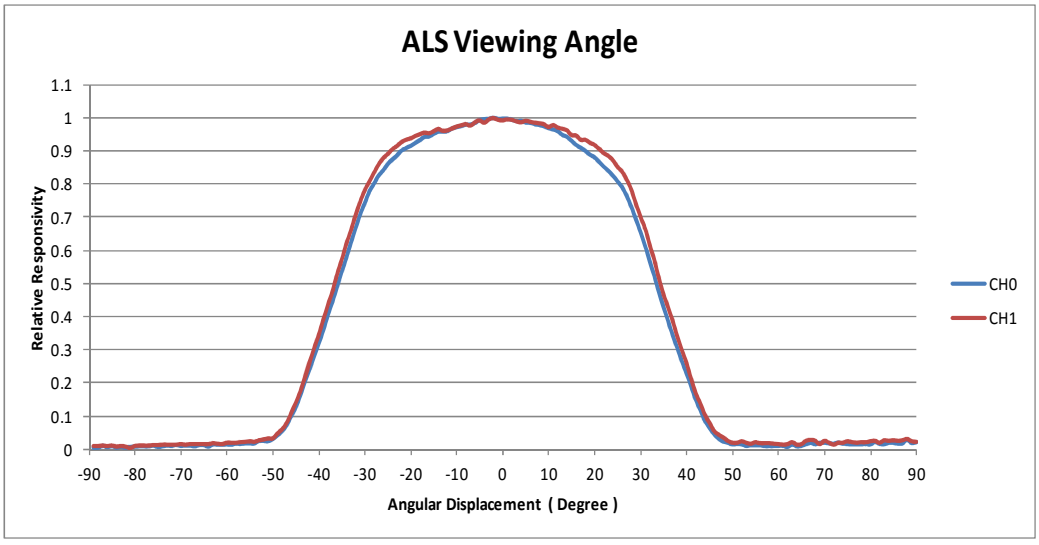


Figure 4.6.2 Viewing angle of ALS

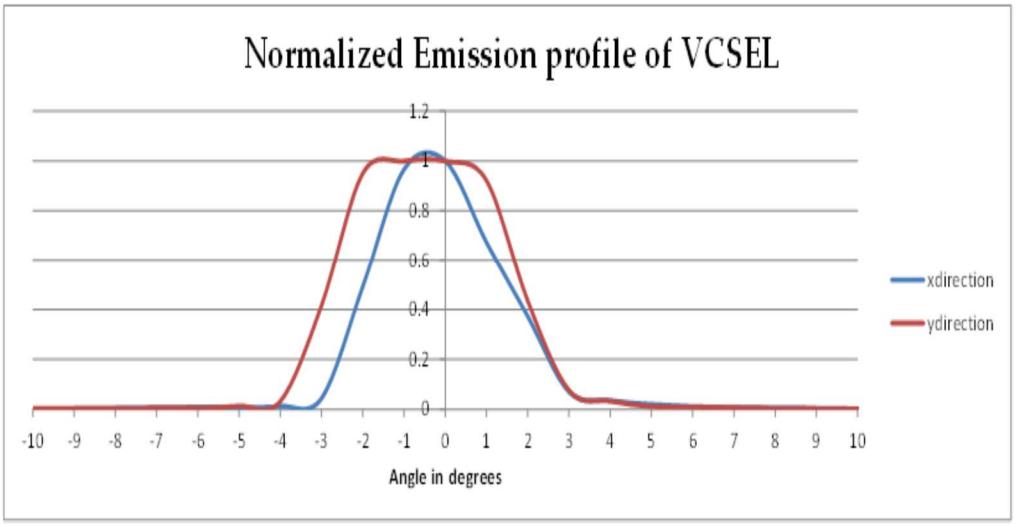
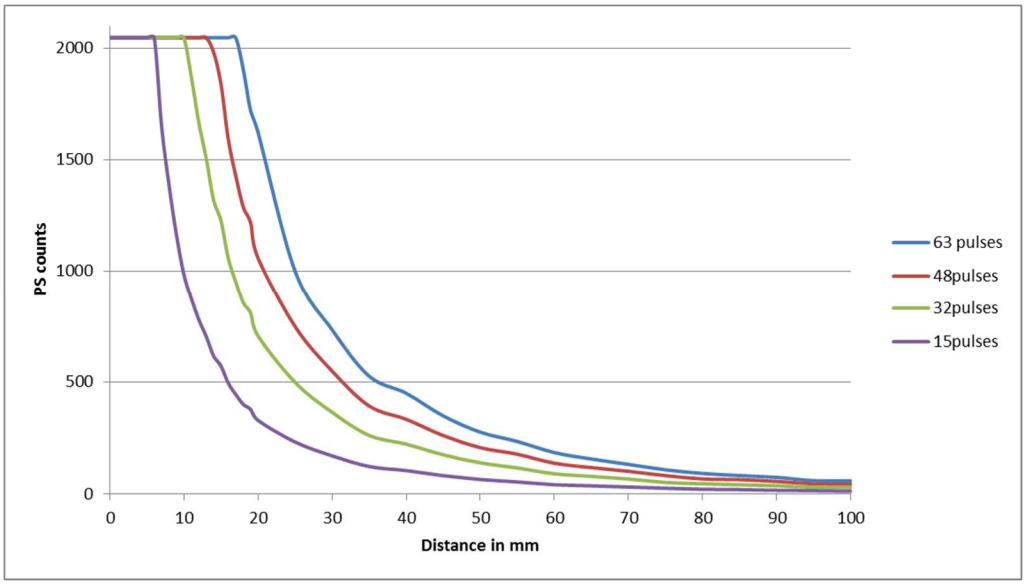


Figure 4.6.3 VCSEL Angular of incidence



PS settings: 6mA & various pulses count.

Figure 4.6.4 PS count Vs distance (without window under 18% gray card)

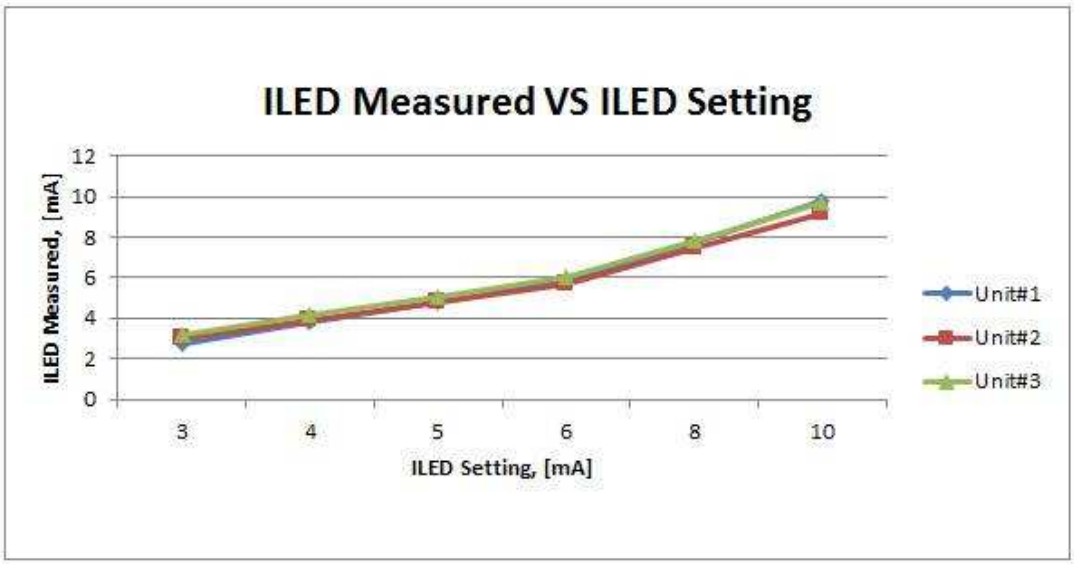
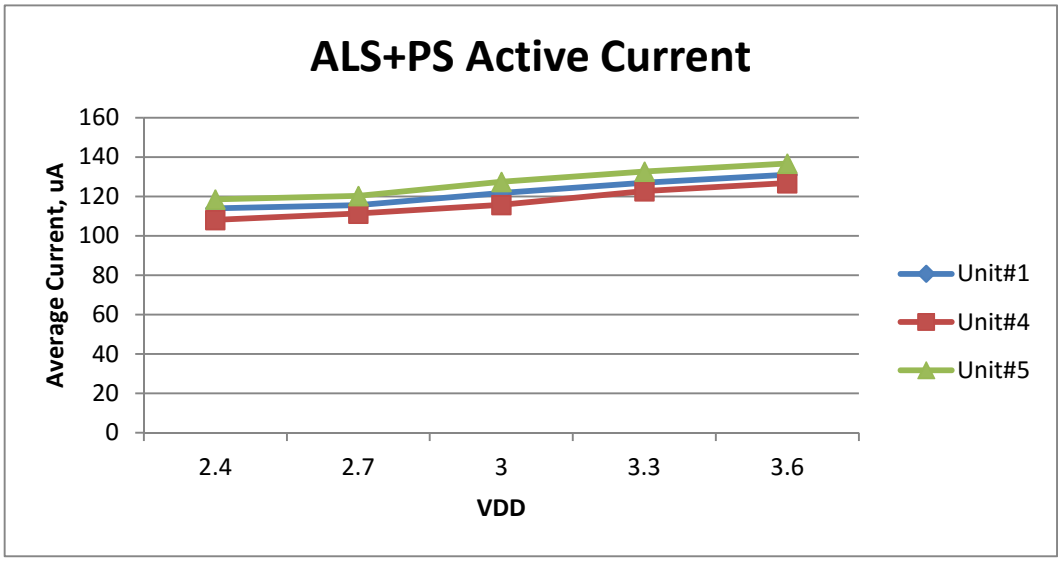


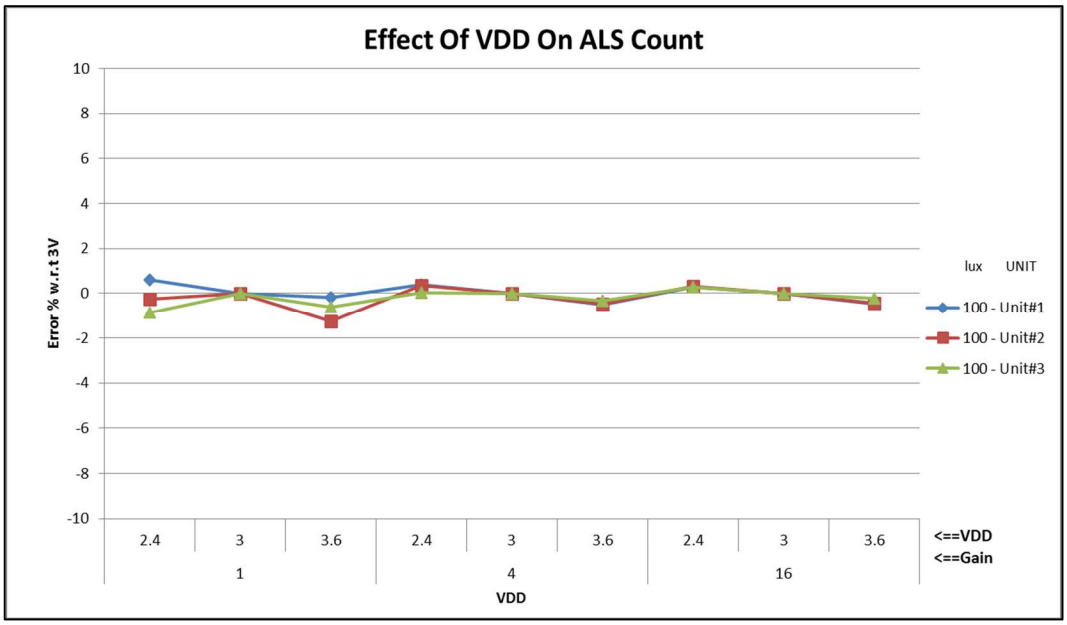
Figure 4.6.5 : LED Current measurement vs VCSEL settings at register 0x82.



PS Settings: 8mA, 15 pulse, 25%DC, 100ms Measurement rate

ALS Settings: Default settings (100ms Integration time, 400ms Measurement rate)

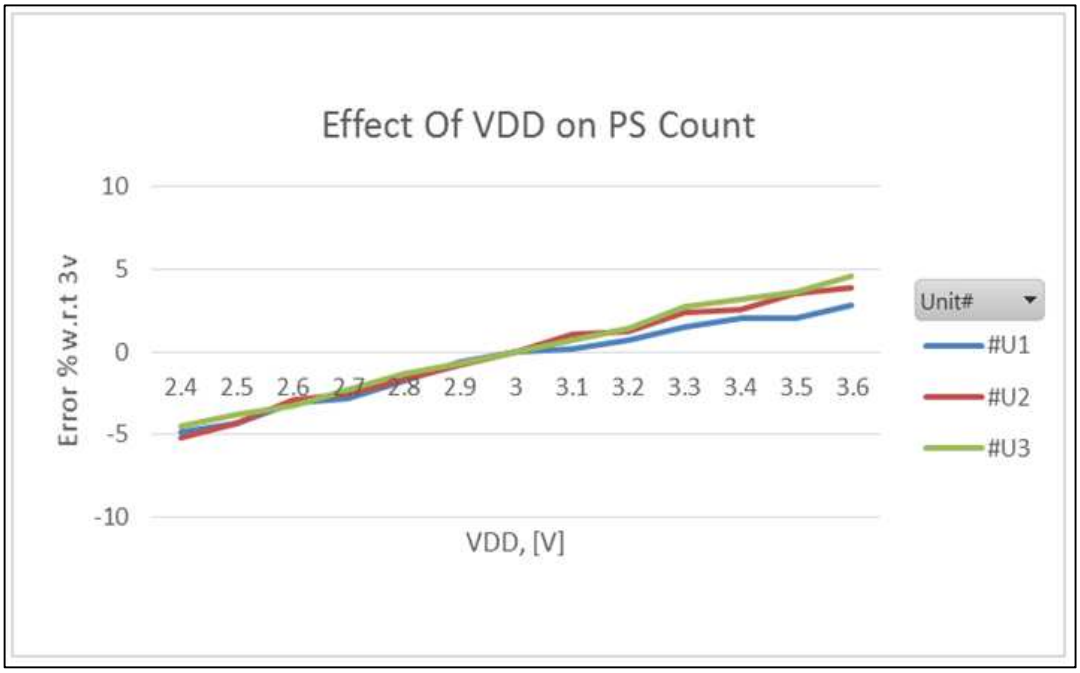
Figure 4.6.6 : ALS + PS enabled active current over supply voltage.



ALS Settings: Gain X1, X4, X16, 100ms Integration time

with white LED light source at 100Lux .

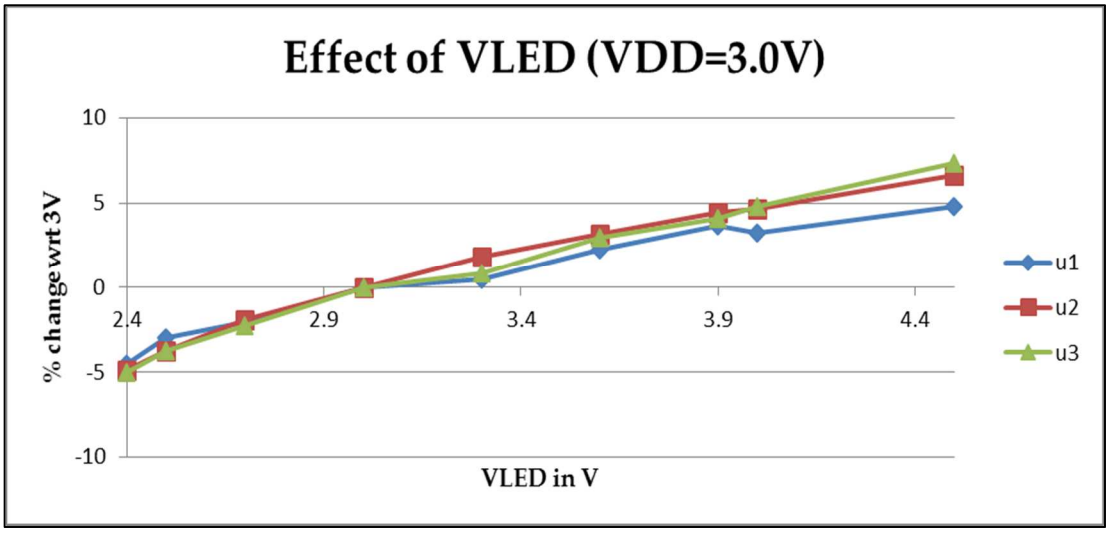
Figure 4.6.7 : PS count variation over supply voltage.



PS Settings: 6mA, 32pulse, 25%DC, VLED 3.0V, 100ms Measurement rate

with grey card as object at 3cm.

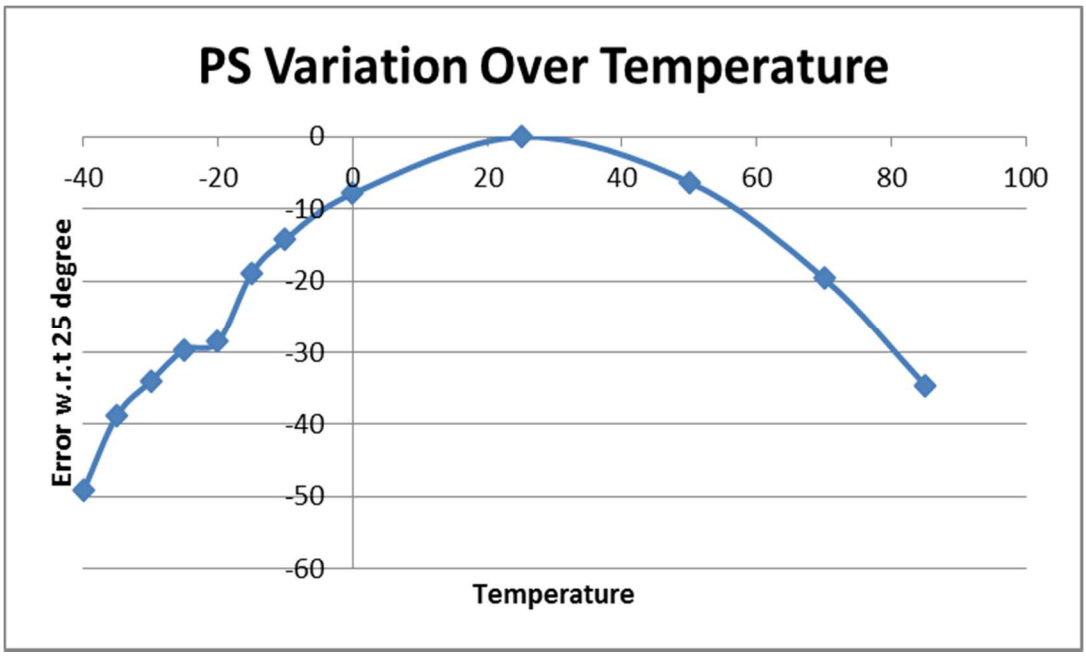
Figure 4.6.8 : PS count variation over supply voltage.



PS Settings: 6mA, 32pulse, 25%DC, VDD 3.0V, 100ms Measurement rate

with grey card as object at 3cm.

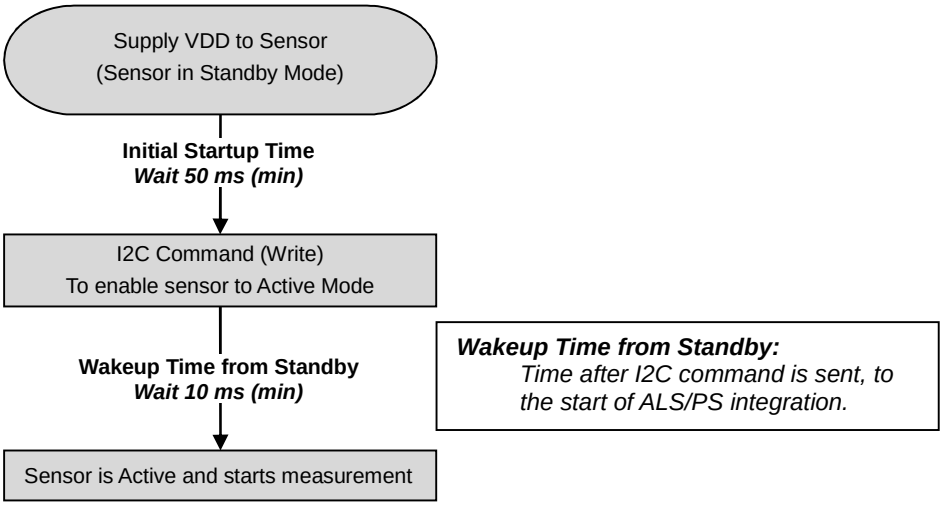
Figure 4.6.9 : PS count variation over LED supply voltage.



PS Setting: 6mA, 32pulse, 25%DC, VDD 3.0V, 100ms Measurement rate

Figure 4.6.10 : PS count variation over temperature.

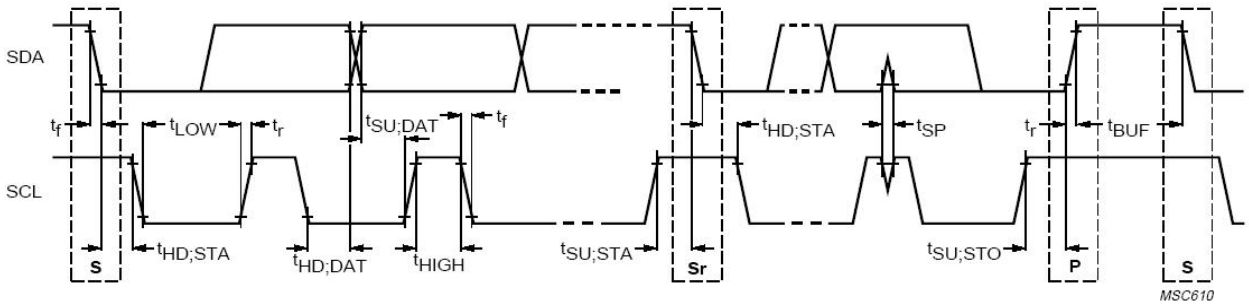
4.7 Startup Sequence



4.8 AC Electrical Characteristics

All specifications are at V_{DD} = 3.0V, T_{ope} = 25°C, unless otherwise noted.

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	1	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1.3		us
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6		us
LOW period of the SCL clock	t_{LOW}	1.3		us
HIGH period of the SCL clock	t_{HIGH}	0.6		us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6		us
Set-up time for STOP condition	$t_{SU;STO}$	0.6		us
Rise time of both SDA and SCL signals	t_r	30	300	ns
Fall time of both SDA and SCL signals	t_f	30	300	ns
Data hold time	$t_{HD;DAT}$	30		s
Data setup time	$t_{SU;DAT}$	100		ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns

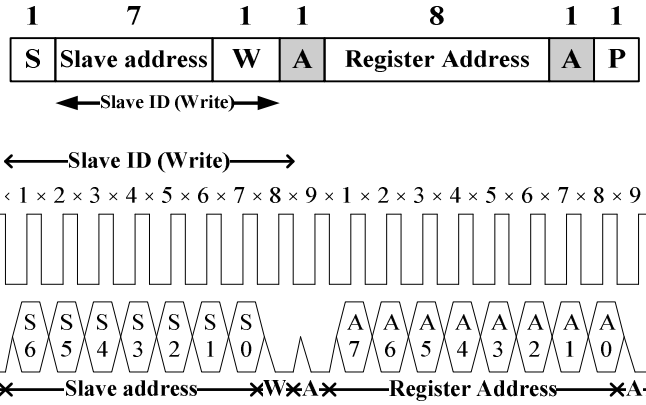


Definition of timing for I²C bus

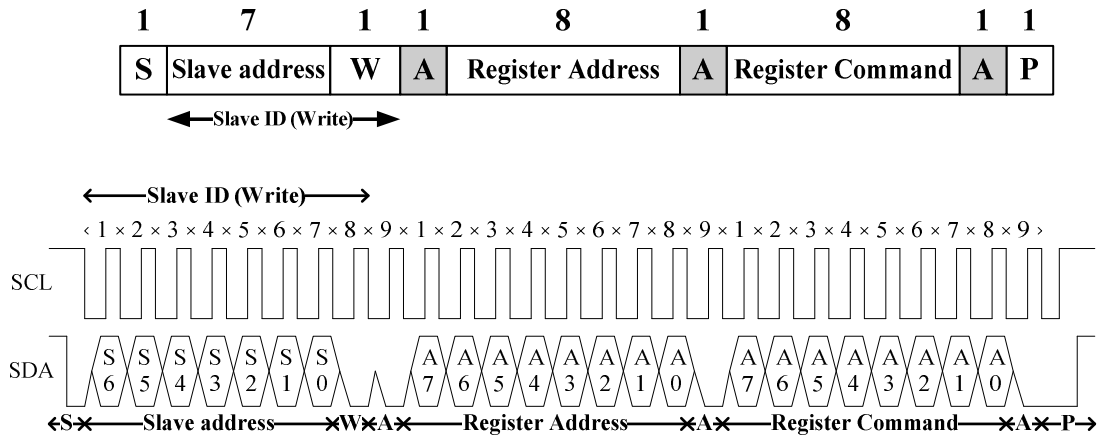
5. Principle of Operation

5.1 I2C Protocol

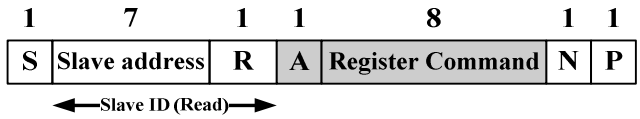
5.1.1 I2C Write Protocol (type 1)

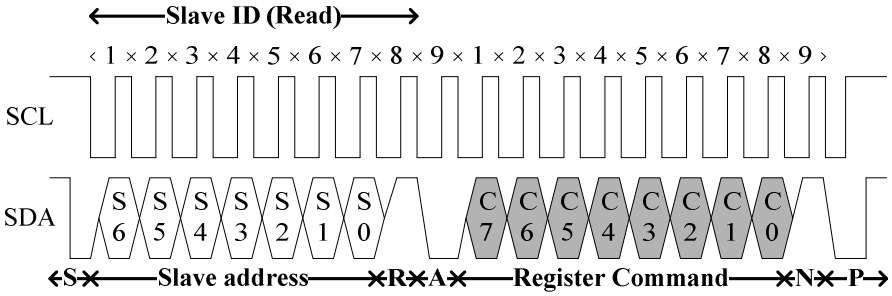


5.1.2 I2C Write Protocol (type 2)



5.1.3 I2C Read Protocol





A	Acknowledge (0 for an ACK)	**N**	Non-Acknowledge(1 for an NACK)
S	Start condition	**Sr**	Repeated Start condition
P	Stop condition		
W	Write (0 for writing)	**R**	Read (1 for read)
	Slave-to-master	□	Master-to-Slave

5.2 I2C Slave Address

The 7 bits slave address for this sensor is 0x23H. A read/write bit should be appended to the slave address by the master device to properly communicate with the sensor.

I²C Slave Address									
Command Type	(0x23H)							(0x23H)	(0x23H)
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Write	0	1	0	0	0	1	1	0	0x46H
Read	0	1	0	0	0	1	1	1	0x47H

6. Register Set

Address	R / W	Register Name	Description	Reset Value
0x80	R / W	ALS_CONTR	ALS operation mode control SW reset	0x00
0x81	R / W	PS_CONTR	PS operation mode control	0x40
0x82	R / W	PS_VCSEL	PS VCSEL setting	0x76
0x83	R / W	PS_N_PULSES	PS number of pulses	0x01
0x84	R / W	PS_MEAS_RATE	PS measurement rate in active mode	0x04
0x85	R / W	ALS_MEAS_RATE	ALS measurement rate in active mode	0x0B
0x86	R	PART_ID	Part Number ID and Revision ID	0x05
0x87	R	MANUFAC_ID	Manufacturer ID	0x05
0x88	R	ALS_DATA _CH1_0	ALS CH1 measurement data, lower byte	0x00
0x89	R	ALS_DATA_CH1_1	ALS CH1 measurement data, upper byte	0x00
0x8A	R	ALS_DATA _CH0_0	ALS CH0 measurement data, lower byte	0x00
0x8B	R	ALS_DATA_CH0_1	ALS CH0 measurement data, upper byte	0x00
0x90	R	ALS_PS_STATUS	ALS and PS new data status	0x00
0x91	R	PS_DATA_0	PS measurement data, lower byte	0x00
0x92	R	PS_DATA_1	PS measurement data, upper byte	0x00
0x93	R / W	INTERRUPT	Interrupt settings	0x00
0x94	R / W	INTERTUPT_PERSIST	PS and ALS interrupt persist setting	0x00
0x95	R / W	PS_THRES_UP_0	PS interrupt upper threshold, lower byte	0xFF
0x96	R / W	PS_THRES_UP_1	PS interrupt upper threshold, upper byte	0x07
0x97	R / W	PS_THRES_LOW_0	PS interrupt lower threshold, lower byte	0x00
0x98	R / W	PS_THRES_LOW_1	PS interrupt lower threshold, upper byte	0x00
0x99	R / W	PS_OFFSET_LSB	PS offset, lower byte	0x00
0x9A	R / W	PS_OFFSET_MSB	PS offset, upper byte	0x00
0x9B	R / W	ALS_THRES_UP_0	ALS interrupt upper threshold, lower byte	0xFF
0x9C	R / W	ALS_THRES_UP_1	ALS interrupt upper threshold, upper byte	0xFF
0x9D	R / W	ALS_THRES_LOW_0	ALS interrupt lower threshold, lower byte	0x00
0x9E	R / W	ALS_THRES_LOW_1	ALS interrupt lower threshold, upper byte	0x00
0x9F	R / W	FD_CONTR	Fault detection control and status register	0x00
0xA0	R	FD STATUS	Fault detection status	0x00

6.1 ALS_CONTR Register (0x80)

The ALS_CONTR register controls the ALS Gain setting, ALS operation modes and software (SW) reset for the sensor. The ALS sensor can be set to either standby mode or active mode. At either of these modes, the I^2C circuitry is always active. The default mode after power up is standby mode. During standby mode, there is no ALS measurement performed but I^2C communication is allowed to enable read/write to all the registers.

Internal OSC is disabled at standby mode, and can only be enabled by either ALS active mode or/and PS active mode. However, ON_CLOCK control bit can be set to logic "1" to force OSC enabled regardless ALS and PS mode.

SW_Reset is used to reset all the control register to default value and internal state machine and control block to original state.

The ALS gain is ranged from 1x to 256x (up to 6 steps). The gain can be selected to achieve the required dynamic range.

0x80	ALS_CONTR (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved		*ON CLOCK*	*ALS Gain*			*SW Reset*	*ALS Mode*

Field	Bits	Default	Type	Description	
Reserved	7:6	00	--	--	Reserved
ON CLOCK	5	0	RW	0	System clock off (default)
				1	System clock on. This is used in conjunction with FD (Fault Detection). Enable bit in register 0x9F to enable fault checking while PS is in the disable state.
ALS Gain	4:2	000	RW	000	Gain 1x(default)
				001	Gain 4x
				010	Gain 16x
				011	Gain 64x
				100	Gain 128x
				101	Gain 256x
				110	Reserved
				111	Reserved
SW Reset	1	0	RW	0	Initial start-up procedure is NOT started (default)
				1	Initial start-up procedure is started, bit has default value of 0 after start-up
ALS Mode	0	0	RW	0	Stand-by mode (default)
				1	Active mode

6.2 PS _CONTR Register (0x81)

The PS_CONTR register controls the PS operation modes. The PS sensor can be set to either standby mode or active mode. At either of these modes, the I^2C circuitry is always active. The default mode after power up is standby mode. During standby mode, there is no PS measurement performed but I^2C communication is allowed to enable read/write to all the registers.

FarToNear(FTN) / NearToFar(NTF) EN controls the FTN/NTF Status Reporting. When FTN/NTF_EN is set, the PS counts will be compared with the PS threshold limits to detect FTN & NTF status.

The PS OFFSET ENABLE allows the PS DATA register to be subtracted with the PS OFFSET data for the purpose of offsetting cross-talk. This will prevent the useful detectable range from saturation.

0x81	PS_CONTR (default = 0x40)							
	B7	B6	B5	B4	B3	B2	B1	B0
	PS OFFSET ENABLE	*Reserved*	*FTN/NTF EN*	*Reserved*			*PS Mode*	*Reserved*

Field	Bits	Default	Type	Description	
PS OFFSET ENABLE	7	0	R/W	0	PS OFFSET disabled
				1	PS OFFSET enabled. PS OFFSET data will be subtracted from PS DATA register.
Reserved	6	1	R/W	--	Must be write 1
FTN/NTF_EN	5	0	R/W	0	Disable FTN/NTF Status Reporting(default)
				1	Enable FTN/NTF Status Reporting
Reserved	4:2	000	R/W	--	Must be write 0
PS Mode	1	0	R/W	1	Active Mode
				0	Stand-by Mode(default)
Reserved	0	0	--	--	Reserved

6.3 PS_VCSEL Register(0x82)

The PS_VCSEL register controls VCSEL peak current. The VCSEL current settings ranged from 3mA to 15mA (up to 13 steps).

Figure 6.3.1 and 6.3.2 show the block diagram & relationship of VCSEL current to the change of PS data, corresponding to the internal clock 1.3MHz (typical).

In short, PS data rate of change is [LED-2mA]/[LEDref-2mA] (i.e. 4mA->6mA, [6-2]/[4-2], means 2X relative increase in PS data). The VCSEL used needs about 2mA of current to start emitting light power.

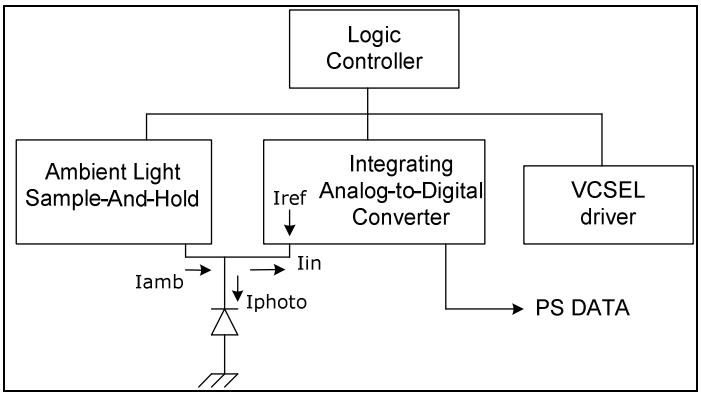


Figure 6.3.1 : Relevant block diagram for LED current & LED pulses explanation.

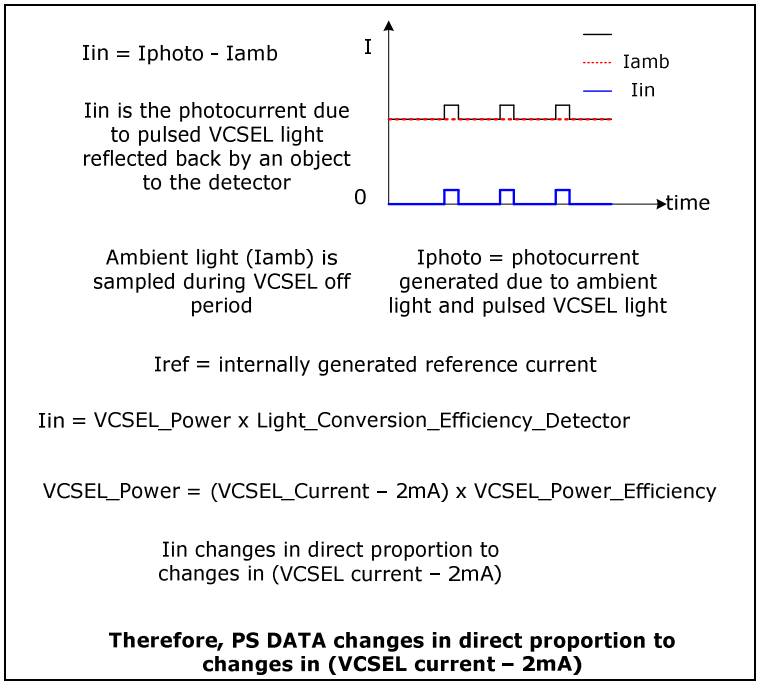


Figure 6.3.2 : The relationship of VCSEL current to the change of PS data.

0x82	PS_VCSEL (default = 0x76)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved				*VCSEL Peak Current*			

Field	Bits	Default	Type	Description	
Reserved	7:4	0111	R/W	----	Must write 0101
VCSEL Current	3:0	0110	R/W	0000	3mA
				0001	4mA
				0010	5mA
				0011	6mA
				0100	7mA
				0101	8mA
				0110	9mA **(default)**
				0111	10mA
				1000	11mA
				1001	12mA
				1010	13mA
				1011	14mA
				1100	15mA
				1101	Reserved
				1110	Reserved
				1111	Reserved

6.4 PS_N_Pulses Register (0x83)

The PS_N_Pulses register controls the number of VCSEL pulses to be emitted. The pulse width is 8us with 25% duty cycle. The PS counts are directly proportional to the VSCEL pulses. If higher PS counts are needed, we can increase the pulses up to 63 pulses.

For pulse rate & number of pulses (Figure 6.4.1), the pulse frequency and duty cycle are fixed, while emitter current and no of pulses settings is available for user programmable.

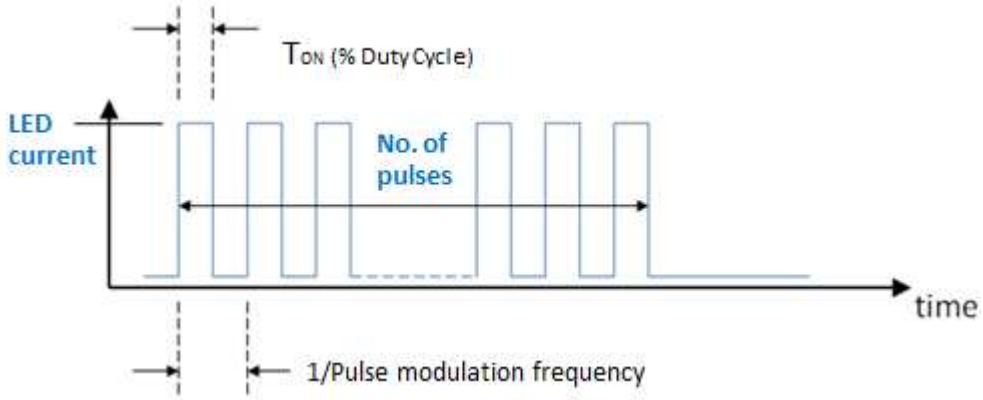


Figure 6.4.1 : LED settings parameters.

Proximity Sensor (PS) data will change in linear proportion to number of pulses (i.e. 2pulses->4pulses means 2X relative increase in PS data). Figure 6.4.2 & 6.3.1 show the block diagram and relationship of VCSEL Pulses to the change of PS data, corresponding to the internal clock 1.3MHz (typical).

$$PS\ DATA = \frac{}{Iref} \times N\_CLKint$$

CLKint = internal clock 1.31MHz

$$N\_CLKint = PulseNumber \times VCSEL\_PulseWidth \div \frac{1}{1.31MHz}$$

$$VCSEL\_PulseWidth = 10 \times \frac{1}{1.31MHz} \sim 8usec$$

8us 24us 8us 24us .....

Each VCSEL pulse is internally generated from internal clock

$$PS\ DATA = \frac{Iin}{Iref} \times PulseNumber \times 10$$

PS DATA changes in direct proportion to change in Number of VCSEL pulse/s

Figure 6.4.2 : The relationship of VCSEL pulses to the change of PS data.

0x83	PS_N_Pulses (default = 0x01)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved		*No of VCSEL Pulse*					

Field	Bits	Default	Type	Description	
VCSEL Pulse Count	7:6	00	--	--	Must be 00
	5:0	000001	R/W	000000	Reserved
				000001	Number of pulses = 1 (default)
				000010	Number of pulses = 2
				000011	Number of pulses = 3
				-----	--------
				111111	Number of pulses = 63

6.5 PS_MEAS_RATE Register (0x84)

The PS_MEAS_RATE register controls the timing of the periodic measurements of the PS in active mode. PS Measurement Repeat Rate is the interval between PS_DATA registers update.

Please refer to Section 7.2 Operating Mode for the ALS and PS measurement sequence (Figure 7.2.1).

0x84	PS_MEAS_RATE (default = 0x04)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved					***PS Measurement Rate***		

Field	Bits	Default	Type	Description	
Reserved	7:3	00000	--	--	--
PS Measurement Rate	2:0	100	RW	000	6.125ms
				001	12.5ms
				010	25ms
				011	50ms
				100	100ms **(default)**
				101	200ms
				110	400ms
				111	800ms

6.6 ALS_MEAS_RATE Register (0x85)

The ALS_MEAS_RATE register controls the integration time and timing of the periodic measurement of the ALS in active mode. ALS Measurement Repeat Rate is the interval between ALS_DATA registers update.

ALS Integration Time is the measurement time for each ALS cycle. ALS Integration Time must be set to be equal or smaller than the ALS Measurement Repeat Rate. If ALS Integration Time is set to be bigger than ALS Measurement Repeat Rate, it will be automatically reset to be equal to ALS Measurement Repeat Rate by the IC internally.

Please refer to Section 7.2 Operating Mode for the ALS and PS measurement sequence (Figure 7.2.1).

0x85	ALS_MEAS_RATE (default = 0x0B)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved			*ALS Integration Time*		*ALS Measurement Rate*		

Field	Bits	Default	Type	Description	
Reserved	7:5	000	---	---	Reserved
ALS Integration Time	4:3	01	RW	00	50ms
				01	100ms **(default)**
				10	200ms
				11	400ms
ALS Measurement Rate	2:0	011	RW	000	50ms
				001	100ms
				010	200ms
				011	400ms **(default)**
				1XX	800ms

6.7 PART_ID Register (0x86) (Read Only)

The PART_ID register defines the part number and revision identification of the sensor.

0x86	PART_ID (default = 0x05)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Part Number ID						*Revision ID*	

Field	Bits	Default	Type	Description
Part Number ID	7:2	000001	R	--
Revision ID	1:0	01	R	--

6.8 MANUFAC_ID Register (0x87) (Read Only)

The MANUFAC_ID register defines the manufacturer identification of the sensor.

0x87	MANUFAC_ID (default = 0x05)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Manufacturer ID							

Field	Bits	Default	Type	Description
Manufacturer ID	7:0	00000101	R	Manufacturer ID (0x05H)

6.9 ALS_DATA CH1 Register(0x88 / 0x89) (Read Only)

The ALS DATA CH1 ADC data is expressed as a 16-bit data spread over two registers. The ALS_DATA_CH1_0 and ALS_DATA _CH1_1 registers provide the lower and upper byte respectively.

To ensure all the 4 bytes of ALS DATA are read out under the same measurement period, the read out must follow the ascending order of the register address (0x88, 0x89, 0x8A, 0x8B).

INT PIN and ALS interrupt flag from ALS_PS_STATUS Register (0x90) will be reset at the end of the reading.

0x88	ALS_DATA_CH1_0 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	ALS Data CH1 Low							

0x89	ALS_DATA_CH1_1 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	ALS Data CH1 High							

Field	Address	Bits	Default	Type	Description
ALS Data CH1 Low	0x88	7:0	00000000	R	ALS CH1 ADC lower byte data
ALS Data CH1 High	0x89	7:0	00000000	R	ALS CH1 ADC upper byte data

6.10 ALS_DATA_CH0 Register (0x8A / 0x8B) (Read Only)

The ALS DATA CH0 ADC data is expressed as a 16-bit data spread over two registers. The ALS_DATA_CH0_0 and ALS_DATA _CH0_1 registers provide the lower and upper byte respectively.

To ensure all the 4 bytes of ALS DATA are read out under the same measurement period, the read out must follow the ascending order of the register address (0x88, 0x89, 0x8A, 0x8B).

INT PIN and interrupt flag from ALS_PS_STATUS Register (0x90) will be reset at the end of the reading.

0x8A	ALS_DATA_CH0_0 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	ALS Data Ch0 Low							

0x8B	ALS_DATA_CH0_1 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	ALS Data Ch0 High							

Field	Address	Bits	Default	Type	Description
ALS Data Ch0 Low	0x8A	7:0	00000000	R	ALS Ch0 ADC lower byte data
ALS Data Ch0 High	0x8B	7:0	00000000	R	ALS Ch0 ADC upper byte data

6.11 ALS_PS_STATUS Register (0x90) (Read Only)

The ALS_PS_STATUS register stores the information about interrupt status and ALS and PS data status independently. New data means data has not been read yet. When the measurement is completed and data is written to the data register, the data status bit will be set to logic 1 for both ALS and PS independently.

ALS Data Status flag and PS Data Status flag will be reset to logic 0 once ALS_Data (0x88, 0x89, 0x8A, 0x8B) and PS Data (0x91 and 0x92) are read respectively.

ALS Data Gain Setting reflects the gain setting on the read ALS Data. Since the ALS function allows writing of Gain setting during the measurement, and the new gain setting will only be take effect after completion of existing measurement. The ALS Data Gain provide the information of the gain use on the read ALS data instead of the new setting. In short, it is recommended to read ALS_PS DATA register before reading ALS data or PS data registers.

Interrupt status determines if the ALS and PS interrupt criteria are met. It will check if the ALS or PS measurement data is outside of the range defined by the upper and lower threshold limits. ALS interrupt and data status will be reset to logic 0 once ALS_DATA (0x88, 0x89, 0x8A, 0x8B) are read, likewise for PS interrupt and data status will be reset to logic 0 once PS_DATA (0x91, 0x92) are read.

0x90	ALS_PS_STATUS (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved	***ALS Data Gain Setting***			***ALS Interrupt Status***	***ALS Data Status***	***PS Interrupt Status***	***PS Data Status***

Field	Bits	Default	Type	Description	
Reserved	7	0	-	Reserved	
ALS Data Gain Setting	6:4	000	R	000	ALS measured data in Gain 1X **(default)**
				001	ALS measured data in Gain 4X
				010	ALS measured data in Gain 16X
				011	ALS measured data in Gain 64X
				100	ALS measured data in Gain 128X
				101	ALS measured data in Gain 256X
				11X	Reserved
ALS Interrupt Status	3	0	R	0	Interrupt signal INACTIVE (default)
				1	Interrupt signal ACTIVE
ALS Data Status	2	0	R	0	OLD data (data already read), (default)
				1	NEW data (first time data is being read)

PS Interrupt Status	1	0	R	0	Interrupt signal INACTIVE (default)
				1	Interrupt signal ACTIVE
PS Data Status	0	0	R	0	OLD data (data already read), (default)
				1	NEW data (first time data is being read)

6.12 PS_DATA_0 Register (0x91 / 0x92) (Read Only)

The PS ADC channel data are expressed as a 11-bit data spread over two registers. The PS_DATA_0 and PS_DATA_1 registers provide the lower and upper byte respectively. When the I^2C read operation starts, both the registers are locked until the I^2C read operation is completed. This will ensure that the data in the registers is from the same measurement even if an additional integration cycle ends during the read operation. New measurement data is stored into temporary registers and the PS_DATA registers are updated as soon as there is no on-going I^2C read operation.

To ensure both the LSB and MSB bytes of PS DATA are read out under the same measurement period, the read out must follow the ascending order of the register address (0x91, 0x92). Interrupt hardware pin and interrupt flag of PS from ALS_PS_STATUS Register (0x90) will be reset at the end of the reading.

0x91	PS_DATA_0 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	PS Data Low							

0x92	PS_DATA_1 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved					***PS Data High***		

Field	Address	Bits	Default	Type	Description	
PS Data, Low	0x91	7:0	00000000	R	--	PS ADC lower byte data
Reserved	0x92	7:3	00000	--	--	--
PS Data, High	0x92	2:0	000	R	--	PS ADC upper byte data

6.13 INTERRUPT Register (0x93)

The INTERRUPT register controls the operation of the interrupt pin and functions.

When the Interrupt Mode is set to 00, the INT output pin 2 is inactive / disabled and will not trigger any interrupt. However at this condition, the ALS_PS_STATUS register will still be updated.

Interrupt polarity sets the Interrupt level is active low or high. See below for illustration:

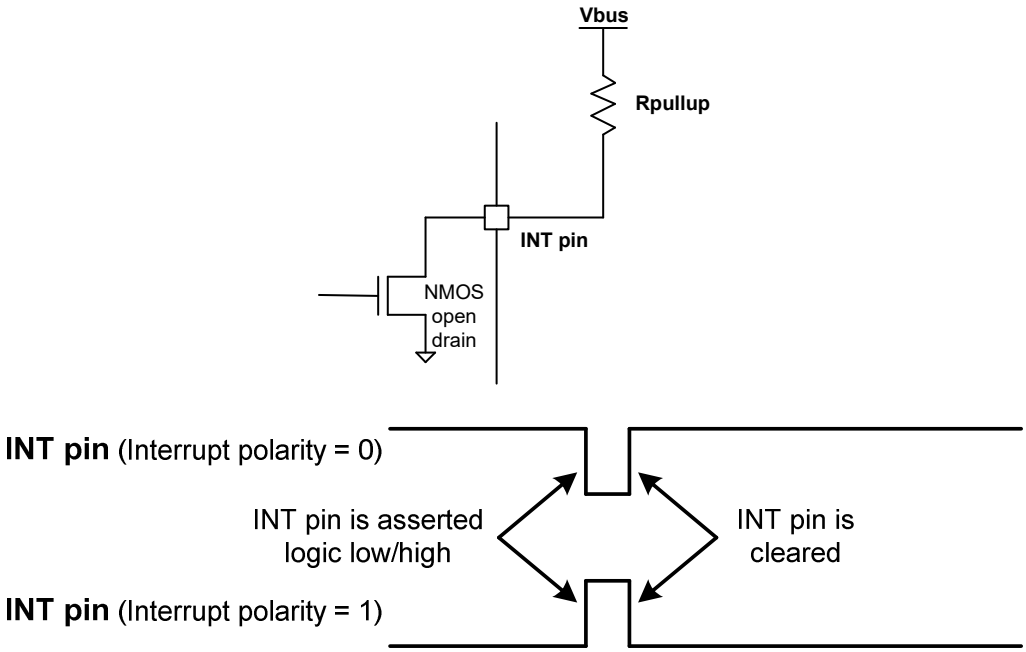


Figure 6.13.1: Interrupt polarity.

Interrupt select is used to choose either ALS CH0 or CH1 data for interrupt computation, since the ALS_PS_STATUS consists only one interrupt status flag. ALS CH0 data is used for interrupt computation when interrupt setting is set to logic 0, vice versa.

FTN (FarToNear) and NTF(NearToFar) is a read only register providing a status bit when object is moving from far to near (FTN) or object is moving near to far (NTF). This feature will only be activated with PS_CONTR (x81[5]) activated.

Note: Since the INTERRUPT Control register is set via I2C communication and I2C clock is not synchronized with IC internal OSC clock, it is not recommended to set this register during active mode, to avoid any glitch or incorrect interrupt information reported.

0x93	INTERRUPT (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	FTN	*NTF*	*Reserved*	*Interrupt Select*	*Reserved*	*Interrupt Polarity*	*Interrupt Mode*	

Field	Bits	Default	Type	Description	
FTN	7	0	R	0	No far-to-near object detected (default)
				1	Far-to-near object detected
NTF	6	0	R	0	No near-to-far object detected (default)
				1	Near-to-far object detected
Reserved	5	0	-	-	-
Interrupt Select	4	0	RW	0	Interrupt computation on CH0 count result(default)
				1	Interrupt computation on CH1 count result
Reserved	3	0	--	--	--
Interrupt Polarity	2	0	RW	0	INT pin is considered active when it is a logic 0 (default)
				1	INT pin is considered active when it is a logic 1
Interrupt Mode	1:0	00	RW	00	Interrupt pin is INACTIVE / high impedance state (default)
				01	Only PS measurement can trigger interrupt
				10	Only ALS measurement can trigger interrupt
				11	Both ALS and PS measurement can trigger interrupt

6.14 INTERRUPT PERSIST Register (0x94)

The INTERRUPT PERSIST register controls the N number of times the measurement data is outside the range defined by the upper and lower threshold limits before asserting the interrupt.

0x94	INTERRUPT PERSIST (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	PS Persist				***ALS Persist***			

Field	Bits	Default	Type	Description	
PS persist	7:4	0000	RW	0000	Every PS value out of threshold range (default)
				0001	1 consecutive PS values out of threshold range
				.....	.....
				1111	16 consecutive PS values out of threshold range
ALS persist	3:0	0000	RW	0000	Every ALS value out of threshold range (default)
				0001	1 consecutive ALS values out of threshold range
				….	….
				1111	16 consecutive ALS values out of threshold range

6.15 PS_THRES Register (0x95 / 0x96 / 0x97 / 0x98)

The PS_THRES_UP and PS_THRES_LOW registers determines the upper and lower limit of the interrupt threshold value respectively. These two values form a range and the interrupt function compares if the measurement value in PS_DATA registers is inside or outside the range. The interrupt function is active if the measurement data is outside the range defined by the upper and lower limits.

The data format for PS_THRES must be the same as PS_DATA registers.

Interrupt will be generated when PS DATA is lower than lower threshold or higher than upper threshold. To differentiate lower than lower threshold and higher than upper threshold, NTF/FTN feature need to be activated. NTF(NeartoFar) when PS Data lower than lower threshold and FTN(FartoNear) when PS Data higher than upper threshold.

0x95	PS_THRES_UP_0 (default = 0xFF)							
	B7	B6	B5	B4	B3	B2	B1	B0
	PS Upper Threshold Low							

0x96	PS_THRES_UP_1 (default = 0x07)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved					*PS Upper Threshold High*		

0x97	PS_THRES_LOW _0 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	PS Lower Threshold Low							

0x98	PS_THRES_LOW_1 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved					*PS Lower Threshold High*		

Field	Address	Bits	Default	Type	Description
PS Upper Threshold Low	0x95	7:0	11111111	RW	PS upper threshold lower byte
Reserved	0x96	7:3	00000	--	Reserved
PS Upper Threshold High	0x96	2:0	111	RW	PS upper threshold upper byte
PS Lower Threshold Low	0x97	7:0	00000000	RW	PS lower interrupt threshold value, lower byte
Reserved	0x98	7:3	00000	--	Reserved
PS Lower Threshold High	0x98	2:0	000	RW	PS lower interrupt threshold value, upper byte

6.16 PS_OFFSET Registers (0x99 / 0x9A)

The PS OFFSET is expressed as a 10-bit word spread over two registers. The PS_OFFSET_LSB and PS_OFFSET_MSB registers provide the lower and upper byte respectively. The actual PS measurement data collected by the PS ADC is 16-bit data. This value will be subtracted by the OFFSET before it is sent to the PS DATA register. The PS DATA register is only 11-bit and data will be stored up to 11-bit (or 2047 count). The PS OFFSET is only 10-bit and therefore maximum count that can be subtracted is 1023. This enable to further extend the dynamic range.

0x99	PS_OFFSET_LSB (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	PS OFFSET LSB							

0x9A	PS_OFFSET_MSB (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved						***PS OFFSET MSB***	

Field	Address	Bits	Default	Type	Description	
PS OFFSET LSB	0x99	7:0	00000000	R/W	--	PS OFFSET lower byte
Reserved	0x9A	7:2	000000	--	--	--
PS OFFSET MSB	0x9A	1:0	00	R/W	--	PS OFFSET upper byte

6.17 ALS_THRES Register (0x9B / 0x9C / 0x9D / 0x9E)

The ALS_THRES_UP and ALS_THRES_LOW registers determines the upper and lower limit of the interrupt threshold value respectively. These two values form a range and the interrupt function compares if the measurement value in ALS_DATA registers is inside or outside the range. The interrupt function is active if the measurement data is outside the range defined by the upper and lower limits.

The data format for ALS_THRES must be the same as ALS_DATA registers.

Interrupt will be generated when ALS DATA is lower than lower threshold or higher than upper threshold.

0x9B	ALS_THRES_UP_0 (default = 0xFF)							
	B7	B6	B5	B4	B3	B2	B1	B0
	ALS Upper Threshold Low							

0x9C	ALS_THRES_UP_1 (default = 0xFF)							
	B7	B6	B5	B4	B3	B2	B1	B0
	ALS Upper Threshold High							

0x9D	ALS_THRES_LOW _0 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	ALS Lower Threshold Low							

0x9E	ALS_THRES_LOW_1 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	ALS Lower Threshold High							

Field	Address	Bits	Default	Type	Description
ALS Upper Threshold Low	0x9B	7:0	11111111	RW	ALS upper threshold lower byte
ALS Upper Threshold High	0x9C	7:0	11111111	RW	ALS upper threshold upper byte
ALS Lower Threshold Low	0x9D	7:0	00000000	RW	ALS lower threshold lower byte
ALS Lower Threshold High	0x9E	7:0	00000000	RW	ALS lower threshold upper byte

6.18 FD_CONTR Register (0x9F)

The FD_CONTR register controls fault detection timing and enable fault detection function. Each PS cycle starts with a process to check whether there is a fault before the actual PS measurement. Two types of fault detection can be selected using Register 0x9F bit1, the Level1 and full (Level1&2) fault detection.

FD Self Check (Register 0x9F bit4) – This is used when the user want to force a fault detection check. Normally, the fault detection check will be ON during PS enable state. Fault detection will not be active if the PS is in the OFF or DISABLE state. However the user can force a fault detection check when the PS is in the off state. This is done by setting the FD Self Check bit and also the ON CLOCK bit in the register 0x80. It is recommended to force a fault detection check whenever the device is power on so that fault can be immediately detected.

0x9F	FAULT_DETECTION_CONTR (default = 0x01)							
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
	Reserved			***FD Self Check***	***Reserved***			***FD Level***

Field	Bits	Default	Type	Description	
Reserved	7:5	00	RW	Must be write as 00	
FD Self Check	4	0	-	0	Self Check Fault Detection disabled (default)
				1	Run Self Check Fault Detection
Reserved	3:1	000	--	000	Must write 0
FD Level	0	0	RW	0	Level 2 Fault Detection
				1	Level 1 Fault Detection **(default)**

6.19 FD_STATUS (0xA0) Register

Besides the flags reporting from FD_STATUS register, an INTERRUPT will be generated from the IC to the host controller, regardless the settings of INTERRUPT Register (0x93, Bit 1:0). When fault is detected, the chip will send/pull ENB pin to high state and turn off the VCSEL. It is recommended to have host controller immediate attention once it received the interrupt signal, to switch off the VLED supply as fault detected.

A list of flags corresponding to each checking process is as below:

- VCSEL leakage – resistive short from VCSEL Cathode to ground which is < 5Kohms
- ENB Gate stuck low – this flag reporting ENB output pin (i.e. external PMOS gate) stuck low
- ENB Gate stuck high – this flag reporting ENB output pin (i.e. External PMOS gate) stuck high
- ENB Fault – this flag reporting PMOS switch faulty (i.e. cannot turn OFF switch).
- VCSEL Fault – this flag reporting VCSEL Cathode is shorted to ground which will cause high driving current to the VCSEL.

0xA0	FD_STATUS (default = 0x00)							
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
	Reserved			***VCSEL leakage***	***ENB Gate stuck low***	***ENB Gate stuck high***	***ENB Fault***	***VCSEL Fault***

Field	Bits	Default	Type	Description	
Reserved	7:5	00	R	Reserved	
VCSEL leakage	4	0	R	0	No leakage **(default)**
				1	VCSEL leak to GND, level 2 FD only
ENB Gate stuck low	3	0	R	0	ENB gate controllable **(default)**
				1	ENB gate stuck at logic low, for level 2 FD
ENB Gate stuck high	2	0	R	0	ENB gate controllable **(default)**
				1	ENB gate stuck at logic high, for level 2 FD
ENB Fault	1	0	R	0	External CMOS switch normal **(default)**
				1	External CMOS switch Faulty, for level 2 FD
VCSEL FAULT	0	0	R	0	VCSEL Cathode not short to GND **(default)**
				1	VCSEL Cathode short to GND, level 1 and level 2 FD

7 Application Information

Lux_Calc is the calculated lux reading based on the output ADC from ALS DATA regardless of light sources.

7.1 ALS Lux Conversion formula

$$Lux = \frac{a \times CH0 + b\ CH1}{(GAIN \times INT)} \times W_{FAC}$$

Where :

1. CH0 is the ALS measurement count for CH0 in register ALS_DATA_CH0 (0x8A and 0x8B)
2. CH1 is the ALS measurement count for CH1 in register ALS_DATA_CH1 (0x88 and 0x89)
3. *Where WinFac = 1*
4. Co-efficient of a and b

Ratio	***a***	***b***
Ratio <0.14	*0*	*0*
0.14 <= Ratio < 0.3	*0.0379*	*0.152*
0.3 <= Ratio < 0.51	*-0.491*	*1.995*
Ratio >= 0.51	*0.8*	*-0.576*

Note: $Ratio = \frac{CH1(Visible)}{CH0(Full\ Spectrum)}$

5. The Gain factors & Integration time factors:

ALS Gain	GAIN
X1	**1**
X4	**4**
X16	**16**
X64	**64**
X128	**128**
X256	**256**

Integration Time (ms)	INT
50ms	**0.5**
100ms	**1**
200ms	**2**
400ms	**4**

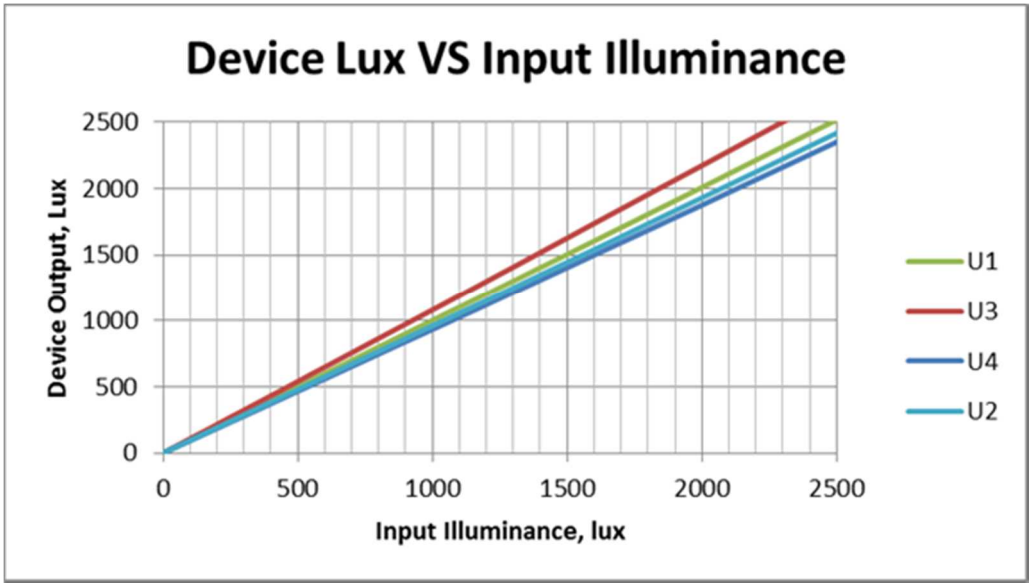


Figure 7.1.1: ALS performance under WhiteLED condition, VDD 3V, 100ms Integration Time, 200ms Measurement rate, Gain X4, with others in default settings.

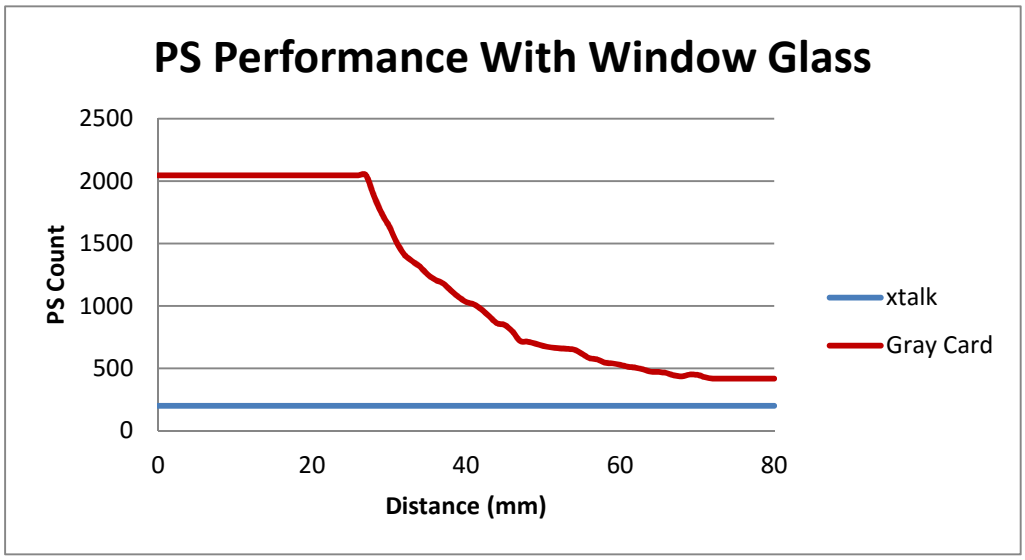


Figure 7.1.2: PS performance over Gray Card (18% reflectivity) with window glass of 0.8mm thickness, VDD 3V, 6mA, 48pulses, with others in default settings.

7.2 Operating Modes

Stand-by Mode

The device is by default in stand-by mode after power-up. No measurement activity done in either ALS or PS. I^2C communication is allowed to be able to read/write to the registers. The device can be reset from MCU by setting appropriate register control (SW reset). Start-up sequence is exactly the same as that when power-on reset is triggered.

Active Mode

The ALS and PS can simultaneously be in active mode (see Fig 1). Measurement data is expected to be available within a known fixed time (refer to measurement time parameter from ALS and PS specification).

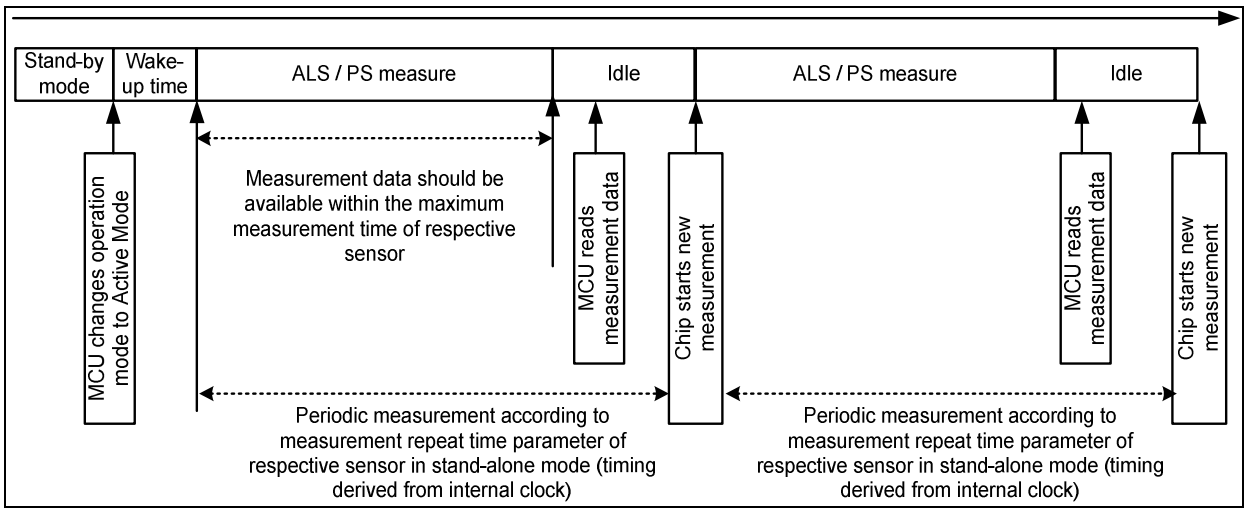


Figure 7.2.1 : ALS and PS measurement sequence

7.3 Interrupt Features

The interrupt function is active if ALS or PS measurements are outside of the upper and lower absolute threshold levels set in the appropriate threshold register. Only newly measured data is compared to the threshold levels set such that old data will not cause triggering of the INT pin if in case the threshold levels are changed in between measurements. The status of interrupt can be monitored directly through the interrupt (INT) pin or by checking contents of the interrupt register. Interrupt pin can either be enable or disabled. Possible to invert interrupt output of LOW or HIGH state. Interrupt pin IO requirements are exactly the same as those of the I2C bus pins SDA and SCL.

There are two user selectable type of interrupts, which are window interrupt type & logic interrupt type. Refer to Figure

7.3.1 and 7.3.2 for illustration.

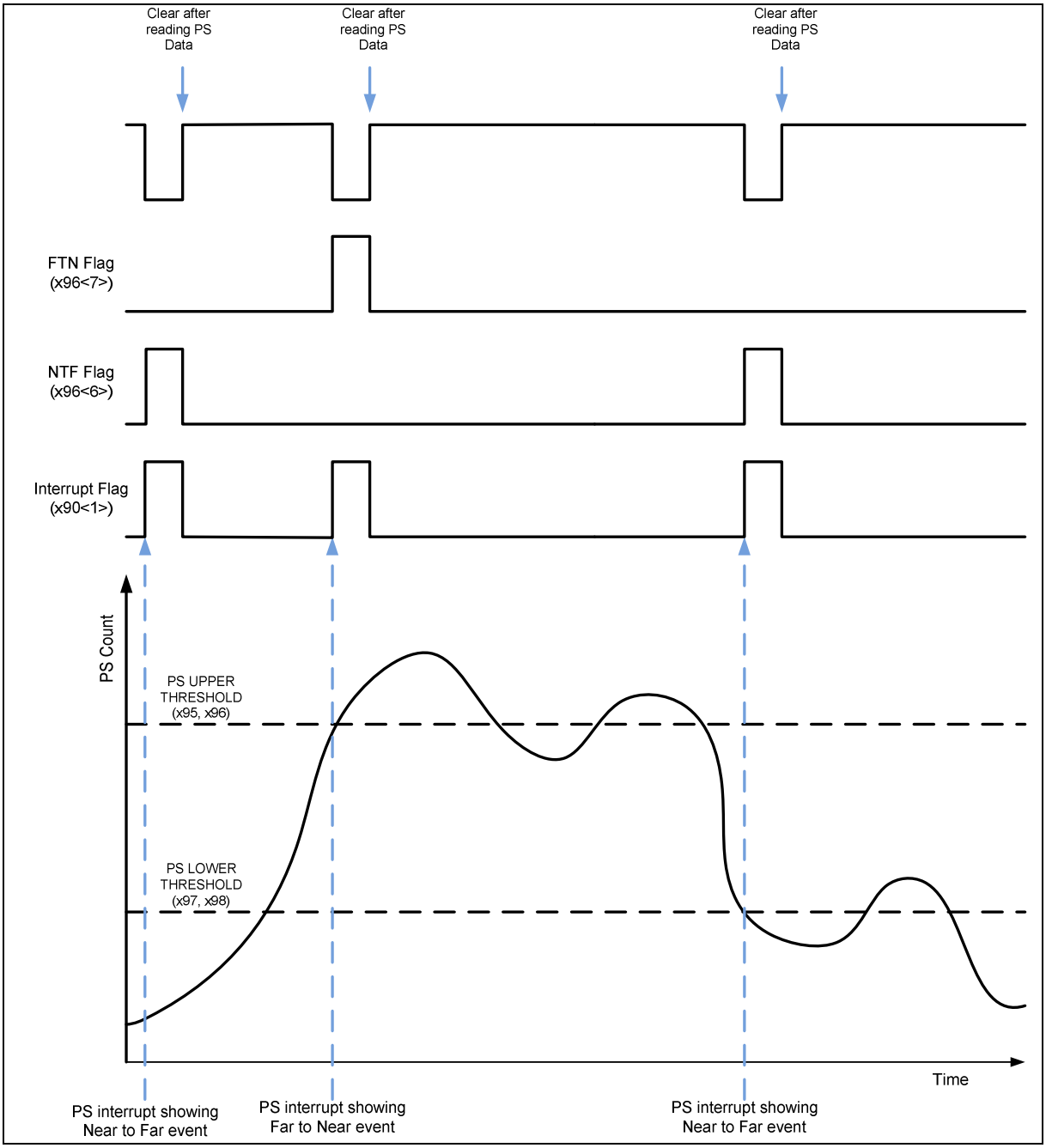


Figure 7.3.1 : Interrupt illustration on logic type (with NTF/FTN reporting)
(Logic Mode: activated by control register PS_CONTR (0x81<5>) and INTERRUPT (0x91<0>))

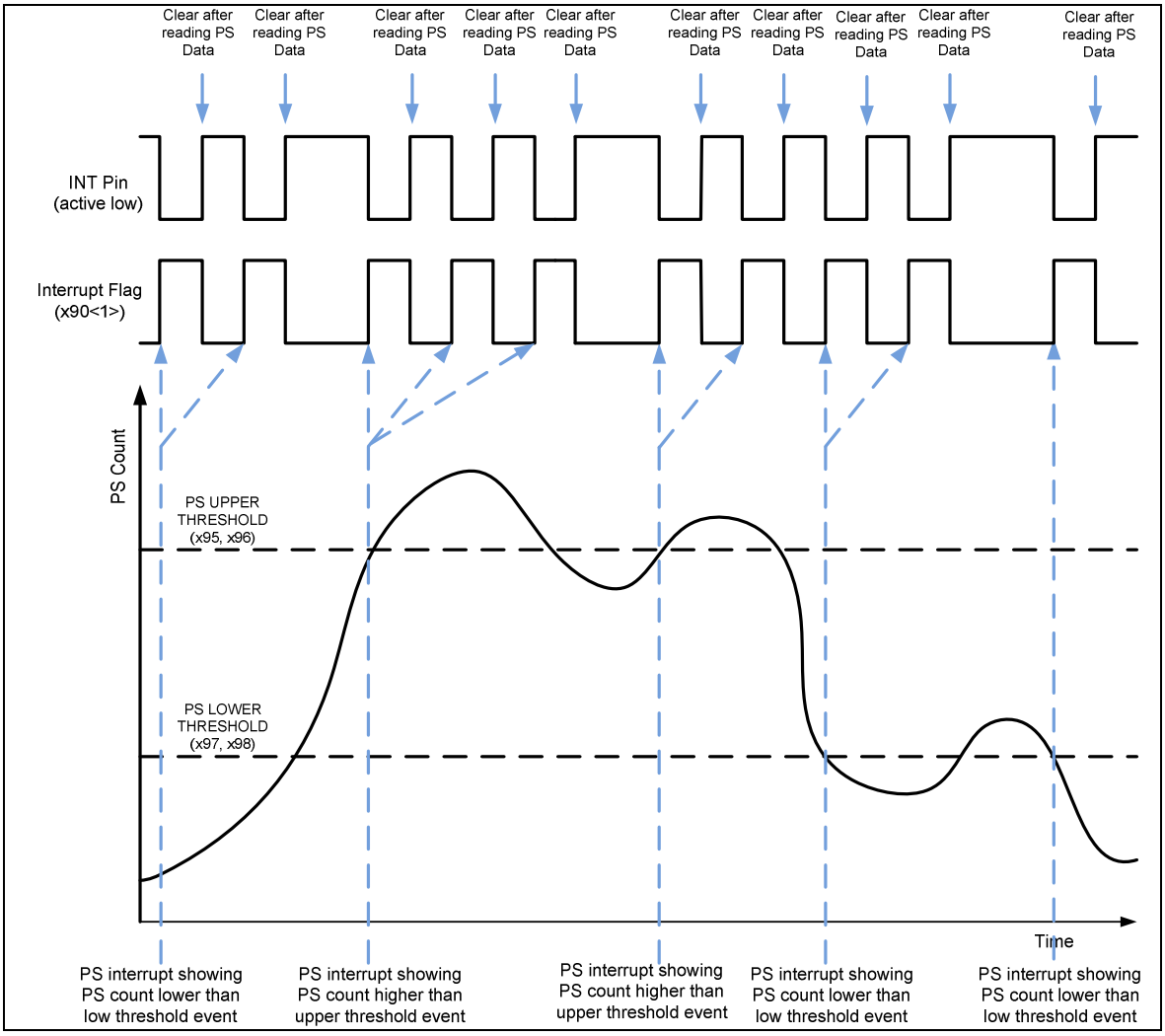
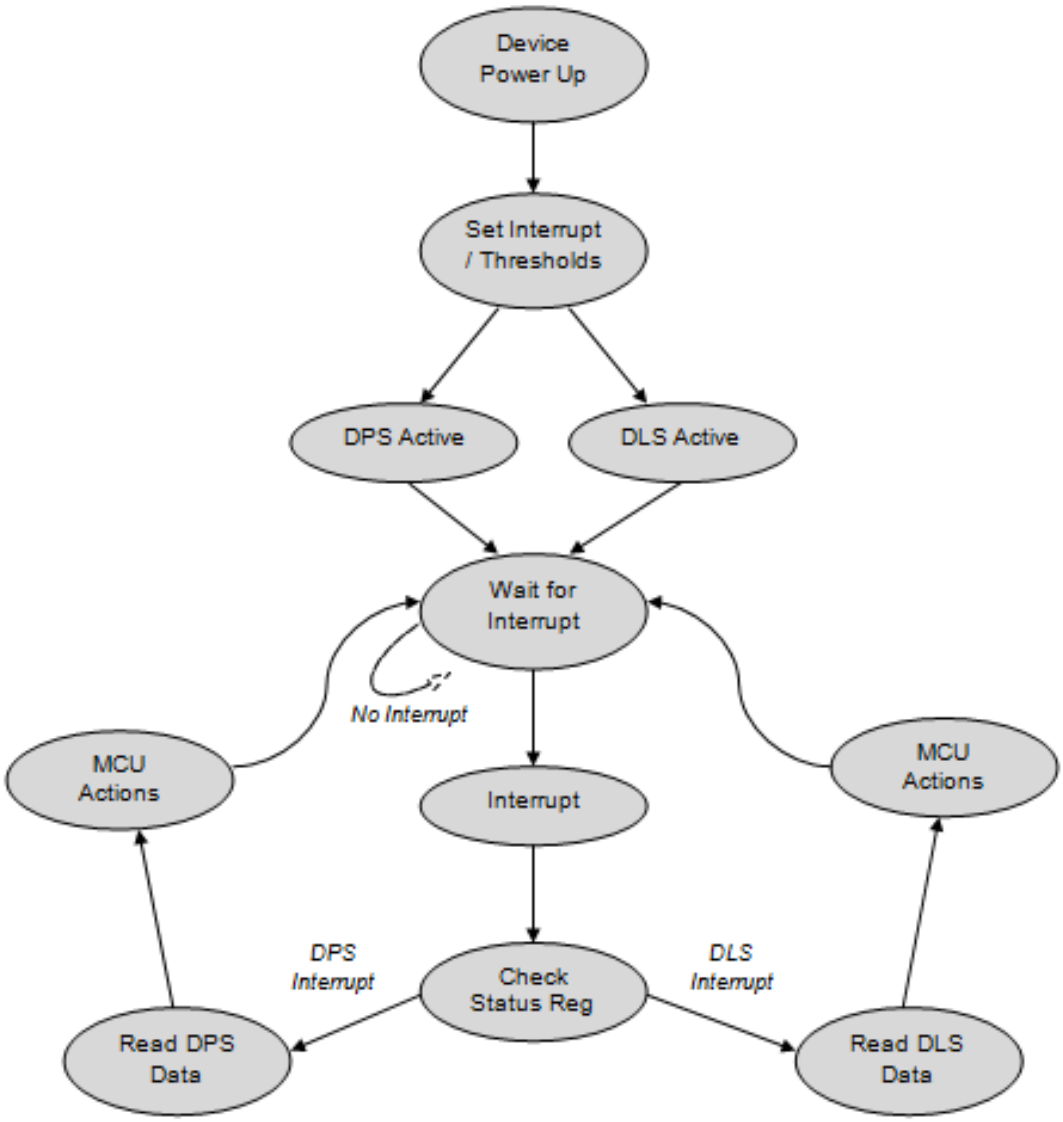


Figure 7.3.2 : Interrupt illustration on window type (by default, without NTF/FTN reporting)

Flow diagram below illustrates the LTR-778ALS-BE operation flow, and involving the use of Thresholds and interrupt.



7.4 Fault detection

For Level 1 of fault detection, the IC will check the VCSEL cathode whether it is shorted to ground potentially causing high current surge in the VCSEL. If it is shorted to ground the “VCSEL Fault” flag (Register 0xA0 bit 0) will be asserted. This fault detection works with the application circuit that does not require an external PMOS transistor.

The 2-level fault detection works with the application circuit that requires an external PMOS transistor to switch the VCSEL to the power supply. In addition to the above Level1 fault detection, the IC will look for further external circuit failures focusing on the ENB output pin and the external PMOS transistor.

In this fault check, the logic level of the ENB output pin (which is connected to the external PMOS gate) is measured by the IC to determine whether it is permanently stuck low or high (i.e. cannot be controlled). If the ENB output pin is found to be stuck low, the “ENB Gate stuck low” flag (Register 0xA0 bit 3) will be set. If the ENB output pin is found to be stuck high, the “ENB Gate stuck high” flag (Register 0xA0 bit 2) will be set. Following this stuck high and low test, the IC will also check whether the external PMOS transistor can be turned OFF. This is flagged as “ENB Fault” (Register 0xA0 bit 1). The IC will also check leakage current from VCSEL Cathode to ground. If there is a resistive short from VCSEL Cathode to ground which is 5Kohms and lower, this is flagged as “VCSEL leakage (Register 0xA0 bit 4)”.

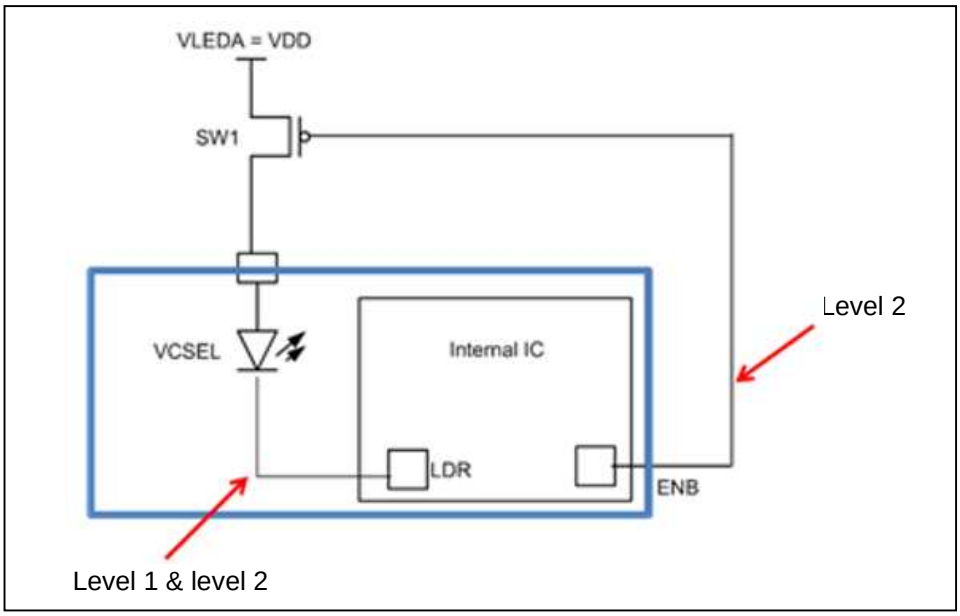


Figure 7.4.1: Fault detection circuits, level 1 & level 2.

7.5 Example Pseudo Code

Control Registers

// The Control Registers define the operating modes and gain settings of the ALS and PS of LTR-778ALS-BE
// Default settings are 0x00 for ALS control register (0x80) and 0x40 for PS registers (0x40).

```
Slave_Addr = 0x23                    // Slave address of LTR-778ALS-BE device

// Enable ALS
Register_Addr = 0x80                 // ALS_CONTR register
Command = 0x01                       // For Gain X1, Command = 0x01
                                     // For Gain X16, Command = 0x09
                                     // For Gain X256, Command = 0x15
WriteByte(Slave_Addr, Register_Addr, Command)

// Enable PS
Register_Addr = 0x81                 // PS_CONTR register
Command = 0x42
WriteByte(Slave_Addr, Register_Addr, Command)
```

PS VCSEL Registers

// The PS VCSEL Registers define the VCSEL peak current.
// Default setting is 0x76 (9mA).

```
Slave_Addr = 0x23                    // Slave address of LTR-778ALS-BE device

Register_Addr = 0x82                 // PS_VCSEL register
Command = 0x76                       // peak current 9mA

WriteByte(Slave_Addr, Register_Addr, Command)
```

PS N PULSES

// The PS_N_PULSES defines the number of pulses
// Default setting is 0x01 (1 pulses).

```
Slave_Addr = 0x23                    // Slave address of LTR-778ALS-BE device

Register_Addr = 0x83                 // PS_LED Register for Number of pulses
Command = 0x20                       // Number of pulses = 32

WriteByte(Slave_Addr, Register_Addr, Command)
```

PS Measurement Rate

// The PS_MEAS_RATE register controls the PS measurement rate.
// Default setting of the register is 0x04 (repeat rate 100ms)

```
Slave_Addr = 0x23                    // Slave address of LTR-778ALS-BE device

// Set PS Repeat Rate 50ms
Register_Addr = 0x84                 // PS_MEAS_RATE register
Command = 0x06                       // Meas rate = 400ms

WriteByte(Slave_Addr, Register_Addr, Command)
```

ALS Measurement Rate

// The ALS_MEAS_RATE register controls the ALS integration time and measurement rate.
// Default setting of the register is 0x0B (integration time 100ms, repeat rate 400ms)

```
Slave_Addr = 0x23                          // Slave address of LTR-778ALS-BE device

// Set ALS Integration Time 100ms, Repeat Rate 500ms
Register_Addr = 0x85                       // ALS_MEAS_RATE register
Command = 0x13                             // Int time = 200ms, Meas rate = 400ms

WriteByte(Slave_Addr, Register_Addr, Command)
```

ALS Data Registers (Read Only)

// The ALS Data Registers contain the ADC output data for the respective channel.
// These registers should be read as a group, with the lower address being read first.

```
Slave_Addr = 0x23                          // Slave address of LTR-778ALS-BE device

// Read back ALS_DATA_CH0
Register_Addr = 0x8A                       // ALS_DATA_CH0 low byte address
ReadByte(Slave_Addr, Register_Addr, Data1)
Register_Addr = 0x8B                       // ALS_DATA_CH0 high byte address
ReadByte(Slave_Addr, Register_Addr, Data2)

ALS_CH0_ADC_Data = (Data2 << 8) | Data1    // Combining lower and upper bytes to give 16-bit Ch0 data
```

ALS / PS Status Register (Read Only)

// The ALS_PS_STATUS Register contains the information on Interrupt, ALS and PS data availability status.
// This register is read only.

```
Slave_Addr = 0x23                          // Slave address of LTR-778ALS-BE device

// Read back Register
Register_Addr = 0x90                       // ALS_PS_STATUS register address
ReadByte(Slave_Addr, Register_Addr, Data)

Interrupt_Status = Data & 0x0A             // Interrupt_Status = 8(decimal) ➔ ALS Interrupt
                                           // Interrupt_Status = 2(decimal) ➔ PS Interrupt
                                           // Interrupt_Status = 10(decimal) ➔ Both Interrupt

NewData_Status = Data & 0x05               // NewData_Status = 4(decimal) ➔ ALS New Data
                                           // NewData_Status = 1(decimal) ➔ PS New Data
                                           // NewData_Status = 5(decimal) ➔ Both New Data
```

PS Data Registers (Read Only)

// The PS Data Registers contain the ADC output data.
// These registers should be read as a group, with the lower address being read first.

```
Slave_Addr = 0x23                          // Slave address of LTR-778ALS-BE device

// Read back PS_DATA registers
Register_Addr = 0x91                       // PS_DATA low byte address
ReadByte(Slave_Addr, Register_Addr, Data0)


Register_Addr = 0x92                       // PS_DATA high byte address
ReadByte(Slave_Addr, Register_Addr, Data1)

PS_ADC_Data = (Data1 << 8) | Data0         // Combining lower and upper bytes to give 16-bit PS data
```

Interrupt Registers

// The Interrupt register controls the operation of the interrupt pins and function.
// The default value for this register is 0x08 (Interrupt inactive)

```
Slave_Addr = 0x23                          // Slave address of LTR-778ALS-BE device

// Set Interrupt Polarity for Active Low, both ALS and PS trigger
Register_Addr = 0x93                       // Interrupt Register address
Command = 0x03                             // Interrupt is Active Low and both ALS and PS can trigger

WriteByte(Slave_Addr, Register_Addr, Command)
```

ALS Threshold Registers

// The ALS_THRES_UP and ALS_THRES_LOW registers determines the upper and
// lower limit of the interrupt threshold value.
// Following example illustrates the setting of the ALS threshold window of
// decimal values of 200 (lower threshold) and 1000 (upper threshold)

```
Slave_Addr = 0x23                          // Slave address of LTR-778ALS-BE device

// Upper Threshold Setting (decimal 1000)
ALS_Upp_Threshold_Reg_0 = 0x9B             // ALS Upper Threshold Low Byte Register address
ALS_Upp_Threshold_Reg_1 = 0x9C             // ALS Upper Threshold High Byte Register address
Data1 = 1000 >> 8                          // To convert decimal 1000 into two eight bytes register values
Data0 = 1000 & 0xFF
WriteByte(Slave_Addr, ALS_Upp_Threshold_Reg_0, Data0)
WriteByte(Slave_Addr, ALS_Upp_Threshold_Reg_1, Data1)


// Lower Threshold Setting (decimal 200)
ALS_Low_Threshold_Reg_0 = 0x9D             // ALS Lower Threshold Low Byte Register address
ALS_Low_Threshold_Reg_1 = 0x9E             // ALS Lower Threshold High Byte Register address
Data1 = 200 >> 8                           // To convert decimal 200 into two eight bytes register values
Data0 = 200 & 0xFF
WriteByte(Slave_Addr, ALS_Low_Threshold_Reg_0, Data0)
WriteByte(Slave_Addr, ALS_Low_Threshold_Reg_1, Data1)
```

PS Threshold Registers

// The PS_THRES_UP and PS_THRES_LOW registers determines the upper and
// lower limit of the interrupt threshold value.
// Following example illustrates the setting of the PS dynamic threshold with hysteresis interruption for
// decimal value 1000 (for NEAR detection) and 500 (for FAR detection)

```
Slave_Addr = 0x23                          // Slave address of LTR-778ALS-BE device

//For NEAR detection (decimal 1000)
PS_Upp_Threshold_Reg_0 = 0x95              // PS Upper Threshold Low Byte Register address
PS_Upp_Threshold_Reg_1 = 0x96              // PS Upper Threshold High Byte Register address
Data1 = 1000 >> 8                          // To convert decimal 1000 into two eight bytes register values
Data0 = 1000 & 0xFF
WriteByte(Slave_Addr, PS_Upp_Threshold_Reg_0, Data0)
WriteByte(Slave_Addr, PS_Upp_Threshold_Reg_1, Data1)

PS_Low_Threshold_Reg_0 = 0x97              // PS Lower Threshold Low Byte Register address
PS_Low_Threshold_Reg_1 = 0x98              // PS Lower Threshold High Byte Register address


Data1 = 0 >> 8                             // To convert decimal 0 into two eight bytes register values
Data0 = 0 & 0xFF
WriteByte(Slave_Addr, PS_Low_Threshold_Reg_0, Data0)
WriteByte(Slave_Addr, PS_Low_Threshold_Reg_1, Data1)
```

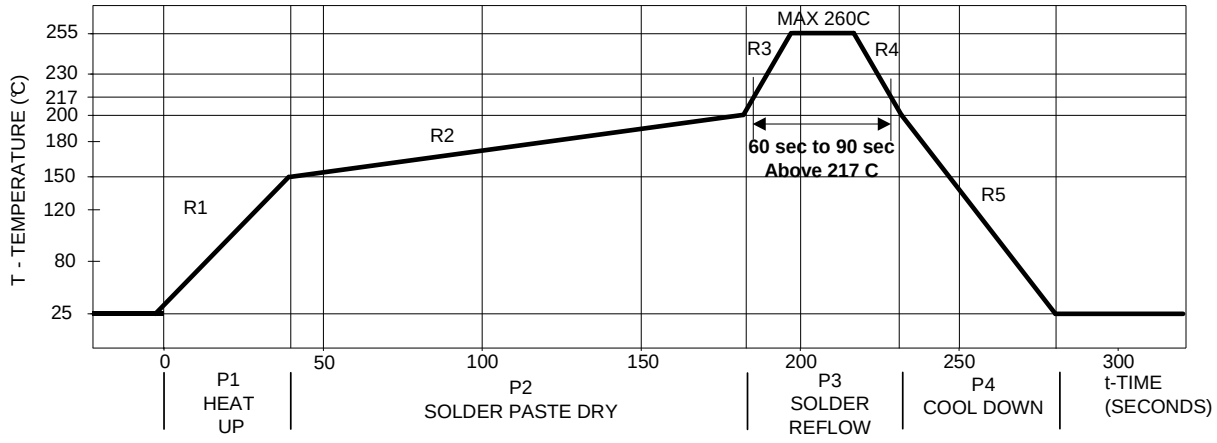
//For FAR detection (decimal 500)

```
PS_Upp_Threshold_Reg_0 = 0x95                    // PS Upper Threshold Low Byte Register address
PS_Upp_Threshold_Reg_1 = 0x96                    // PS Upper Threshold High Byte Register address
Data1 = 2047 >> 8                                // To convert decimal 2047 into two eight bytes register values
Data0 = 2047 & 0xFF
WriteByte(Slave_Addr, PS_Upp_Threshold_Reg_0, Data0)
WriteByte(Slave_Addr, PS_Upp_Threshold_Reg_1, Data1)

PS_Low_Threshold_Reg_0 = 0x97                    // PS Lower Threshold Low Byte Register address
PS_Low_Threshold_Reg_1 = 0x98                    // PS Lower Threshold High Byte Register address
Data1 = 500 >> 8                                 // To convert decimal 500 into two eight bytes register values
Data0 = 500 & 0xFF
WriteByte(Slave_Addr, PS_Low_Threshold_Reg_0, Data0)
WriteByte(Slave_Addr, PS_Low_Threshold_Reg_1, Data1)
```

Fault Detection Control Register

```
// Upon power up and before PS is enable, it is recommended that the fault detection is activated.
//This is done by the following instructions.
Slave_Addr = 0x23                                // Slave address of LTR-778ALS-BE device

Register Addr = 0x9F                             //  Fault detection register
Command = 0x10                                   //  0x10 for Force detection of Full (Level1&2) fault detection
WriteByte(Slave_Addr, Register_Addr, Command)    //  0x11 for Force detection of Level1 fault detection

Register Addr = 0x80                             //  ALS control register
Command = 0x10                                   //  Activate the CLOCK to force a fault detection
WriteByte(Slave_Addr, Register_Addr, Command)

Register_Addr = 0xA0                             // Fault detection register
ReadByte(Slave_Addr, Register_Addr, Data)
Interrupt_Status = Data & 0x0F                   // Fault status = 8(decimal) ➔ ENB Gate stuck low
                                                 // Fault status = 4(decimal) ➔ ENB Gate stuck high
                                                 // Fault status = 2(decimal) ➔ ENB Fault
                                                 // Fault status = 1(decimal) ➔ VCSEL fault

Register Addr = 0x80                             //  ALS control register
Command = 0x00                                   //  De-Activate the CLOCK to stop the fault detection
WriteByte(Slave_Addr, Register_Addr, Command)


// Setting the fault level of the fault detection.
//This is done by the following instructions.
Slave_Addr = 0x23                                // Slave address of LTR-778ALS-BE device

Register Addr = 0x9F                             //  Fault detection register
Command = 0x00                                   //  0x00 for Force detection of Full (Level1&2) fault detection
WriteByte(Slave_Addr, Register_Addr, Command)    //  0x01 for Force detection of Level1 fault detection

Register_Addr = 0x83                             // PS_LED Register for Number of pulses
Command = 0x08                                   // Number of pulses = 8

Register_Addr = 0x81                             // PS_CONTR register
Command = 0x02                                   // PS ON
WriteByte(Slave_Addr, Register_Addr, Command)

Register_Addr = 0xA0                             // Fault detection register
ReadByte(Slave_Addr, Register_Addr, Data)
Interrupt_Status = Data & 0x0F                   // Fault status = 8(decimal) ➔ ENB Gate stuck low
                                                 // Fault status = 4(decimal) ➔ ENB Gate stuck high
                                                 // Fault status = 2(decimal) ➔ ENB Fault
                                                 // Fault status = 1(decimal) ➔ VCSEL fault
```

8 Recommended Lead-free Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100s to 180s
Solder Reflow	P3, R3 P3, R4	200°C to 260°C 260°C to 200°C	3°C/s -6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s
Time maintained above liquidus point , 217°C		> 217°C	60s to 90s
Peak Temperature		260°C	-
Time within 5°C of actual Peak Temperature		> 255°C	20s
Time 25°C to Peak Temperature		25°C to 260°C	8mins

It is recommended to perform reflow soldering no more than three times without rework.

For manual soldering, the soldering iron tip shall not touch the package plastic body, The soldering iron shall only in contact to the circuit board pad and the heat should be conducted to the tin wire and component lead. The temperature of the solder iron can be set as high as 300 degree but the temperature on the tip of the tool shall be 270 to 275ºC. Soldering process shall take a few seconds for each pin/pad. The package maximum temperature shall be kept less than 270ºC and all mechanical stresses in the pin should be minimized. It should be noted that the thermoplastic shield material (PA9T) attached on top of the component has a thermal deflection temperature of around 280 degree and will be damaged if excessive heat above this temperature is used.

9 Moisture Proof Packaging

All LTR-778ALS-BE are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC J-STD-033A Level 3.

Time from Unsealing to Soldering

After removal from the moisture barrier bag, the parts should be stored at the recommended storage conditions and soldered within seven days. When the moisture barrier bag is opened and the parts are exposed to the recommended storage conditions for more than seven days, the parts must be baked before reflow to prevent damage to the parts.

Recommended Storage Conditions

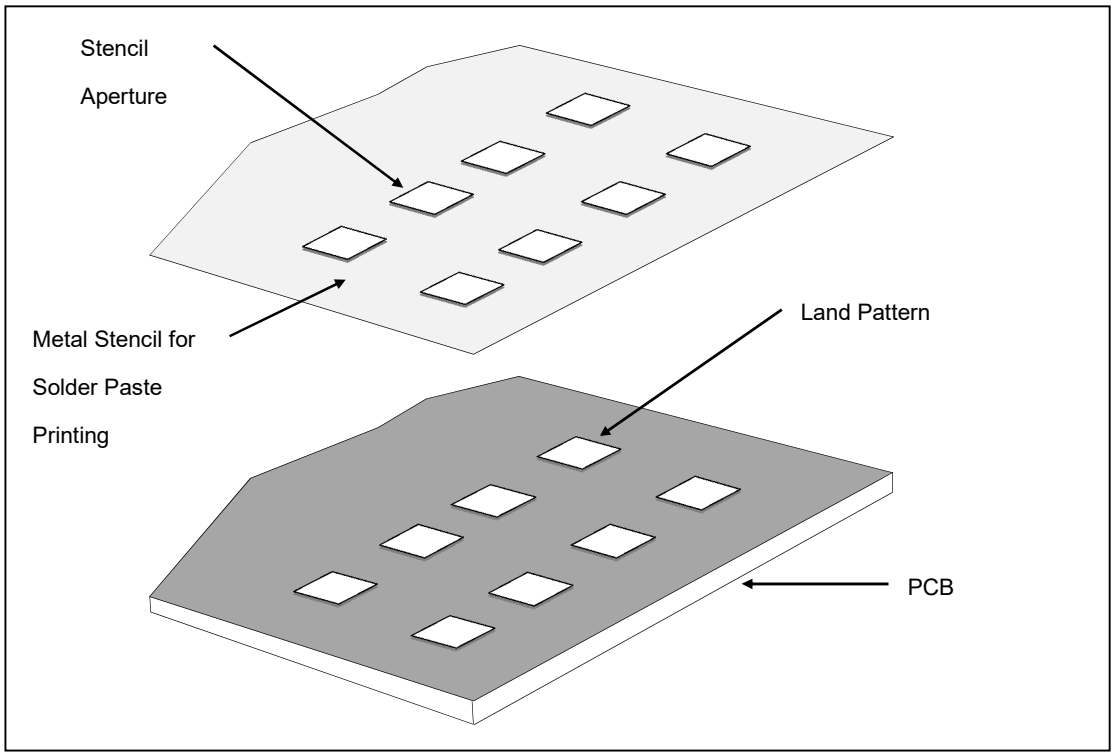
Storage Temperature	10°C to 30°C
Relative Humidity	Below 60% RH

Baking Conditions

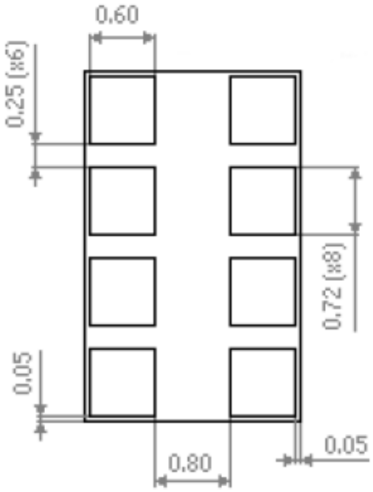
Package	Temperature	Time
In Reels	60°C	48 hours
In Bulk	100°C	4 hours

- Baking should only be done once.

10 Recommended Land Pattern and Metal Stencil Aperture



10.1 Recommended Land Pattern

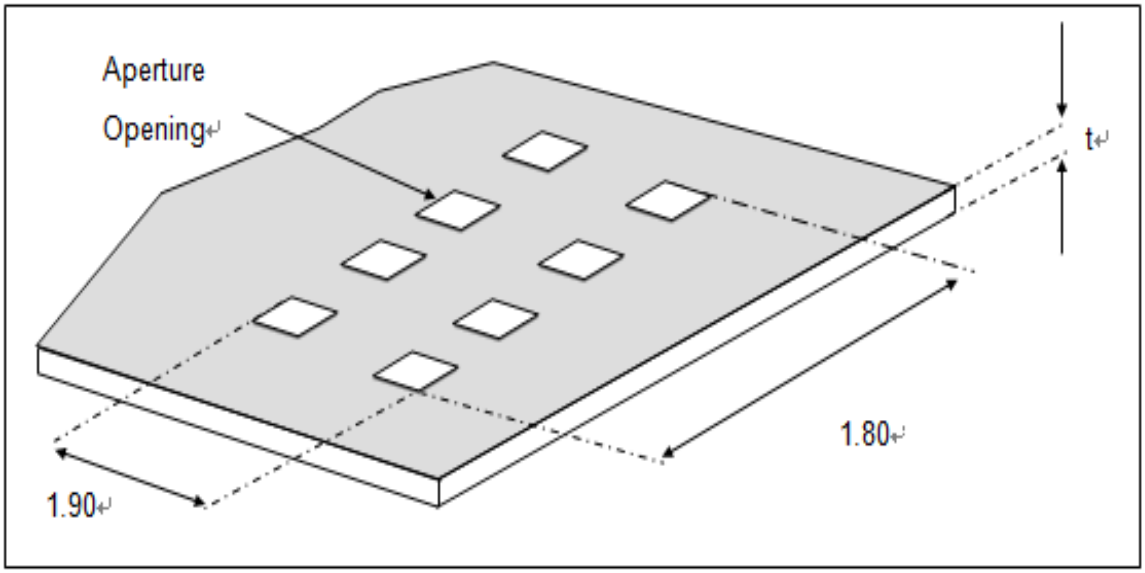


Note: All dimensions are in millimeters.

10.2 Recommended Metal Stencil Aperture

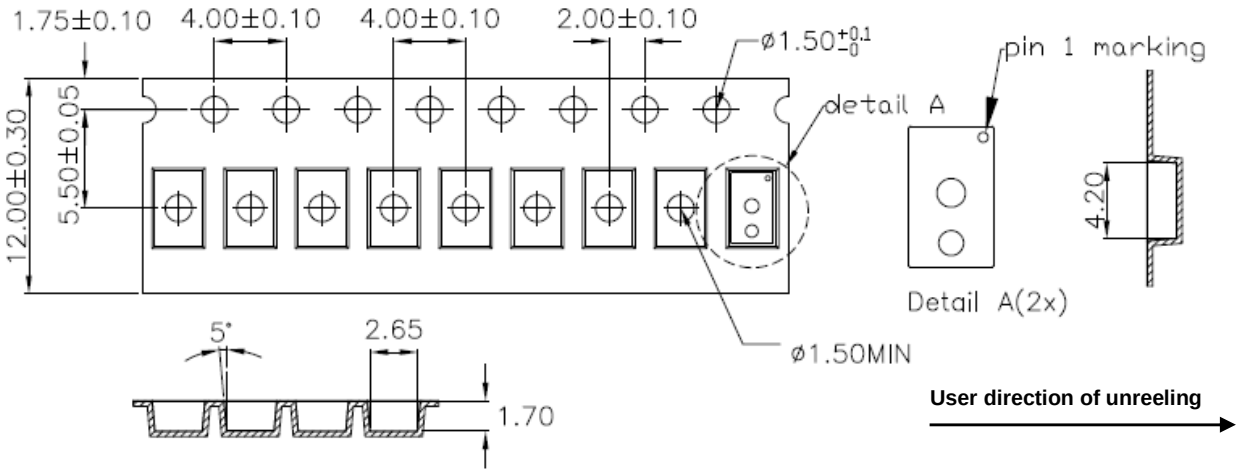
It is recommended that the metal stencil used for solder paste printing has a thickness (t) of 0.11mm (0.004 inches / 4 mils) or 0.127mm (0.005 inches / 5 mils).

The stencil aperture opening is recommended to be 0.30mm x 0.35mm which has the same dimension as the land pattern. This is to ensure adequate printed solder paste volume and yet no shorting.



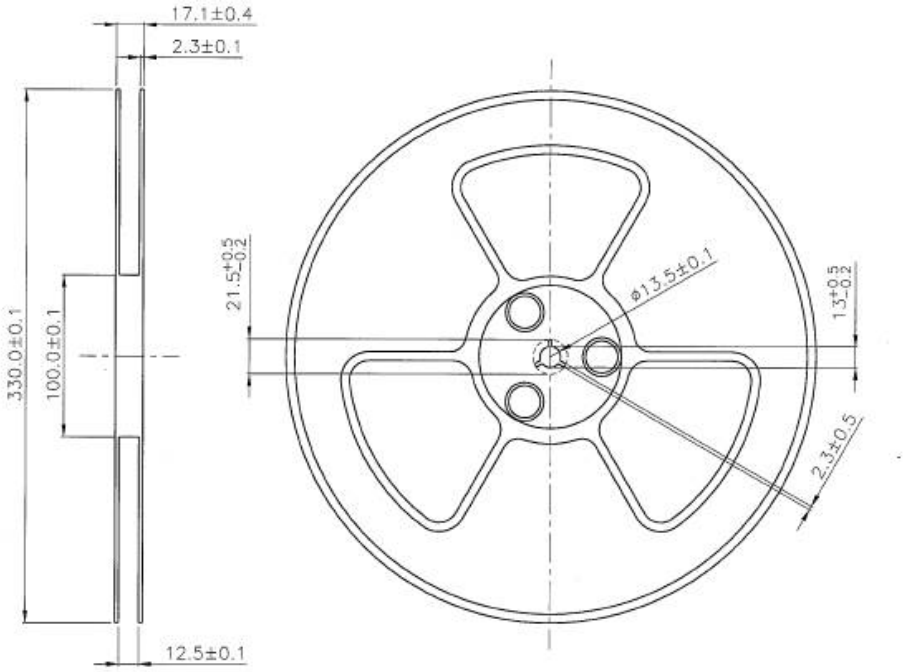
Note: All dimensions are in millimeters.

11 Package Dimension for Tape and Reel



Note:

11.1 All dimensions are in millimeters



Notes:

1. All dimensions are in millimeters (inches).
2. Empty component pockets sealed with top cover tape.
3. 13 inch reel – 8000 pieces per reel.
4. In accordance with ANSI/EIA 481-1-A-1994 specifications.

12 Revision Table

Version	Update	Page	Date
1.0	Final Datasheet –BE as created	Total 54	18-Jun-17
1.1	Add Figure 4.6.7-10 (Page 12-13) Update Figure 4.6.5 (Page 11), update PS_VCSEL current notation in the register table (Page 22)	Total 56	5-Jul-17