품 표 준

(LTY460HQ05-A01)

VER 0.0

LCD사업부
TV개발 2팀

■ Revision History

No	일자	페이지	개정전 사양	개정후 사양	비고
00	12.01.16	-	최초제정		-

1. 목적

제품 정보를 정의하고 개발제품 Target을 설정하며, 이를 부서간에 공유하기 위함.

2. 적용범위

TFT LCD 모듈 : LTY460HQ05-A01

3. 일반개요

3.1 개요

LTY460HQ05-A01은 비정질 실리콘(Amorphous Silicon) 박막 트랜지스터(TFT; Thin Film Transistor)를 스위칭 소자로 사용한 컬러 능동 행렬(Color active matrix) 방식의 TFT 액정 표시소자(LCD;Liquid Crystal Display) Module이다.

Module은 Panel, 구동 회로부와 Backlight부로 구성되며, Interface방법은 Digital 영상정보를 직렬로 고속 전송하는 방식의 일종인 Mini-LVDS 방식을 채용하였다.

본 제품은 1,920 * 1080(16:9) 화소를 포함하고, 16.7M의 색상을 지원한다. 그리고 독자 기술인 SPVA Mode 기술을 적용하여 시야각은 상하좌우 90° 제공하는 광시야각 제품이다.

3.2 특징

① High Contrast Ratio & High aperture structure
② 고속 응답 특성(DCC1.5 적용 회로 채용)
③ Wide XGA (1,920 x 1,080 화소) 지원 (16:9)
④ SPVA (Super Patterned Vertical Align) Mode 광시야각(±178°)
⑤ Edge w-LED방식 B/L UNIT 채택
⑥ Mini LVDS INTERFACE

3.3 응용분야

① Home-alone Multimedia TFT-LCD TV
② Full High Definition TV Ready (F-HD TV Ready)
③ AV 제품의 화상 표시 단말기

3.4 일반사양

항 목	사 양	단 위	비 고
유효표시면적	1018.08(H) x 572.67(V)	mm	ACTIVE
구동소자	a-Si TFT Active matrix		
표현가능색 수	1.07Giga(10 Bits-True)	color	
화소수	1,920 × 1,080	pixel	16:9
화소배열	RGB Vertical Stripe		
화소크기	0.53025(V) × 0.17675(H) * 3	mm	Pixel pitch
표시모드	Normally Black		
표면처리	Haze 2.3% +-2.1, Hard-Coating (2H)		VH-01

4. 기구사양

Item		Min.	Typ.	Max.	Note
Module size	Horizontal (H)	1,047.9	1,048.9	1,049.9	mm
	Vertical(V)	602.3	603.3	604.3	mm
	Depth(D)	24.2	25.2	26.2	mm
Weight		8,800	9,800	10,800	g

Note(1) Tolerrence ± 1.0 .표기

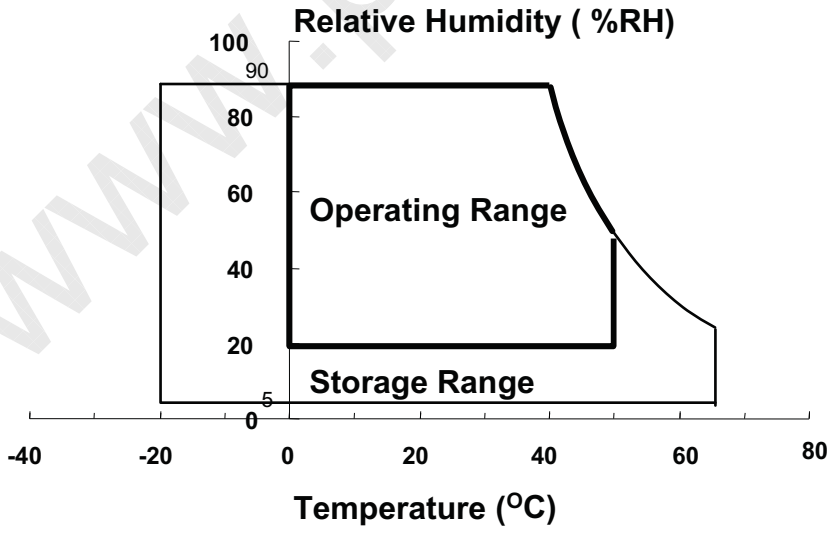
5. 절대 최대 정격

5.1 환경 사양 절대 정격

ITEM	SYMBOL		MIN.	MAX.	UNIT	NOTE
Storage temperature	39page : 14.2Storage 참조					
Operating temperature	TOPR		0	50	℃	**(1)**
Panel surface temperature	Tsur		0	65	℃	**(2)**
Shock(Non-operating)	Snop	+-x,y	-	40	G	**(3)**
		+- z		30		
Vibration(Non-operating)	Vnop		-	1.5	G	**(4)**

NOTE (1) 온도와 상대습도 관계는 아래 그림에 따른다.
(최대습구 온도는 39℃임 <40℃에서 93.8%RH에 해당>)

NOTE (2) 동작중 Panel의 표면온도로서 일부범위에서는 화질상의 문제가 발생할수 있지만, 편광판등의 자재가 영구적인 손상을 받지않는 범위임.



NOTE (3) 11ms ±X,Y40G / ±Z30G (6방향 / 1회)

NOTE (4) 10~300Hz / 1.5G /10 minSR, XYZ, 30 min/axis

5.2 전기적 사양 절대 정격

5.2.1 TFT LCD MODULE 절대 정격

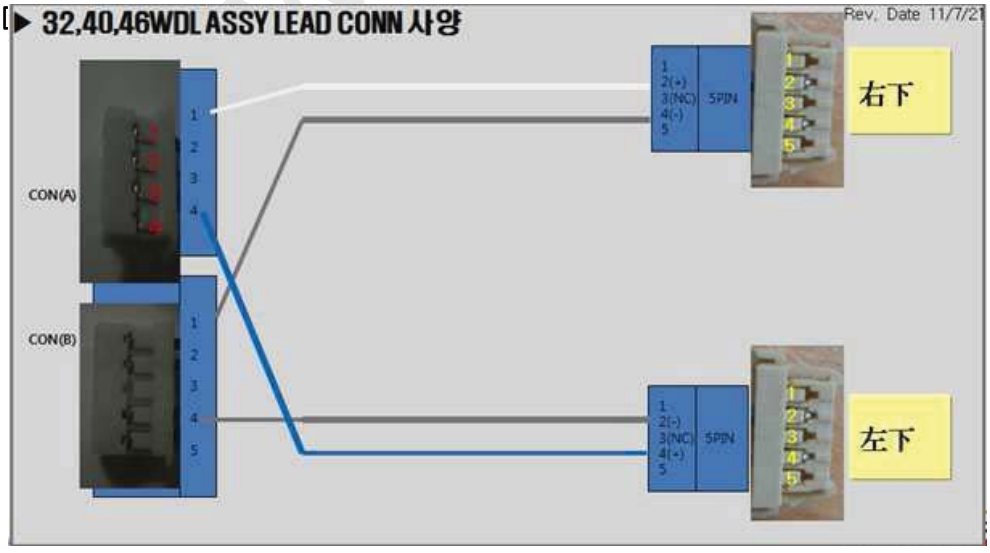
(V_{DD} = 12V)

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Power Supply Voltage/ Display	V_{DD}	V_{DD}-1	V_{DD}+1	V	**(1)**

NOTE(1) 동작온도 범위안에서.

5.2.2 LED UNIT Absolute Maximum Rating

ITEM	SYMBOL	최대정격	Condition
Operating temperature range	Top	-40 ~ 85℃	
Storage temperature range	Tstg	-40 ~ 100℃	
Junction Temperature	Tj	150℃	
Forward current	IF	260mA	operating current 100mA
Forward voltage	VF	5.95 ~ 6.65	IF=100mA
Reverse Voltage	VR	0.7 ~ 1.2V	IR = 5mA
Thermal resistance, Junction to Solder	Rth,JS	20< K/W	
Assembly Process Temp.		260℃, < 10 sec	
ESD		5 KV	HBM



6. 광학 특성

6.1 측정 환경

-. 환경 조건

온도 : 25℃±2℃ / 습도 : 25%~85% RH / 압력 : 86kPa~106kPa / 암실 : 1Lux이하 / 무풍(직접적인 바람 제거) / 무진동

-. Warm-Up Time : ① 최소 30분 이상

② 주기적(약 15초 간격)으로 center 휘도를 측정하여 10분전 휘도 와 현재 휘도 차이의 비가 0.5%이하가 되는 최초 시점

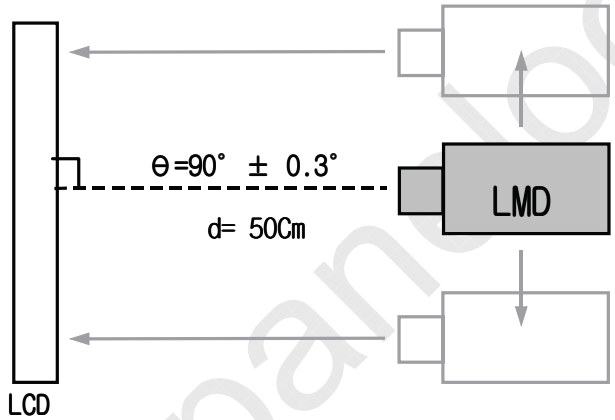
$$T_{warm\text{-}up} = \left(\left| Lum_{t-10} - Lum_{now} \right| / Lum_{now} \right) \times 100 < 0.5 \text{ 가 되는 시간}$$

where , Lum_{t-10}는 10분전 휘도 , Lum_{now}는 현재 휘도

6.2 측정 장비(LMD : Light Measurement Device)

-. 종류 : SR-3

-. 측정 거리 및 방향 :



LMD	Field
BM-5A	2°
BM-7	2°/ 1°
PR-650	1°
XR-3	1°

6.3 구동 조건

-. TFT LCD Module : VCC = 12.0 V, fV = 60 Hz, fDCLK = 148.5 MHz

-. BACK-LIGHT UNIT : Dimming = 20~ 100%

6.4 광학 특성

광특성은 Note (4)의 방법으로 암실에서 측정한다.

측정장비 :BM-5A, BM-7(Topcon社), EZ-Contrast(Eldim社) PR650(Photo Research社)

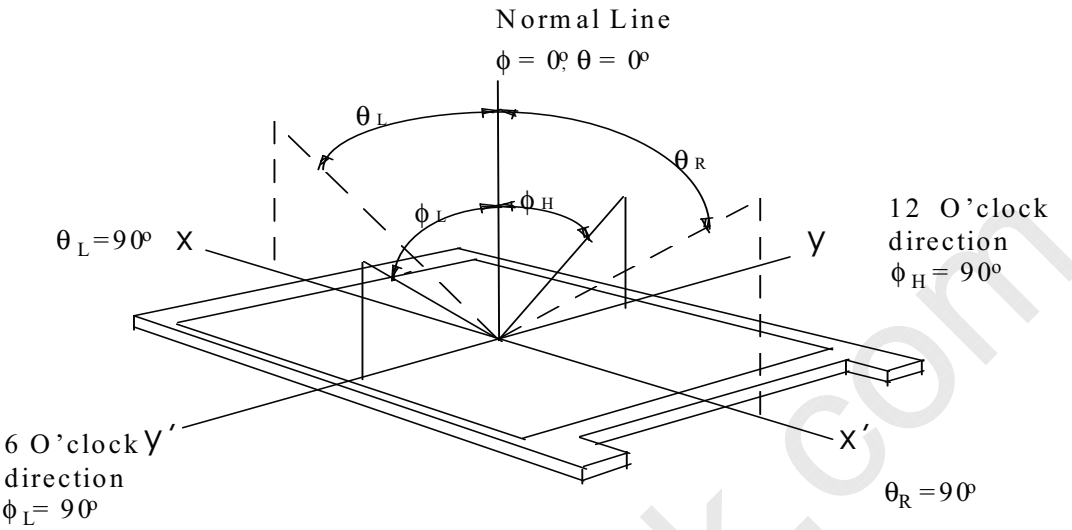
Ta= 25±2℃, VDD=12.0V, fv=60Hz, fDCLK=148.5MHz, Dim=100%

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Contrast Ratio (center)		C/R	Normal	3000	4000	-		(2)의 ① BM-5A
Response time	G-to-G [AVE]			-	3.5	12	msec	(3) BM-7
Luminance of White (center)		YL		380	450	-	cd/m²	(2)의 ② BM-5A
Color Chromaticity (CIE 1931)	Red	RX	(Φ=0, θ=0) Viewing Angle	TYP -0.03	0.642	TYP +0.03		(1) SR-3A
		RY			0.331			
	Green	GX			0.313			
		GY			0.608			
	Blue	BX			0.155			
		BY			0.056			
	White	WX			0.280			
		WY			0.285			
Viewing Angle	Hor.	θL	C/R≥10	79	89	-	Degrees	(1) EZ-Contrast
		θR		79	89	-		
	Ver.	ΦH		79	89	-		
		ΦL		79	89	-		
Color Gamut				-	72	-	%	
Color Temperature		K		-	10000	-		
Gamma		γ	7G~57G (Full=64G)	1.7	2.2	2.7		(9)
Flicker		F		-	-	30		(5)
Crosstalk		DSHA	0G-13G	-	-	30		(6)
			14G-64G			8		
Brightness Uniformity (9 Points)		Buni		-	-	30	%	(2)의 ③ BM-5A

C/R = (White at point ⑤ of Note 2) / (Most Dark Point of Black Pattern at area ⓐ of Note 2)

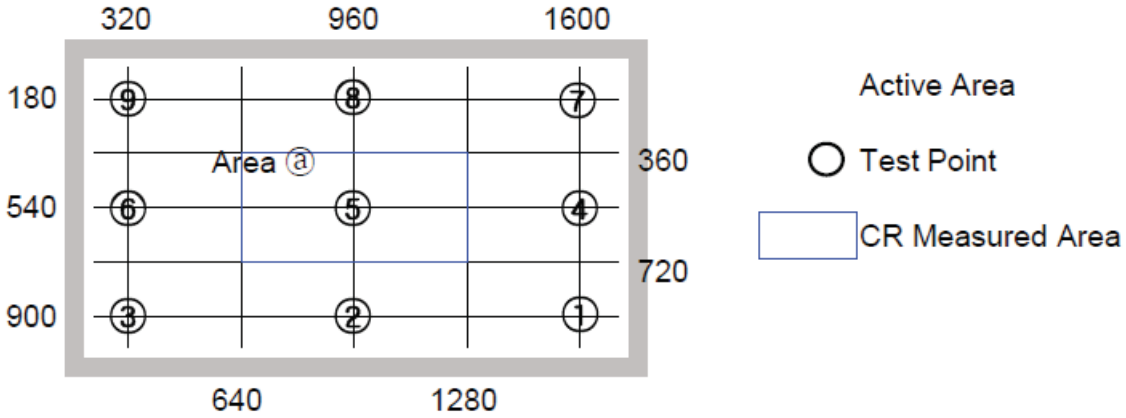
NOTE (1)

시야각(Viewing angle)의 정의 : C/R이 10이상되는 시각의 범위



NOTE (2)

측정위치 : 판넬상 측정위치는 9개 점으로 한다.



① 대비비(C/R : Contrast ratio)

: 측정위치 중앙(Point ⑤)에서 White 상태(G_{MAX})와 Black 상태(G_{MIN})의 비로 정의.

$$C/R = \frac{\text{판넬상에서 WHITE 상태 휘도}}{\text{판넬상에서 BLACK 상태 휘도}}$$

② White 휘도의 정의 (Y_L) :

측정위치 중앙(Point ⑤)의 white 휘도(Y_L) 를 측정한 값.

③ Brightness Uniformity(Buni) :

측정 화면 : Fully White

측정화면상의 9개의 휘도를 측정, 아래와 같이 정의한다.

$$\frac{B_{max} - B_{min}}{B_{max}} \times 100$$

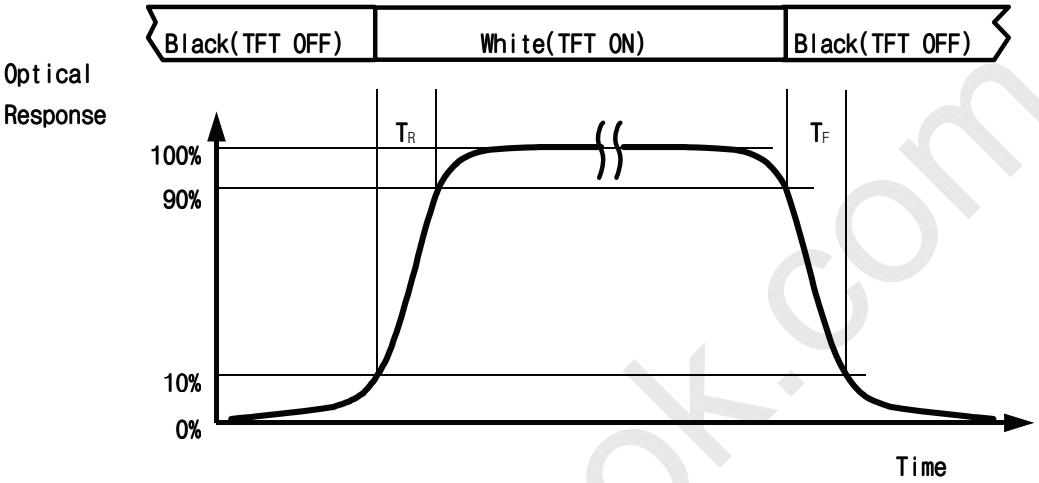
where, Bmax = Maximum brightness

Bmin = Minimum brightness

NOTE (3)

응답시간(Response time)의 정의

: 화면이 어두어 질 때와 밝아질 때에 투과율이 10%와 90%사이로 변화하는 시간의 합.



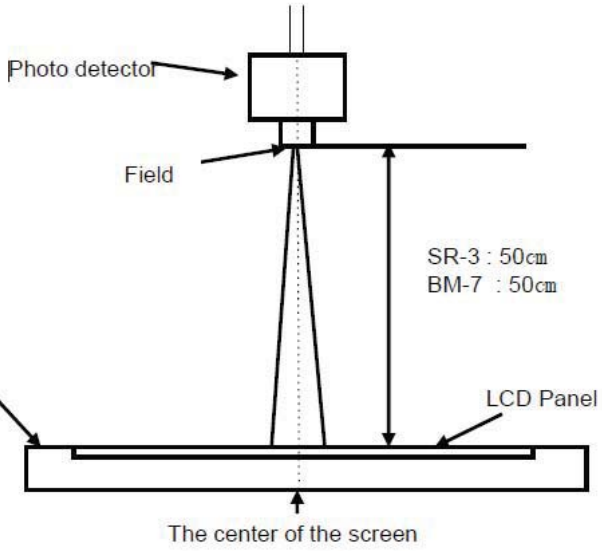
NOTE (4)

상온에서 30분 방치 후 정격에서 백라이트를 켜고 30분 후에 측정.

환경조건: 주위 온도 : 25℃±2℃

암실, 무풍(직접적인 바람제거), 무진동

Photo detector	Field
SR-3	1°
BM-7	2°

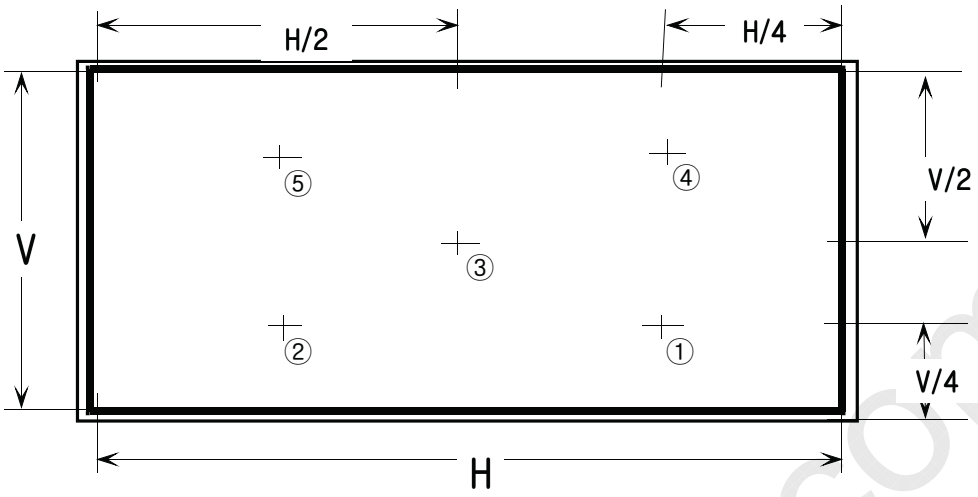


NOTE (5)

▶ 화면의 번쩍 거림(Flicker)의 정의 : LCD Panel의 화면이 깜박거리는 현상.

① 계산식은 Flicker 측정표준에 준함.

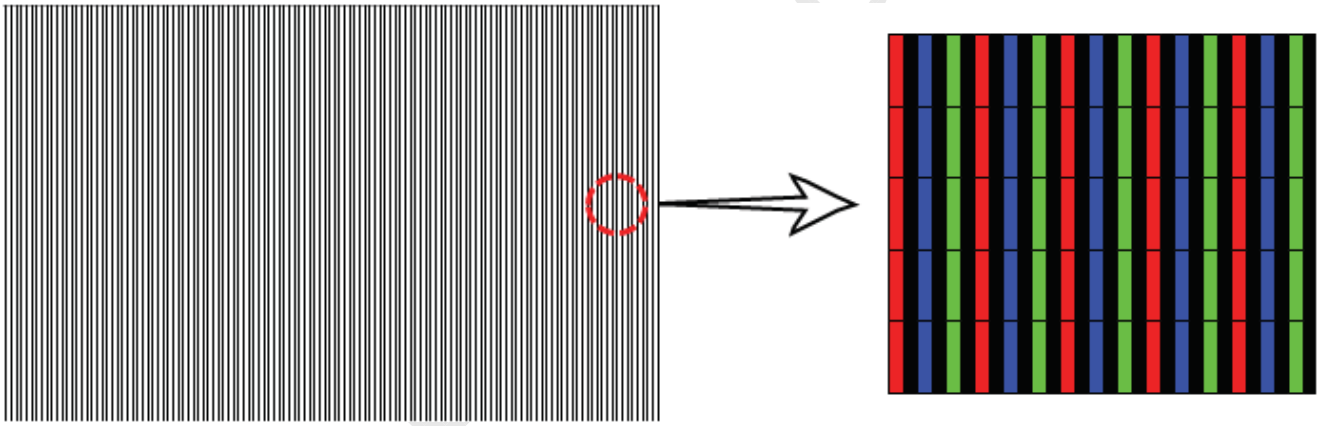
② 측정위치



③ 위 5point 평균을 Flicker로 정한다.

④ Flicker 측정 Pattern :

- Sub Vertical Stripe 32G



NOTE (6)

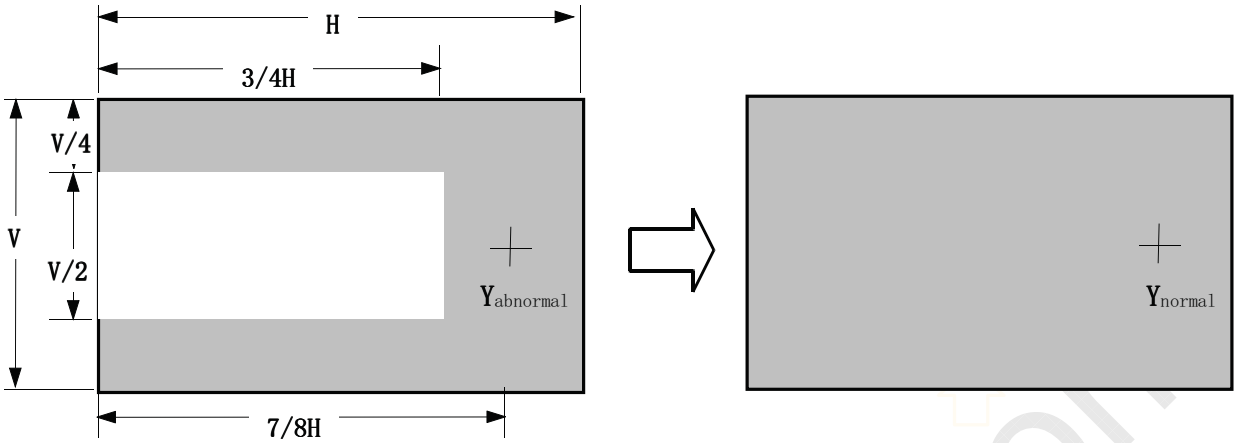
▶ 상호 혼선(Crosstalk;Cross modulation)의 정의(DSHA): 화소간의 신호간섭에 의하여 대비비가 저하되는 현상.

$$Crosstalk\ Modulation\ \ Ratio(D_{SHA}) = \frac{|Y_{normal} - Y_{abnormal}|}{Y_{normal}} \times 100(\%)$$

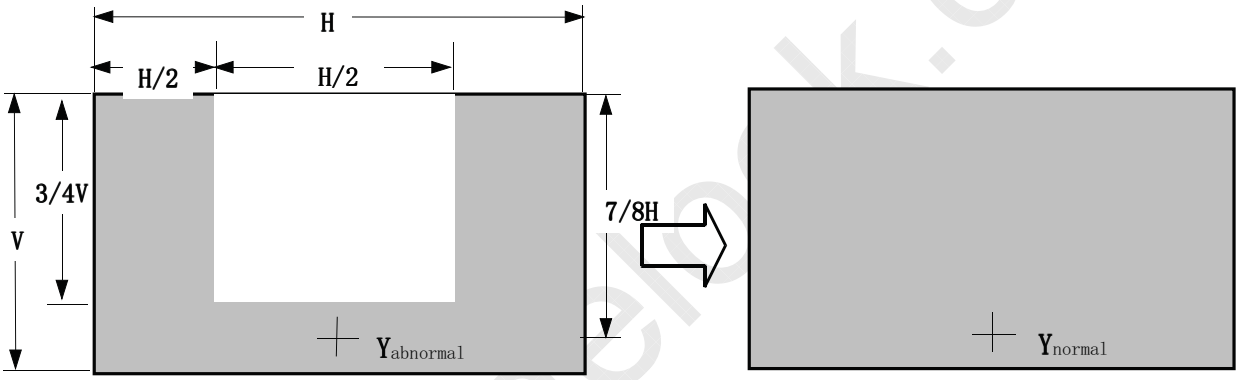
* White Box 이외의 back ground pattern은 Gray1~ Gray64 까지 4Gray 간격으로 측정
* Horizontal Crosstalk 과 Vertical Crosstalk을 모두 측정
* 측정 결과 중 가장 큰 값을 Crosstalk라고 정의

참고 : Normally White mode시 Box는 Black(Gmin) /Normally Black mode시 Box는 white(Gmax)

* Crosstalk 측정 Pattern 및 Point



Horizontal Crosstalk



Vertical Crosstalk

Note (9) Definition of 2 point Gamma

$$Gamma = \log(X_{lum}/100)/\log(Y/100)$$

$$X_{lum} = (Z - B_{\min})/(B_{\max} - B_{\min}) \times 100$$

Y: Measurement Level / Z: Measurement Brightness

B_{max}: *Maximum Brightness* / B_{min}: *Minimum Brightness*

7. 전기적 특성

7.1 TFT LCD 모듈

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Power Supply Voltage	VDD	11	12	13	V	(1)
Interface Type	Mini-LVDS	Tcon 내장형				
Power Consumption	(a) Black	-	1180	1520	mA	(2),(3), (5)
	(b) White	-	1220	1610	mA	
	(c) Mosaic	-	1160	1510	mA	
	(d)Max(H-Stripe)	-	1820	2380	mA	
Hsync Frequency	fH	-	67.5	-	kHz	
Vsync Frequency	fV	-	60	-	Hz	
Main Frequency	fDCLK	-	148.5	-	MHz	
Rush Current	IRUSH	-	-	5	A	(4)

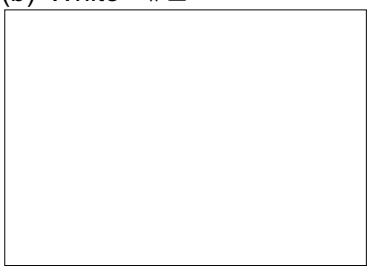
NOTE(1) 디스플레이 데이터 및 타이밍 신호용 콘넥터는 연결되어 있을 것(V_{SS} = 0V)

(2) f_V = 60 Hz, f_{DCLK} = 148.5 MHz, V_{DD} = 12.0V, DC current

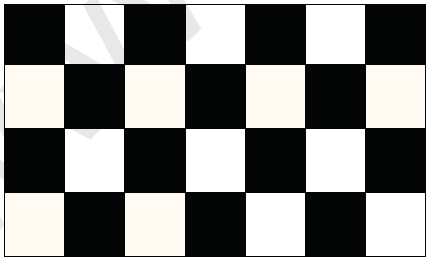
(3) 소비전력 체크 패턴

(a) Black 패턴

(b) White 패턴

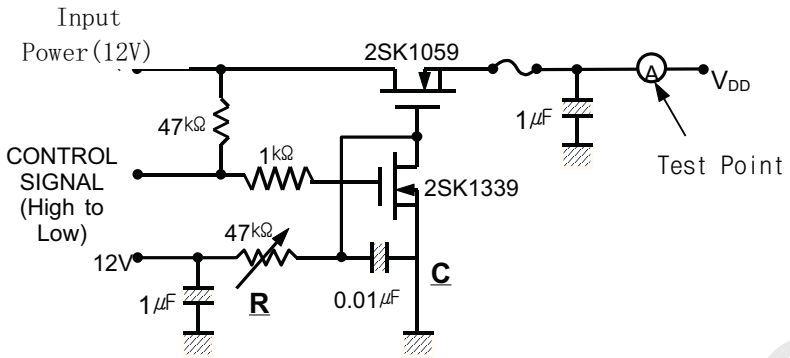


(c) Mosaic 패턴

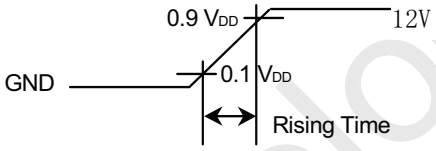


(d) Max 패턴 (H-stripe)

(4) 측정조건 (12V 구동, rising time =0.47ms)



Note : Control Signal : High(+12V) -->Low(Ground)
All Signal lines to panel except for power 12V : Ground
The rising time of supplied voltage is controlled to 0.47ms by R and C value.



(5) Balance board의 소비전류는 포함하지 않은 상태임.

7.2 Operation temperature range at specific component

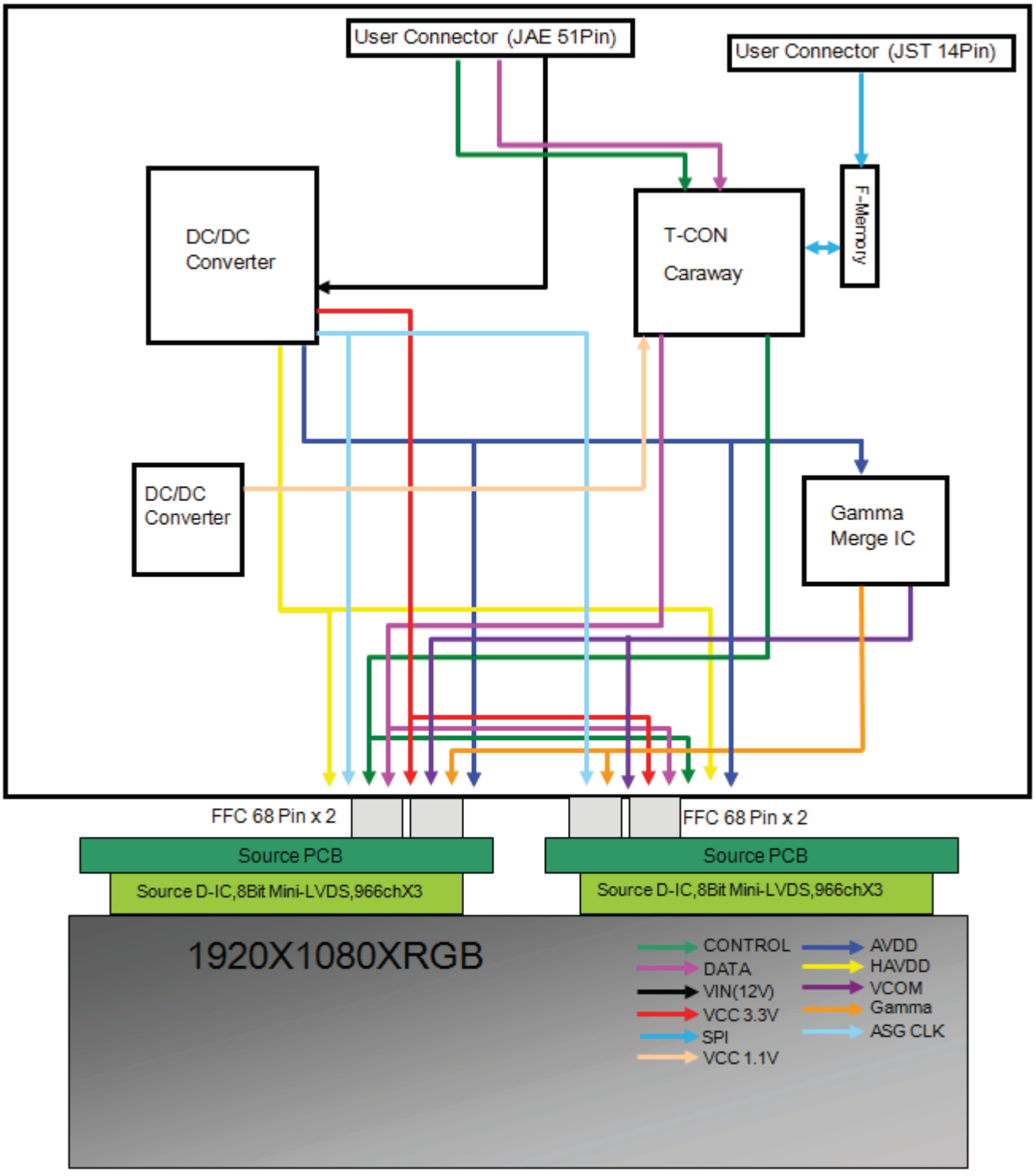
Part	Spec	Ambient Operating Temperature	Junction Operating Temperature
Timing Controller	Caraway	0℃ ~ 70℃	0℃ ~ 125℃

7.3 LED Driver

No.	ARTICLE	SPECIFICATION					
		기호	MIN	TYP	MAX	UNIT	비고
1	Operating Voltage	Vop	269	287	306	V	@140mA/module @ Tj-20℃
		Vop	262	280	298	V	@140mA/module @ Tj 0℃
		Vop	254	272	290	V	@140mA/module @ Tj 25℃
		Vop	247	264	281	V	@140mA/module @ Tj 60℃
		ΔVf	-	-	11.5	V	@140mA/module @ Tj 25℃
2	Color Chromaticity	x	0.265	0.275	0.285		@140mA/module
		y	0.232	0.242	0.252		@140mA/module

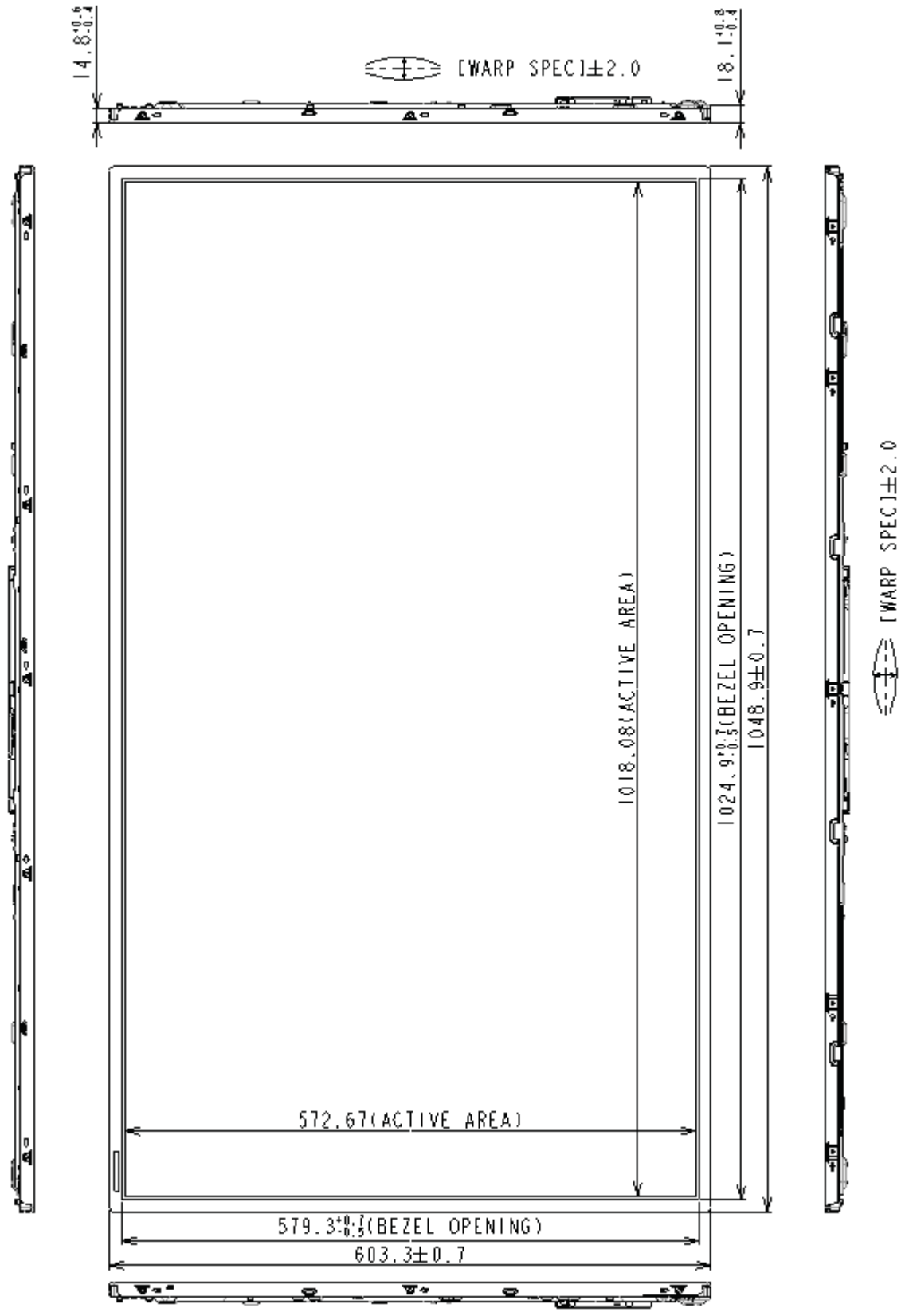
8. 블럭 다이어그램(Block Diagram)

8.1 Input circuit 등가회로

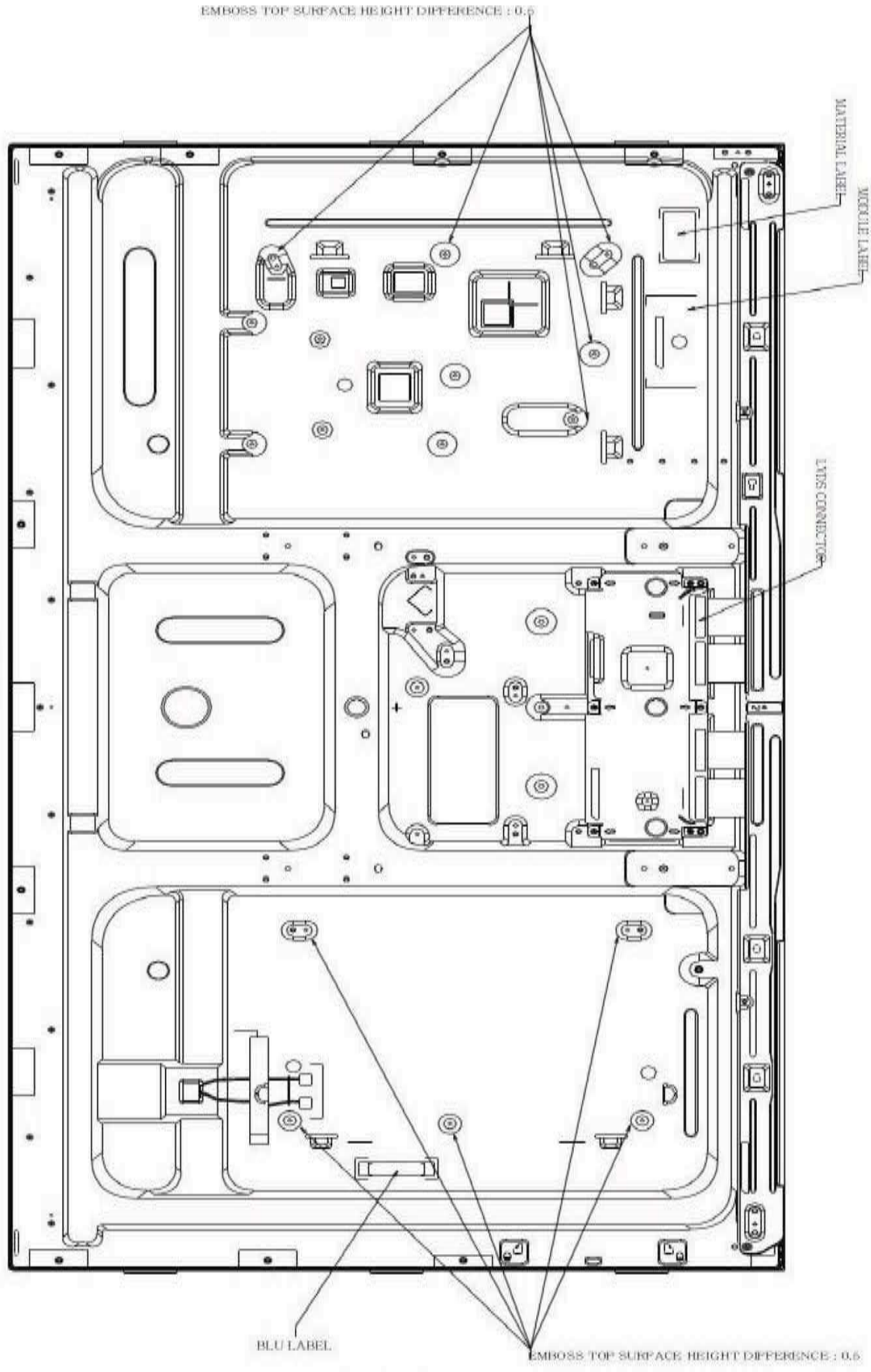


8.2 Back Light

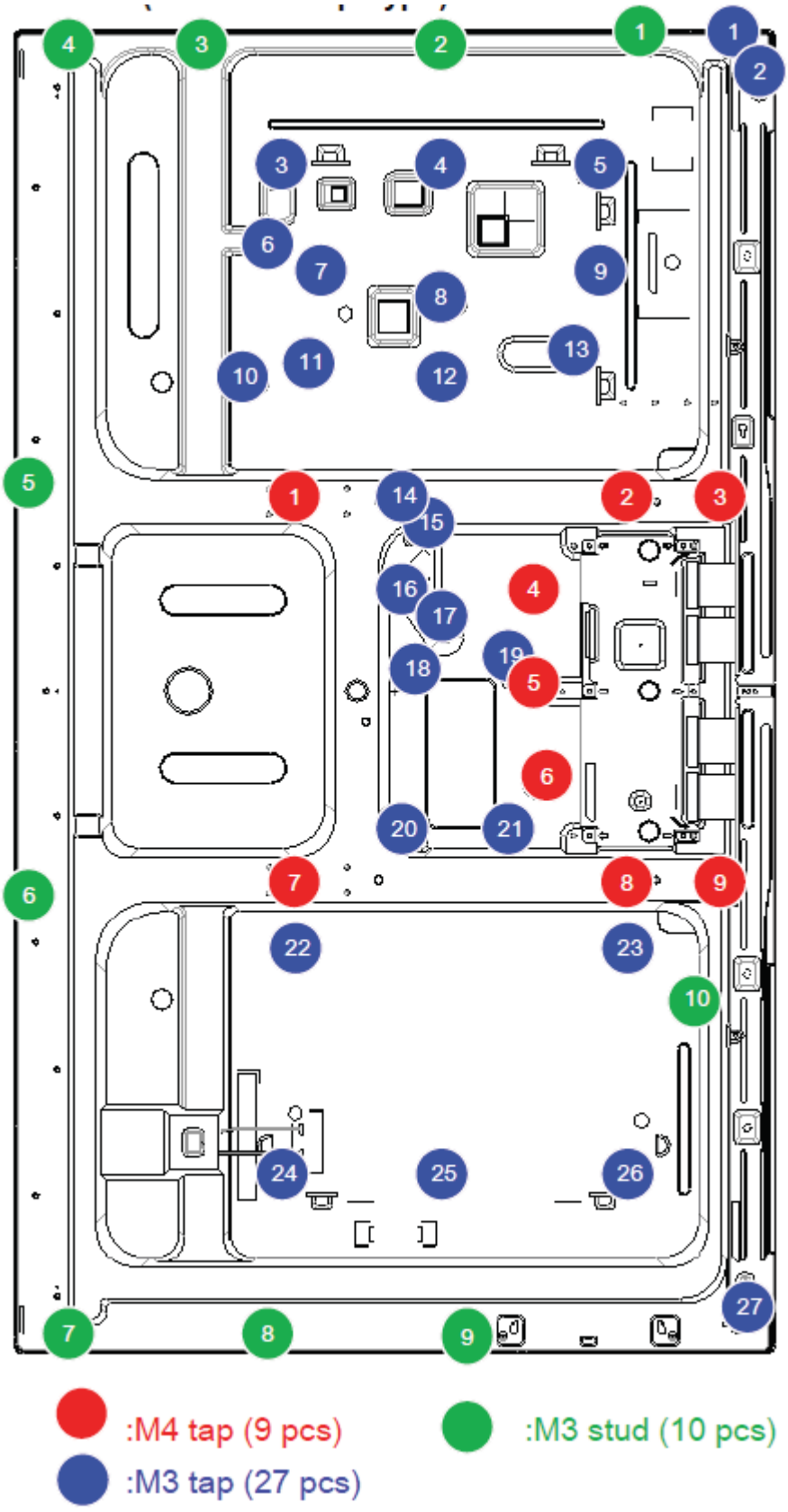
* Front



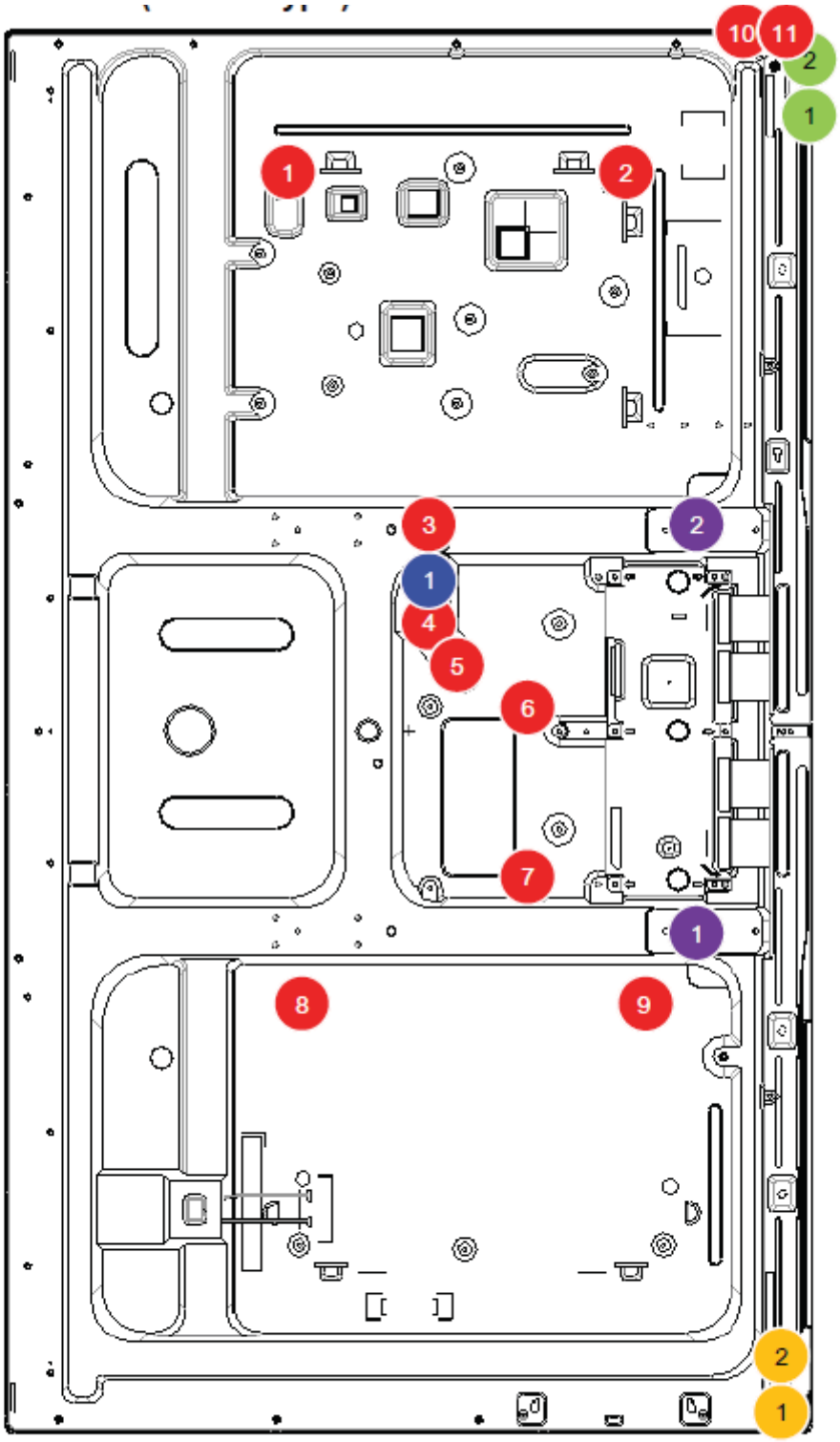
*Back



*Outline dimension (Stud and Tap Type)



*Outline dimension (Dowel Type)



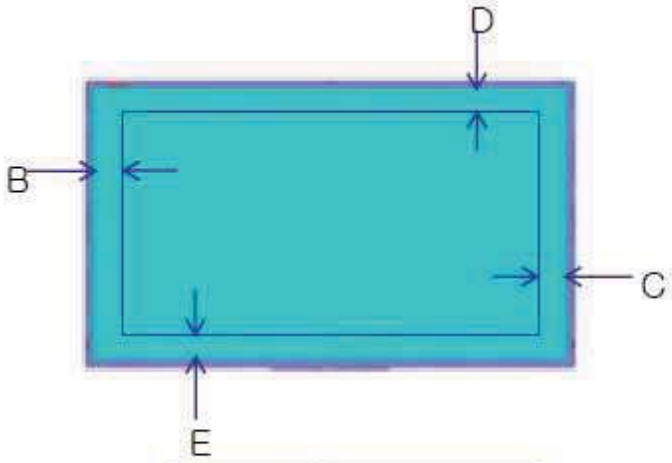
:Type B1 (15 pcs)
:Type B3 (2 pcs)
:Type S1 (2 pcs)
:Type B2 (1 pc)
:Type S2 (2 pcs)

*General item

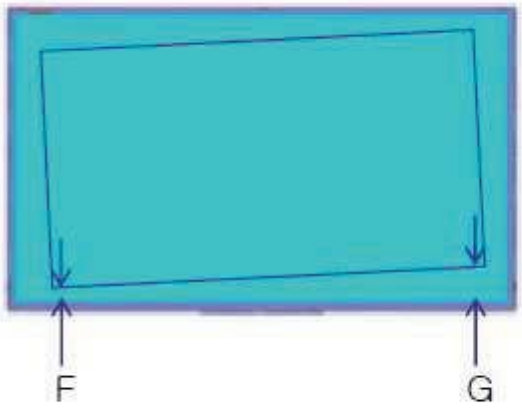
●General tolerance

Distance (mm)	X ≤ 16	16 < X ≤ 64	64 < X ≤ 256	256 <X≤ 512	512 <X≤ 1024	1024 < X	Bending Angle
Tolerance	±0.1	±0.2	±0.3	±0.45	±0.6	±0.8	±1°

●Black matrix



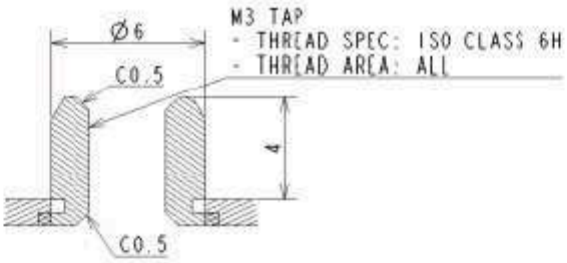
|B-C|	① Max 2
|D-E|	② Max 2



|F-G|	③ Max 2

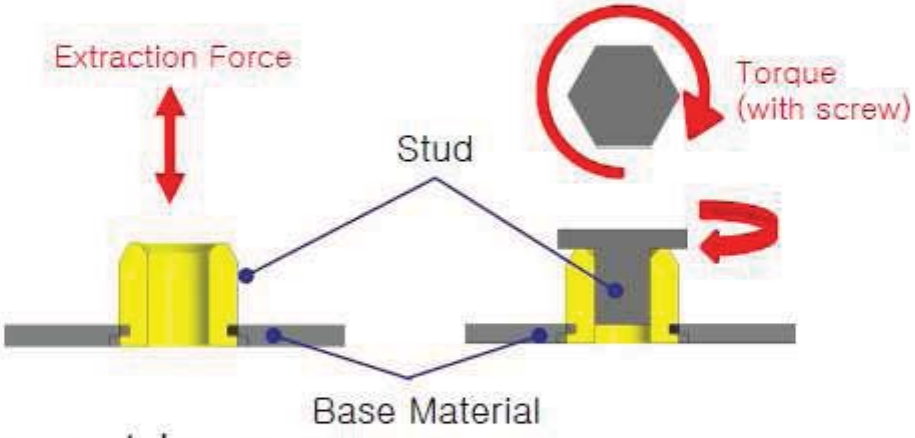
* Stud

•Stud dimension - M3 stud

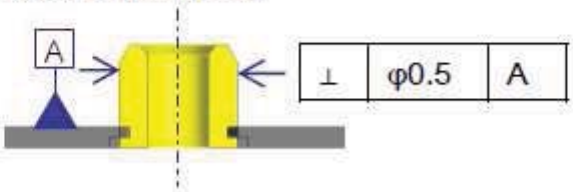


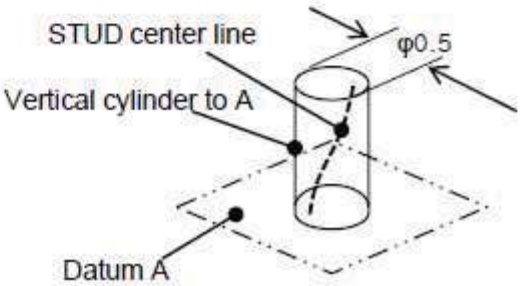
•Stud durability

Stud Type	Base Material	Extraction Force kN(kgf)	Torque N・m(kgf・cm)
		Min	Min
M3	Al	0.25(25)	2.1(21)
M4		0.42(43)	2.9(30)
M5	SECC	0.42(43)	5.9(60)
M6		0.84(86)	5.9(60)



•Stud squareness tolerance



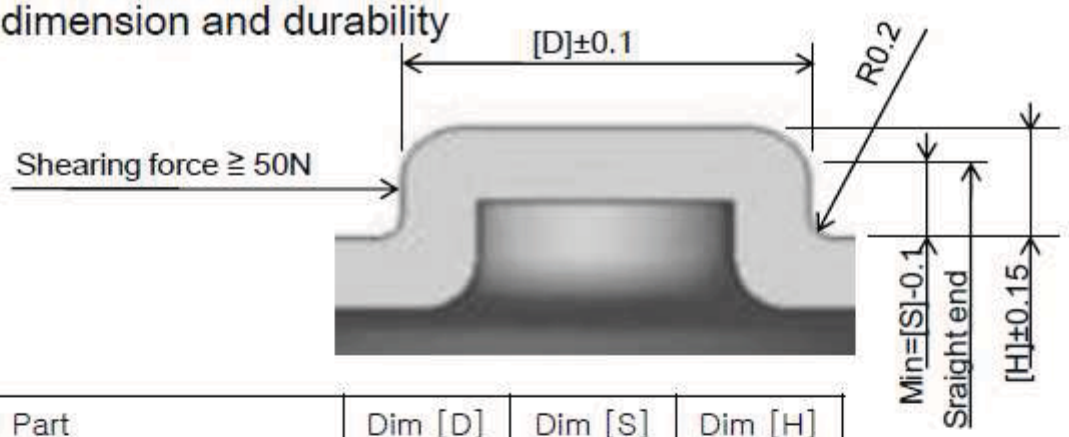


*) STUD center line should be in the vertical cylinder of φ0.5 to A.

Squareness definition

*Dowel and Tap

●Dowel dimension and durability



[mm]

Type	Part	Dim [D]	Dim [S]	Dim [H]
B1	BACK CHASSIS	4.2	0.5	1.5
B2	BACK CHASSIS	3.7	0.5	1.5
B3	BACK CHASSIS	6.0	1.0	3.0
S1	SOURCE SHIELD (R)	4.2	0.3	0.7
S2	SOURCE SHIELD (L)	4.2	0.3	0.9

●Tap dimension

- Thread compliant to ISO class 6H

●Tap durability

■The screw torque must satisfy the following.

M3 : 0.7N· m X 10 times

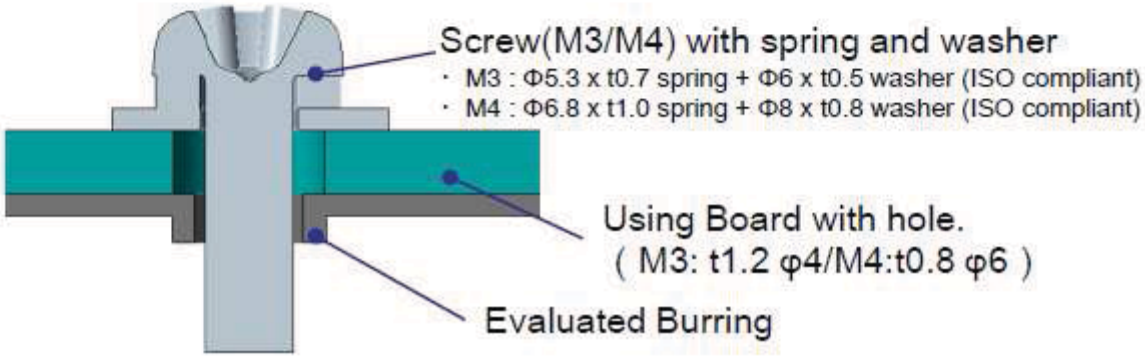
M4 : 1.0N· m X 10 times

※Standard driver : Nitto Kohki / Delvo DLV8231-EJN

■Evaluate all of burring tap using following board.

M3 Burring : Board thickness t1.2 / Hole size φ4

M4 Burring : Board thickness t0.8 / Hole size φ6



8.3 BACK-LIGHT UNIT 절대정격

The back light contains 88 LEDs.

The characteristics of LEDs are shown in the following tables.

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Operating Life Time		Hr	30,000	-	-	Hour	(1)
Operating Current	Continuous	Iop	-	140	260	mA	
Operating Voltage	Continuous	Vop	254	-	290	V	44LEDs /@140mA@Ta 25℃
Range of Voltage		ΔVf	-	-	11.5	V	@140mA(/String)

Note (1) It is defined as the time to take until the brightness reduces to 50% of its original value at each Srting, Iop=.140.0mArms

[Definition of Operating Voltage : At each Strings, Iop = 140.0 mArms (typ.)]

9. 입력단 신호 순서(Input Terminal Pin Assignment)

9.1 TFT LCD 모듈(Interface signal & power)

9.1.1 51Pin Connector : FI-RNE51SZ-HF (JAE)

No	Signal		No	Signal	
1	VIN	DC power supply	26	RE[0]P	Even LVDS Signal +
2	VIN	DC power supply	27	RE[1]N	Even LVDS Signal -
3	VIN	DC power supply	28	RE[1]P	Even LVDS Signal +
4	VIN	DC power supply	29	RE[2]N	Even LVDS Signal -
5	VIN	DC power supply	30	RE[2]P	Even LVDS Signal +
6	N.C.	No Connection	31	GND	Ground
7	GND	Groung	32	RECLKN	Even LVDS Signal -
8	GND	Ground	33	RECLKP	Even LVDS Signal +
9	GND	Ground	34	GND	Ground
10	RO[0]N	Odd LVDS Signal -	35	RE[3]N	Even LVDS Signal -
11	RO[0]P	Odd LVDS Signal +	36	RE[3]P	Even LVDS Signal +
12	RO[1]N	Odd LVDS Signal -	37	RE[4]N	Even LVDS Signal -
13	RO[1]P	Odd LVDS Signal +	38	RE[4]P	Even LVDS Signal +
14	RO[2]N	Odd LVDS Signal -	39	GND	Ground
15	RO[2]P	Odd LVDS Signal +	40	SET_SCL	I2C SCL
16	GND	Ground	41	SET_SDA	I2C SDA
17	ROCLKN	Odd LVDS Signal -	42	Option1	TV SET use only
18	ROCLKP	Odd LVDS Signal +	43	BINT	BUS RELEASE
19	GND	Ground	44	Option2	TV SET use only
20	RO[3]N	Odd LVDS Signal -	45	Option3	TV SET use only
21	RO[3]P	Odd LVDS Signal +	46	Option4	TV SET use only
22	RO[4]N	Odd LVDS Signal -	47	Option5	TV SET use only
23	RO[4]P	Odd LVDS Signal +	48	Option6	TV SET use only
24	GND	Ground	49	Option7	TV SET use only
25	RE[0]N	Even LVDS Signal -	50	Option8	TV SET use only
			51	Option9	TV SET use only

9.1.2 14 Pin Connector : 14FLT-SM2-C-TB (JST)

PIN No.	Signal	Description
1	N.C.	No Connection
2	N.C.	No Connection
3	/WP	SPI_WP
4	/CS	SPI_CS
5	CTRL	SPI_CTRL
6	GND	GND
7	CLK	SPI_CLK
8	GND	GND

PIN No.	Signal	Description
9	DO	SPI_DO
10	GND	GND
11	DI	SPI_DI
12	GND	GND
13	GND	GND
14	GND	GND

9.2입력신호와 표시색상과의 관계

COLOR	DISPLAY	DATA SIGNAL																								GRAY SCALE LEVEL
		RED								GREEN								BLUE								
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7	
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	-
	GREEN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	-
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
	RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	-
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	-
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
GRAY SCALE OF RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	DARK ↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R252
	↓ LIGHT	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R253
		0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R254
	RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R255
GRAY SCALE OF GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	DARK ↑	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G1
		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G252
	↓ LIGHT	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G253
		0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G254
	GREEN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G255
GRAY SCALE OF BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	DARK ↑	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	B1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	B2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B252
	↓ LIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	B253
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	B254
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	B255

NOTE

(1) Gray 정의 :

Rn : 빨강색 Gray, Gn : 녹색 Gray, Bn : 파란색 Gray (n=Gray level)

(2) 입력신호 : 0=Low level voltage, 1=High level voltage

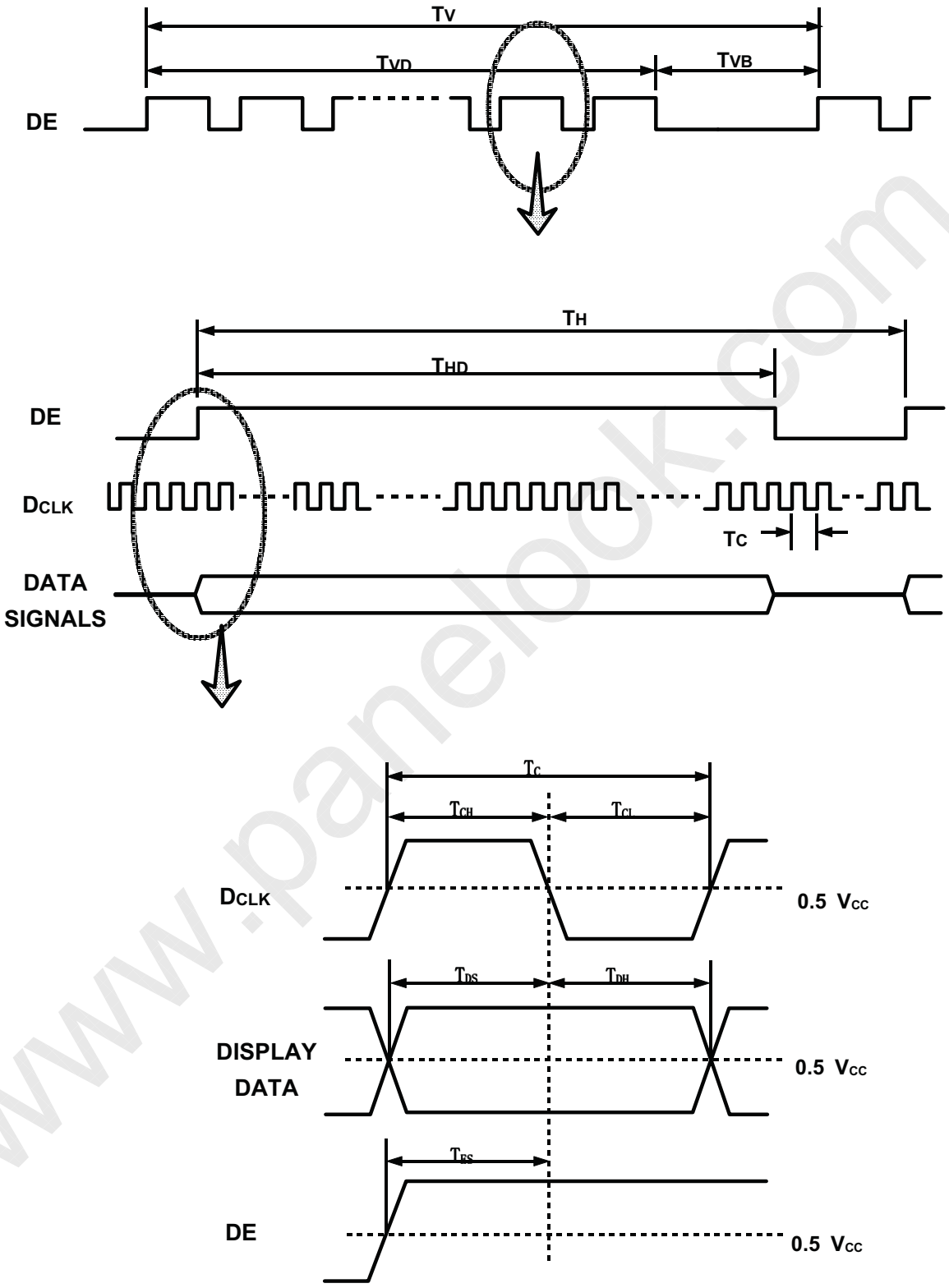
10. Interface Timing

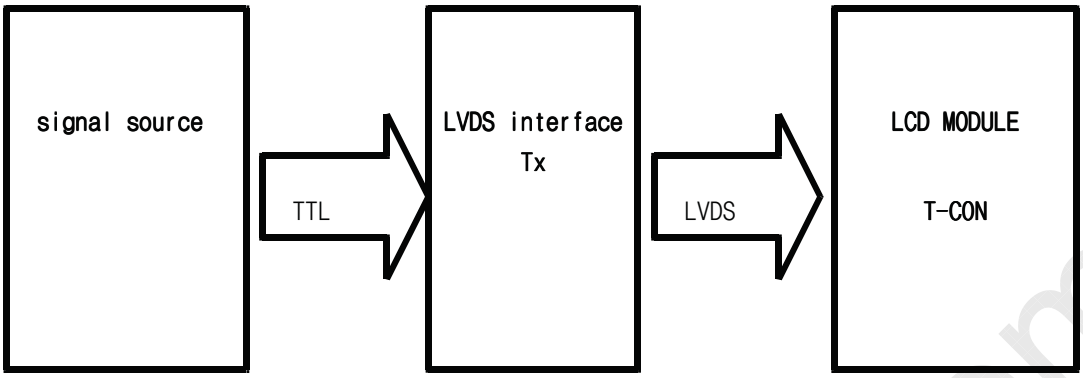
10.1 Time parameter(DE Mode)

SIGNAL	ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock	Frequency	1/Tc	-	148.5	-	MHz	-
Hsync		Fh	-	67.5	-	KHz	-
Vsync		Fv	-	60	-	Hz	-
Vertical Active Disply Term	Display Period	TVD	-	1080	-	lines	-
	Vertical Total	TV	-	1125	-	lines	-
Horizontal Active Display Term	Display Period	THD	-	1920	-	clocks	-
	Horizontal Total	TH	-	2200	-	clocks	-

→ 본 제품은 DE only mode로 동작하며, H-sync와 V-sync신호의 입력여부는 정상적인 동작에 영향을 주지 않음.

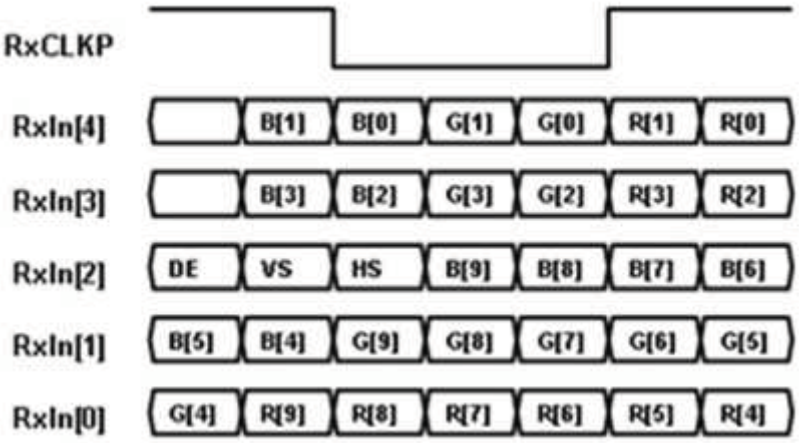
10.2 인터페이스 신호의 타이밍 다이어그램(DE Mode)





- LVDS Transmitter : DS90C385MTD (N/S) / THC63LVDM83A(THINE) : Recommand

- LVDS Data Interface (Odd & Even Channel Same Data Format)



RECOMMENDED TRANSMITTER INPUT CHARACTERISTICS

-OVER RECOMMENDED OPERATING SUPPLY AND TEMPERATURE RANGES UNLESS OTHERWISE SPECIFIED.

SYMBOL	PARAMETER	MIN.	TPY.	MAX.	UNITS.
TCIT	TxCLK IN TRANSITION TIME (FIG2)	1.0	-	6.0	ns
TCIP	TxCLK IN PERIOD (FIG3)	11.76	T	50	ns
TCIH	TxCLK IN HIGH TIME (FIG3)	0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN LOW TIME (FIG3)	0.35T	0.5T	0.65T	ns
TXIT	TxCLK TRANSITION TIME	1.5	-	6.0	ns

TRANSMITTER SWITCHING CHARACTERISTICS

-OVER RECOMMENDED OPERATING SUPPLY AND TEMPERATURE RANGES UNLESS OTHERWISE SPECIFIED.

SYMBOL	PARAMETER		MIN.	TPY.	MAX.	UNITS.
LLHT	LVDS LOW TO HIGH TRANSITION TIME (FIG1)		-	0.75	1.5	ns
LHLT	LVDS HIGH TO LOW TRANSITION TIME (FIG1)		-	0.75	1.5	ns
TPPos0	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 0 (FIG 7) NOTE 1	F = 40MHZ	-0.25	0	0.25	ns
TPPos1	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 1		3.32	3.57	3.82	ns
TPPos2	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 2		6.89	7.14	7.39	ns
TPPos3	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 3		10.46	10.71	10.96	ns
TPPos4	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 4		14.04	14.29	14.54	ns
TPPos5	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 5		17.61	17.86	18.11	ns
TPPos6	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 6		21.18	21.43	21.68	ns
TPPos0	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 0 (FIG 7) NOTE 1	F = 65MHZ	-0.20	0	0.20	ns
TPPos1	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 1		2.00	2.20	2.40	ns
TPPos2	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 2		4.20	4.40	4.60	ns
TPPos3	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 3		6.39	6.59	6.79	ns
TPPos4	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 4		8.59	8.79	8.99	ns
TPPos5	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 5		10.79	10.99	11.19	ns
TPPos6	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 6		12.99	13.19	13.39	ns
TPPos0	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 0 (FIG 7) NOTE 1	F = 85MHZ	-0.20	0	0.20	ns
TPPos1	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 1		1.48	1.68	1.88	ns
TPPos2	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 2		3.16	3.36	3.56	ns
TPPos3	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 3		4.84	5.04	5.24	ns
TPPos4	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 4		6.52	6.72	6.92	ns
TPPos5	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 5		8.20	8.40	8.60	ns
TPPos6	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 6		9.88	10.08	10.28	ns
TSTC	TxIN SETUP TO TxCLK IN (FIG 3)		2.5	-	-	ns
THTC	TxIN HOLD TO TxCLK IN (FIG 3)		0	-	-	ns
TCCD	TxCLK IN TO TxCLK OUT DELAY (FIG4)	Ta = 25 ℃, Vcc = 3.3 V	3.8	-	6.3	ns
	TxCLK IN TO TxCLK OUT DELAY (FIG4)		2.8	-	7.1	ns
TJCC	TRANSMITTER JITTER CYCLE TO CYCLE (FIG 8,9)	F=85 MHZ	-	110	150	ps
		F=65 MHZ	-	210	230	ps
		F=40 MHZ	-	350	370	ps
TPLLS	TRANSMITTER PHASE LOCK LOOP SET (FIG 5)		-	-	10	ms
TPDD	TRANSMITTER POWER DOWN DELAY (FIG 6)		-	-	100	ns

note1)The minimum and maximum limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. this parameter is functionality tested only on automatic test equipment (ATE)

note2)The limits are based onbench charaterization of the device's jitter response over the power supply voltage range. output clock jitter is measured with a cycle to cycle jitter of ± 3ns applied to the input clock signal while data inputs are switching (fig8,9).A jitter event of 3 ns, represents worse case jump in the clock edge from most graphics controller VGA Cihps currently available. this parameter is used when calculating system margin as descrbed in AN-1059.

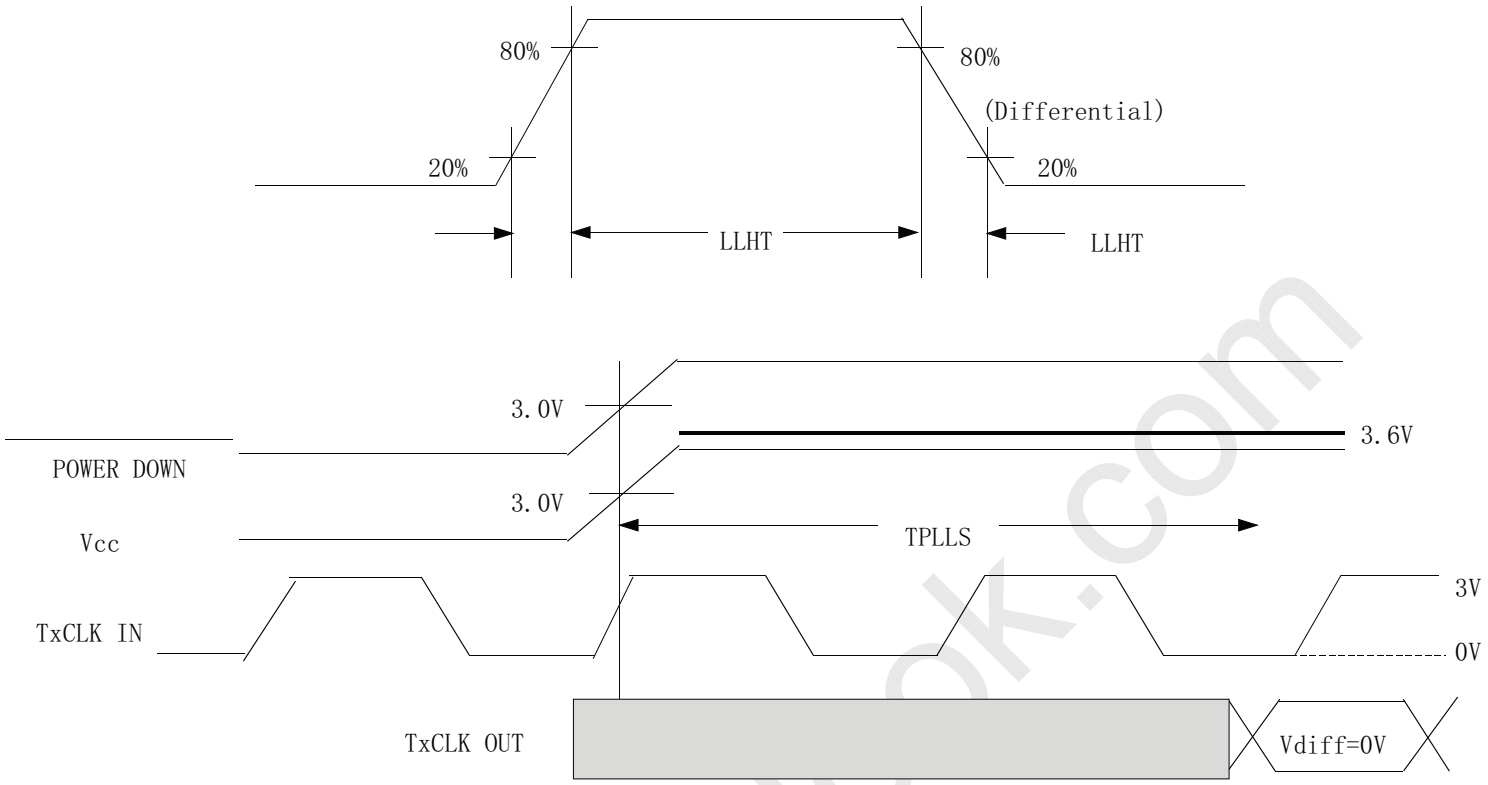


FIGURE 5.Transmitter Phase lock loop(PLL) SET-UP TIME

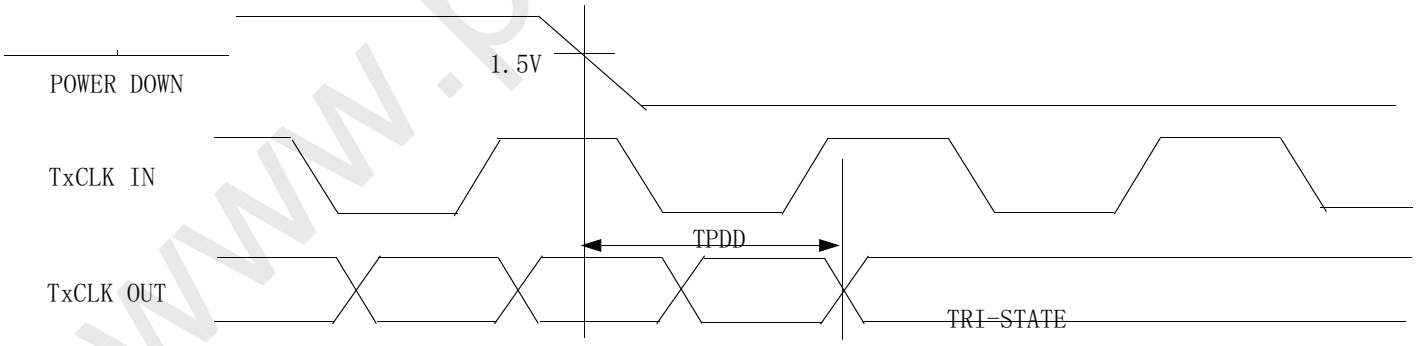


FIGURE 6.Transmitter Power down delay

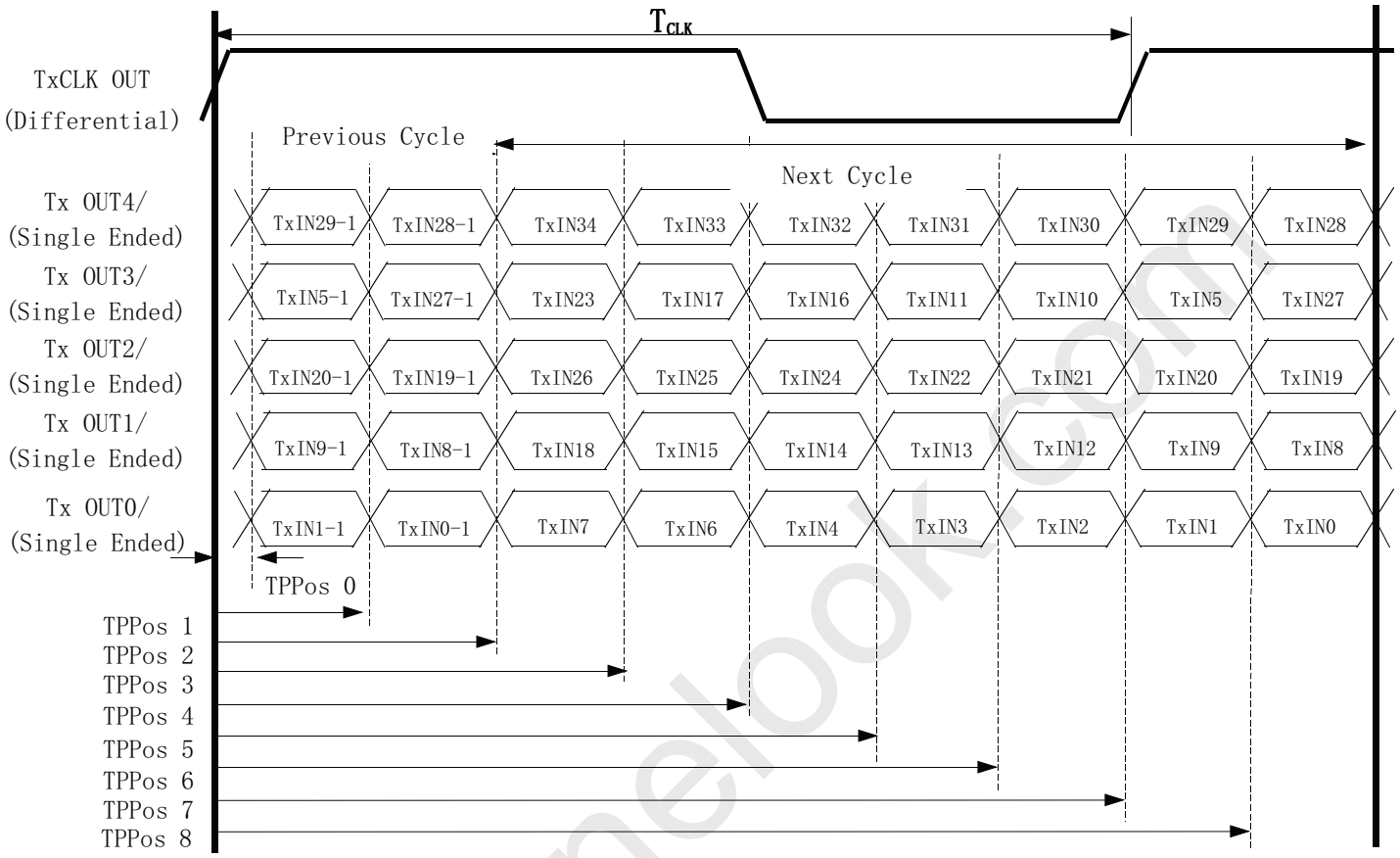


FIGURE 7.Transmitter LVDS OUTPUT PULSE POSITION MEASUREMENT

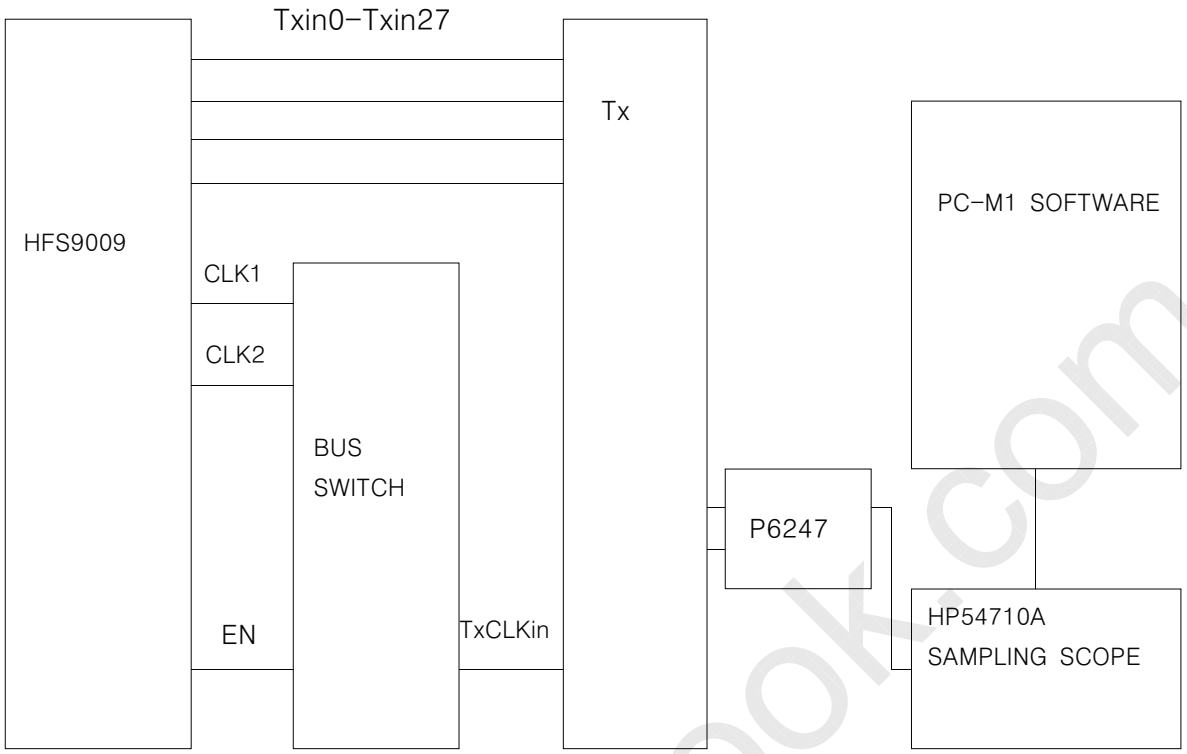


FIGURE 8.TJCC TEST SET-UP -DS90C385 SHOWN

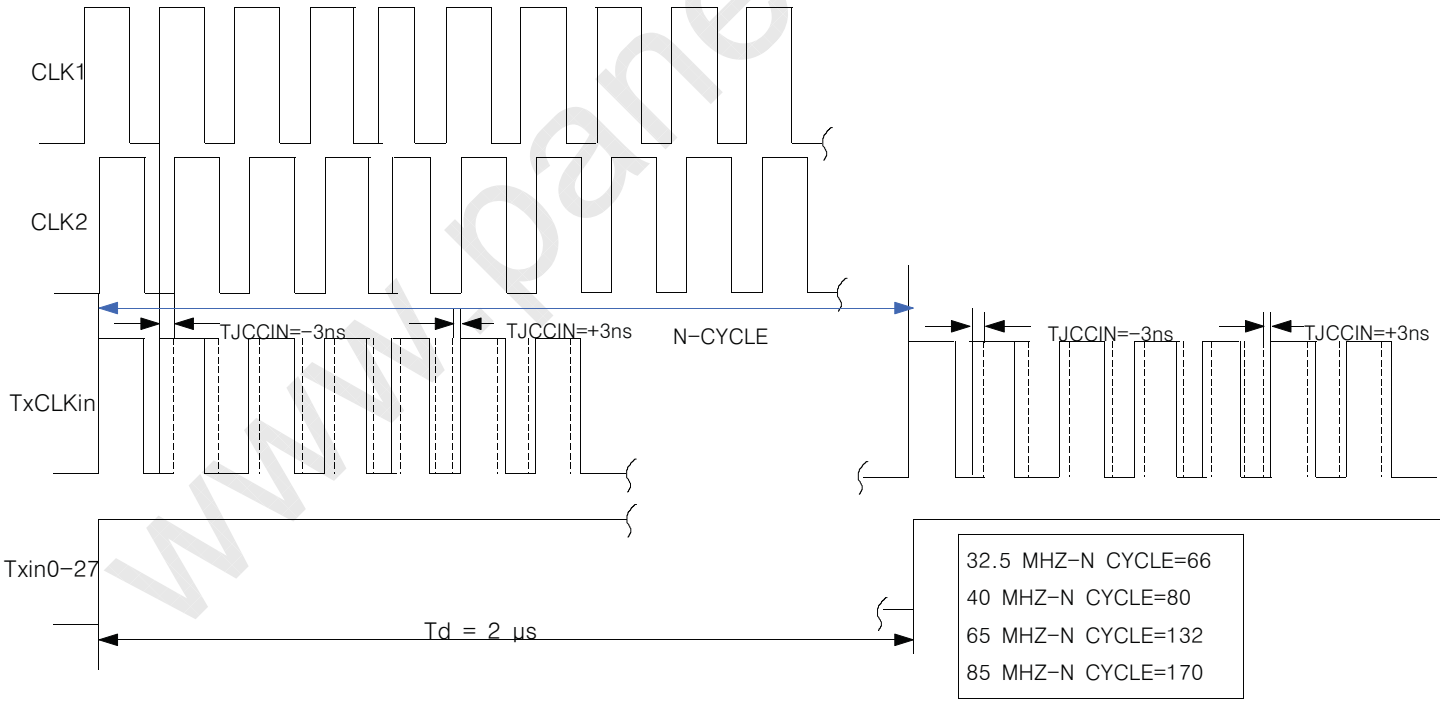


FIGURE 9.TIMING DIAGRAM OF THE INPUT CYCLE TO CYCLE CLOCK JITTER

10.3 LVDS Interface

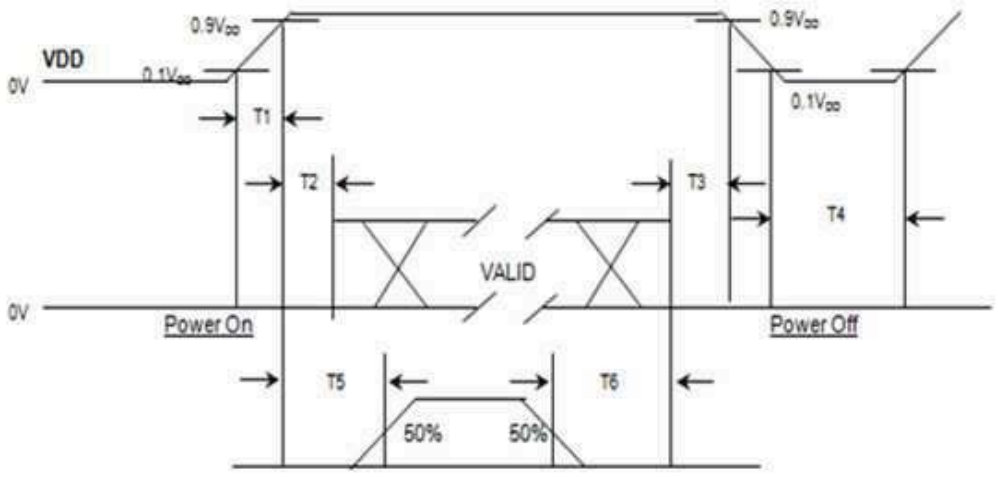
- LVDS Receiver : Tcon 내장형
- JEIDA 규격 채용

	LVDS pin	Odd Data	Even Data
TxOUT/RxIN0	TxIN/RxOUT0	R4	R4
	TxIN/RxOUT1	R5	R5
	TxIN/RxOUT2	R6	R6
	TxIN/RxOUT3	R7	R7
	TxIN/RxOUT4	R8	R8
	TxIN/RxOUT6	R9	R9
	TxIN/RxOUT7	G4	G4
TxOUT/RxIN1	TxIN/RxOUT8	G5	G5
	TxIN/RxOUT9	G6	G6
	TxIN/RxOUT12	G7	G7
	TxIN/RxOUT13	G8	G8
	TxIN/RxOUT14	G9	G9
	TxIN/RxOUT15	B4	B4
	TxIN/RxOUT18	B5	B5
TxOUT/RxIN2	TxIN/RxOUT19	B6	B6
	TxIN/RxOUT20	B7	B7
	TxIN/RxOUT21	B8	B8
	TxIN/RxOUT22	B9	B9
	TxIN/RxOUT24	HSYNC	HSYNC
	TxIN/RxOUT25	VSYNC	VSYNC
	TxIN/RxOUT26	DEN	DEN
TxOUT/RxIN3	TxIN/RxOUT27	R2	R2
	TxIN/RxOUT5	R3	R3
	TxIN/RxOUT10	G2	G2
	TxIN/RxOUT11	G3	G3
	TxIN/RxOUT16	B2	B2
	TxIN/RxOUT17	B3	B3
	TxIN/RxOUT23	RESERVED	RESERVED
TxIn/RxIn4	TxIn/RxOUT28	R0	R0
	TxIn/RxOUT29	R1	R1
	TxIn/RxOUT30	G0	G0
	TxIn/RxOUT31	G1	G1
	TxIn/RxOUT32	B0	B0
	TxIn/RxOUT33	B1	B1
	TxIn/RxOUT34	RESERVED	RESERVED

10.4 전원 온/오프 순서(Power ON/OFF Sequence)

: Latch-up이나 LCD 모듈의 DC operation을 막기위해 전원 온/오프 순서는 아래와 같아야 함.

0.47ms<T1≤10ms
10ms <T2 ≤50ms
0ms<T3 ≤50ms
1000ms ≤T4
350ms ≤T5
60ms ≤T6



T1 : V_{DD} rising time from 10% to 90%
T2 : The time from V_{DD} to valid data at power ON.
T3 : The time from valid data off to V_{DD} off at power Off.
T4 : V_{DD} off time for Windows restart
T5 : The time from valid data to B/L enable at power ON.
T6 : The time from valid data off to B/L disable at power Off.

[Valid Data Condition]
1. Input LVDS signals must satisfy "Interface Timing" Specification on p23.
2. LVDS Clock must keep the same frequency.
3. Data signal should not input during "Fail Safe Mode".

- The supply voltage of the external system for the Module input should be the same as the definition of V_{DD}.
- Apply the LED voltage within the LCD operation range. When the back light turns on before the LCD operation or the LCD turns off before the back light turns off, the display may momentarily show abnormal screen.
- In case of V_{DD} = off level, please keep the level of input signals low or keep a high impedance.
- T3 should be measured after the Module has been fully discharged between power off and on period.
- Interface signal should not be kept at high impedance when the power is on.

11. 신뢰성 수명 시험조건

Item	Test condition	Quantity
Temperature Step Stress	0 ~ 50℃,439Cycle determination	4EA
HTOL	50℃, 1000hr (500hr determination)	8EA
LTOL	0℃, 1000hr (500hr determination)	4EA
HTS	70℃, 1000hr (500hr determination)	4EA
LTS	-30℃,1000hr (500hr determination)	4EA
THB	40℃ / 95%RH,1000hr (500hr determination)	4EA
WHTS	60℃ / 75%RH, 1000hr (500hr determination)	4EA
T/C	-20 ℃ ~ 60 ℃, 200cycle (100cycle determination)	4EA
ESD (non-operation)	±10 kV,200㎊/100 Ω,9Point,3times/Point	3EA
ESD(operation)	Samsung condition : contact : ±8 kV ,150㎊/330Ω,100Point,1 time/Point non-contact : ±15 kV,150㎊/330Ω,100Point,1 time/Point contact : ±8 kV ,200㎊/100Ω,100Point,1 time/Point non-contact : ±15 kV,200㎊/100Ω,100Point,1 time/Point	3EA
POWER ON/OFF	30sec (on) / 30sec(off) : 12,000 times	4EA
Vibration	10~300Hz/1.5G/10minSR, XYZ, 30min/axis	3EA
Shock	SEC condition :11msec, ±XY/axis 40G &±Z 1time/axis 30G	3EA
PALLET Vibration	1.05 Grms, 2~200Hz, Random, Z axis 1Hr	1PALLET
PALLET Drop	20cm, Bottom, Front, Rear 1times	1PALLET

PLI 출하검사 항목 중 단기 잔상에 대하여 고객사(Sony) Spec으로 평가함
변경전 : 12Hr 150G기준(2시간 Mosaic PTN 고정 → gray PTN 판정, 10시간 반복)
변경후 : 2.5Hr Sony기준 50IRE(128Gray) 판정

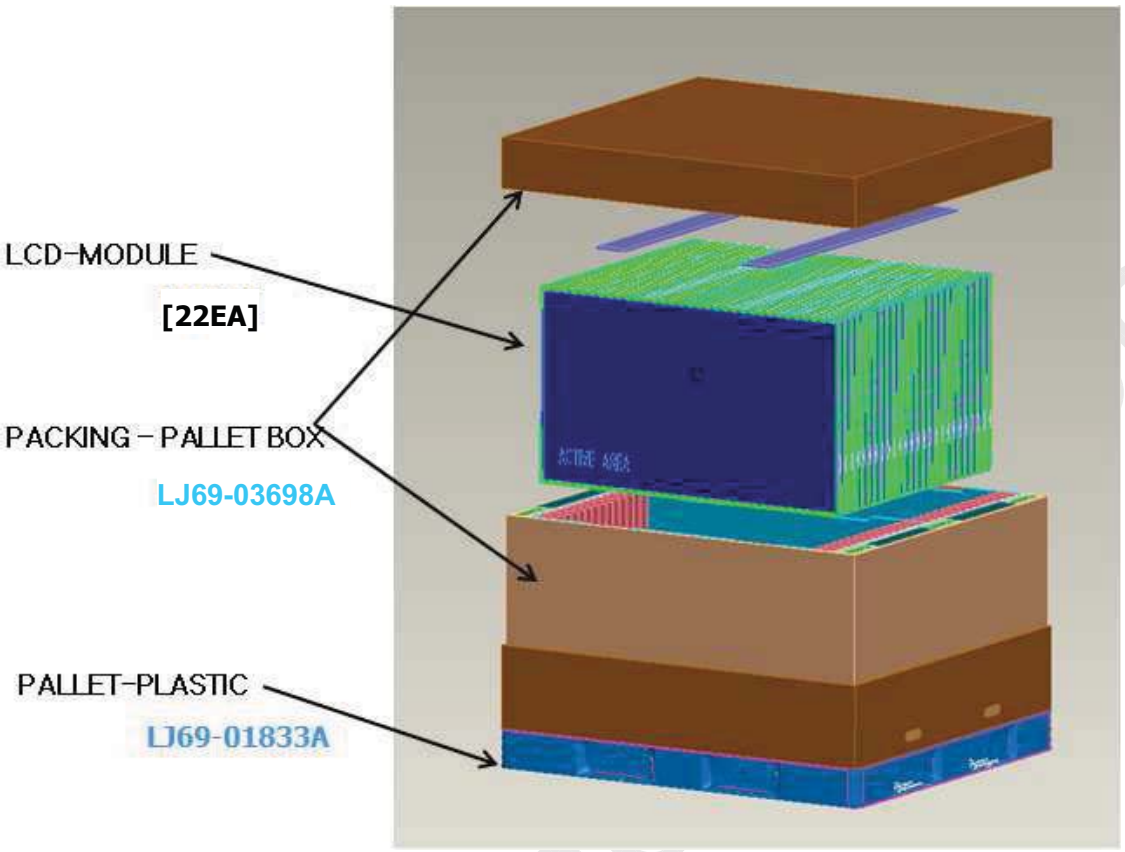
[Result Evaluation Criteria]

Under the display quality test conditions with normal operation state, these shall be no change which may affect practical display function.

HTOL/ LTOL : High/Low Temperature Operating Life,
THB : Temperature Humidity Bias
HTS/LTS : High/Low Temperature Storage
WHTS : Wet High Temperature Storage

12. PACKING

12.1 Packing flow



12.2 Packing Specification

ITEM	Specification	Remark
LCD Packing	22ea / Box (Packing-Pallet Box)	1. 220 Kg / LCD (22ea) 2. 28 Kg / Packing-Pallet Box Material : Paper
Desiccant (Drier)	6EA/LCD	10g/EA, Cobalt-dichloride-free
Pallet-Plastic	1Box / Pallet (W1270,L1150,H125,BLUE)	7.8 Kg / Pallet
Packing Direction	Vertical	
Pallet size	H x V x height	1254mm(H) x 1127mm(V) x 660mm(height)
Pallet weight	257.12kg	Pallet (7.8kg) + Module (220kg) + Packing-Pallet Box (28kg) + Desiccant(0.06kgx22=1.32kg)

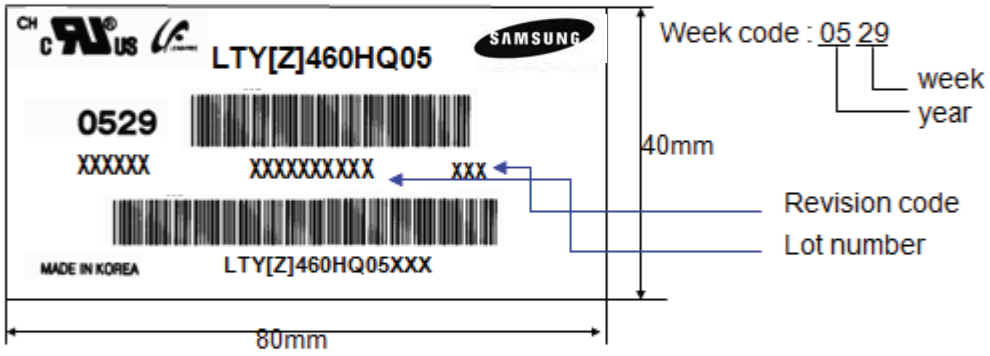
13. MARKING & OTHERS

A nameplate bearing followed by is affixed to a shipped product at the specified location on each product.

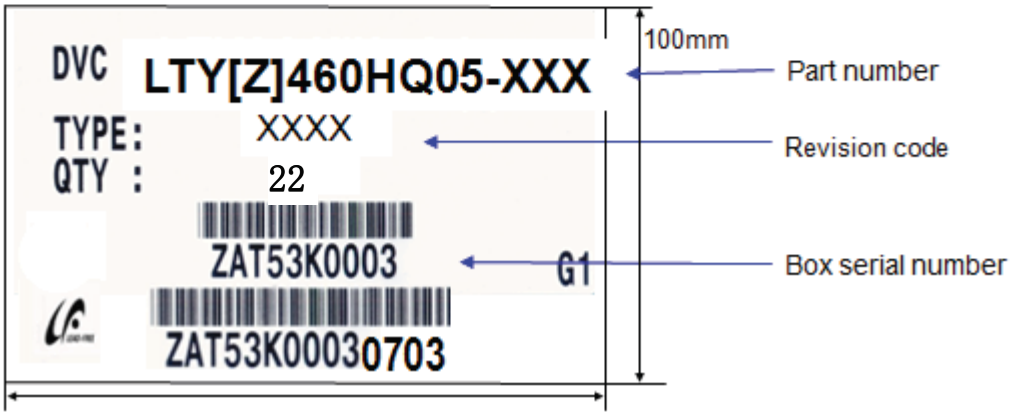
(1) Parts number : LTY[Z]460HQ05-XXX
(2) Revision: One letters
(3) Lot number : X X X X XXX XX X

- Cell Position No. (In the Glass)
- Glass No. (In the one Lot)
- Lot No. (Glass)
- Month
- Year (Note1)
- Product code
- Line

(4) Nameplate Indication



(5) Packing box attach



14. General Precautions

14.1 Handling

(a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.

(b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and CCFT back-light.

(c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.

(d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(f) The desirable cleaners are water, IPA(Isopropyl Alcohol) or Hexane.
Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth . In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(h) Protect the module from static , it may cause damage to the CMOS Gate Array IC.

(i) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(j) Do not disassemble the module.

(k) Do not pull or fold the lamp wire.

(l) Do not adjust the variable resistor which is located on the module.

(m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(n) Pins of I/F connector shall not be touched directly with bare hands.

14.2 Storage

ITEM	Unit	Min.	Max.
Storage Temperature	(℃)	5	40
Storage Humidity	(%rH)	35	75
Storage life	12 months		
Storage Condition	- The storage room should provide good ventilation and temperature control - Products should not be placed on the floor, but on the Pallet away from a wall. - Prevent products from direct sunlight, moisture nor water; Be cautious of a build up of condensation. - Avoid other hazardous environment while storing goods. - If products delivered or kept in conditions of over the storage period of 3 months, the recommended temperature or humidity range, we recommend you leave them at a temperature of 20℃ and a humidity of 50% for 24 hours.		

14.3 Operation

(a) Do not connect,disconnect the module in the "Power On" condition.

(b) Power supply should always be turned on/off by the item 6.3 "Power on/off sequence"

(c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(d) The cable between the back-light connector and its Balance board power supply shall be a minimized length and be connected directly . The longer cable between the back-light and the Balance board may cause lower luminance of lamp(CCFT) and may require higher startup voltage(Vs).

14.4 Others

(a) Ultra-violet ray filter is necessary for outdoor operation.

(b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on) Otherwise the module may be damaged.

(d) If the module displays the same pattern continuously for a long period of time,it can be the situation when the image "Sticks" to the screen.

(e) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

15. 환경 유해물질 관리 기준

15.1 금지물질

아래에 제시하는 물질에 대해서는 부품 및 디바이스 등에 함유되는 일이 있어서는 안된다.

표 15.1 법률에 의해 사용이 금지되어 있는 물질

물질명
Cadmium and cadmium 화합물*1
PBB(plybromobiphenyl)군, PBDE (polybrominated biphenyl ethers)군 *2
Polychlorinated biphenyl (PCB) 류
Polychlorinated naphthalene 류
Organic tin 화합물 (Tributhyl tin category/Triphenyl tin category)
Asbestos
Azo화합물 (용해 후 표 8.3에 나와 있는 Amine을 생성하는 화합물. 이 화합물은 인체와

*1: 포장재료에 대해서는 수은, 카드뮴, 6가 크롬, 납의 중금속 불순물 허용농도가 합계 100ppm 미만이 되도록 한다.

*2: 직접 물질을 금지하는 법은 없으나, 독일의 다이옥신 규제를 따르기 위해 금지 물질로 분류된다.

카드뮴의 경우, 아래에 제시하는 부위에 대한 사용에 대해서는 현재 금지되어 있지 않으나, 향후 규제될 것이므로 적극적으로 전폐를 목표로 한다.

표15.2 규제할 카드뮴 및 기타 화합물의 용도와 전폐 목표

용도	전폐 목표
(a) DC 모터, 스위치, 릴레이, 브레이커 등 신뢰성을 요구하는 모든 기기의 전기 접점 (b) 형광표시장치에 함유되는 형광체 (c) Ni-Cd 전지 (신규로 출시하는 것, 다망 이미 발매 중인	2003년 3월말
(d) 유리 및 유리도료의 안료, 염료	2004년 3월말

아조화합물 중에서 분해에 의해 표16.3에 제시하는 아민이 발생할 용도의 사용을 금지한다.

표15.3 아조화합물의 분해에 의해 발생해서는 안되는 아민 일람

CAS No	아민
92-67-1	4-amonodiphenyl
92-87-5	Benzidine
95-69-2	4-chloro-o-toluidine
91-59-8	2-naphthylamine
97-56-3	o-aminoazotoluene
99-55-8	2-amino-4-nitrotoluene
106-47-8	p-chloroaniline
615-05-4	2,4-diaminoanisole
101-77-9	4,4'-diaminodiphenylmethane
91-94-1	3,3'-dichlorobenzidine
119-90-4	3,3'-dimethoxybenzidine
119-93-7	3,3'-dimethylbenzidine
838-88-0	3,3'dimethyl-4,4'-diaminodiphenylmethane
120-71-8	p-cresidine
101-14-4	4,4'-methylene-bis-(2-chloro aniline)
101-80-4	4,4'-oxideaniline
139-65-1	4,4'-thiodianiline
95-53-4	o-toluidine
95-80-7	2,4-tolluylenediamine
137-7-7	2,4,5-trimenthylaniline
90-04-0	o-anisidine

15.2 완전폐기 물질

다음의 물질은 표 16.5에 표기된 용도를 제외하고 어느 부품이나 장치에 함유되어서는 안 된다.

표 15.4 완전폐기물질

물질명
납 및 납 화합물
수은 및 수은 화합물
6가 크롬 화합물
PVC 및 PVC 혼합물
PBB, PBDE 이외의 유기브롬화합물
염소화 파라핀류 (염소계 난연제/가소제)

아래의 경우에 대해서는 현상황에서 대체기술이 미확립 상태이고, 부품의 기능 및 신뢰성을 확보하는데 있어서 해당부품의 계속사용이 부득이하다고 판단하여 표8.5의 완전폐기 기일까지 완전 폐기하는 것으로 한다.
다만, 대체재료의 기술확립이 가능해진 경우는 기한을 기다리지 않고 사용금지로 한다.
또한 대체기술이 없어 법규제의 규정에 의해 제외 및 예외가 인정된 경우는 기한을 재조정한다.

표 15.5 완전폐기물질에 대한 주요 용도 및 완전폐기 목표

물질명	용도	전폐목표
납 / 그 화합물	사용금지 : 아래 (a),(b),(c),(d),(e),(f),(g),(h),(i),(j),(k),(l),(m) 및 (n) 이외의 용도.	
	(a) 액세서리를 포함한 제품의 외장부 (인체에 쉽게 접촉되는 부위)에의 사용 (플라스틱에 사용되는 안정제, 안료 등) (b) 선재피복에 사용하는 안정제, 안료 등 (c) 액세서리를 포함한 제품의 외장부에 사용하는 각종 합금 및 그 도장면	2003년 3월말
	(e) 부품의 외부전극 · 리드단자 등의 납땜처리 (전기부품/반도체 디바이스/히트싱크 등) (f) 부품 · 디바이스의 내부접속용 납땜, 고융점 납땜 (Pb 85wt% 미만의 주석/납땜) (g) 브라운관 이외의 광학유리에 함유된 납 (h) 납을 함유하는 각종 합금 (i) 도료, 잉크, 저항기의 저항체 (j) 불순물로서 납을 함유하는 각종 합금 다만, 아래 합금은 첨가물로서의 납의 함유가 허용된다. 합금 종류 납 함유 허용농도 강재 0.3wt% 미만 알루미늄합금 0.4wt% 미만 동합금 4wt% 미만	2004년 3월말

15.3 플라스틱 중의 카드뮴 허용 농도

선재피복 등의 플라스틱에 카드뮴 및 그 화합물을 일절 참가해서는 안된다.
측정기의 검출한계, 오차, 자연계에 존재하는 불순물의 혼입을 고려하여 5ppm 미만으로 한다.
이 때의 전처리방법, 측정방법에 대해서는 BS EN 1122 「Plastics - Determination of cadmium - Wet decomposition method에 준한다.
측정은 유도결합 플라즈마 발광 분광 분석법(ICP-AES)을 표준으로 한다.

	(l) 부품·디바이스의 내부접속용 고융점납땜 (Pb 85wt% 이상 함유하는 주석/납땜) (m) 세라믹 압전소자에 함유된 납화합물	예외
수은 / 그 화합물	사용금지 : 아래 (a),(b),(c) 및 (d) 이외의 용도. 예컨데 포장재, 수은전지, 시간계 등	
	(a) 소형형광등 : 1개당 수은함유량이 5mg 이상인 것.	2004년 3월말
	(c) 소형형광등 : 1개당 수은함유량이 5mg 미만인 것.	예외
6가 크롬	사용금지 : 아래 이외의 용도	
	도금, 안료 등의 성분으로 함유되는 것	2004년 3월말
폴리염화비닐 / 그 혼합물	폴리염화비닐을 가지는 모든 부품·디바이스 주요 용도로서 기내배선용 비닐전선, 전원코드, 외부접속코드, 기타 코드류를 가지는 유니트 등. 다만, 안전규격의 규제를 받는 것에 대해서는 소니측이 확인한 후에 계속	2004년 3월말
PBB/PBDE 이외의 유기 취소화합물	프린트배선판, 외광 등 대형부품.	2003년 3월말
	상기 이외의 부위	2004년 3월말

15.4 방출을 규제하는 물질

표15.6 방출을 규제하는 물질

물질명	방출 농도	주요 용도
포름알데히드	대기 중 농도 10㎥ 이상의 기밀시험실에서	모든 목제재료 및

15.5 부품, 디바이스 제조시에 사용해서는 안되는 물질

표15.7 부품, 디바이스 제조시에 사용해서는 안되는 물질

물질명
[오존층을 파괴하는 물질] CFC(chlorofluorocarbon),HCFC(hydrochlorofluorocarbon),methyl bromide,
[Chlorine 유기 용매] 1,1,2-trichloroethane, 1,2-dichloroethane, 1,1-dichloroethlene, 1,2-dichloroethylene,methylene chloride,