SHARP

NEW PRODUCT INFORMATION

LU8500F0/F1

8-bit Single-chip Microcomputer with built-in Flash Memory

■ Description

The LU8500F0/F1 are single chip 8-bit microcomputers, flash memory versions of SM8500 series. LU8500F0 is packaged in 100-pin QFP and LU8500F1 in 100-pin LQFP (0.5 mm pin-pitch).

The LU8500F0/F1's internal flash memory is user programmable: it can be programmed using a PROM writer, through the serial interface (UART) (on-board writing), or by copying data stored in a PROM by using the copy board designed for this purpose.

LU8500F0/F1 are compatible with SM8500 series which contains ROM instead of flash memory. LU8500F0/F1 can be programmed to operate as ROM version. Once the program has been imported into the ROM, the user can run the program without having to verify it.

■ Features

1. CMOS silicon gate process
2. Flash memory capacity 61 440 × 8-bit
3. RAM capacity 2 048 × 8-bit
4. Memory organization
   - It is possible to set the range of accessible address of the internal flash memory in unit of 4k bytes (4 to 60k bytes) by the user program.
5. External memory expansion
   - The LU8500F0/F1 can access external memory by program setting.
6. CPU core
   - 8-bit×8 ports (or 16-bit×4 ports) and 16-bit×4 ports general purpose register are used as accumulator, register pointer, and index register.
   - 68 instructions sets include multiplication, division, and bit manipulation instruction.
   - 23 types of addressing mode.
   - System clock cycle 0.17 μs (MIN.) (When main clock cycle is 12 MHz.)
   - System clock cycle can be varied by program.
   - System clock can be derived from the main clock (divided by 1/2, 1/4, 1/8, 1/16 or 1/32) or sub clock (divided-by-2 32.768 kHz).
7. Oscillator circuit
   - Main clock oscillation circuit (CK_{IN}, CK_{OUT} pins) : 1.5 to 12 MHz
   - Sub clock crystal osicllation circuit (OSC_{IN}, OSC_{OUT} pins) : 32.768 kHz
8. Interrupt
   - Maskable interrupts : 14
     4 external interrupts and 10 internal interrupts from peripheral functions can be set to enable/disable independently and masked by 14-level priority.
   - Non-maskable interrupts : 2
     Watchdog timer interrupt.
     Illegal instruction trap
9. Standby modes
   - HALT Mode
     Changing the mode by HALT instruction.
     The system clock supplied to CPU will be stopped.
   - STOP Mode
     Changing the mode by STOP instruction.
     The main clock will be stopped (sub clock is kept running).

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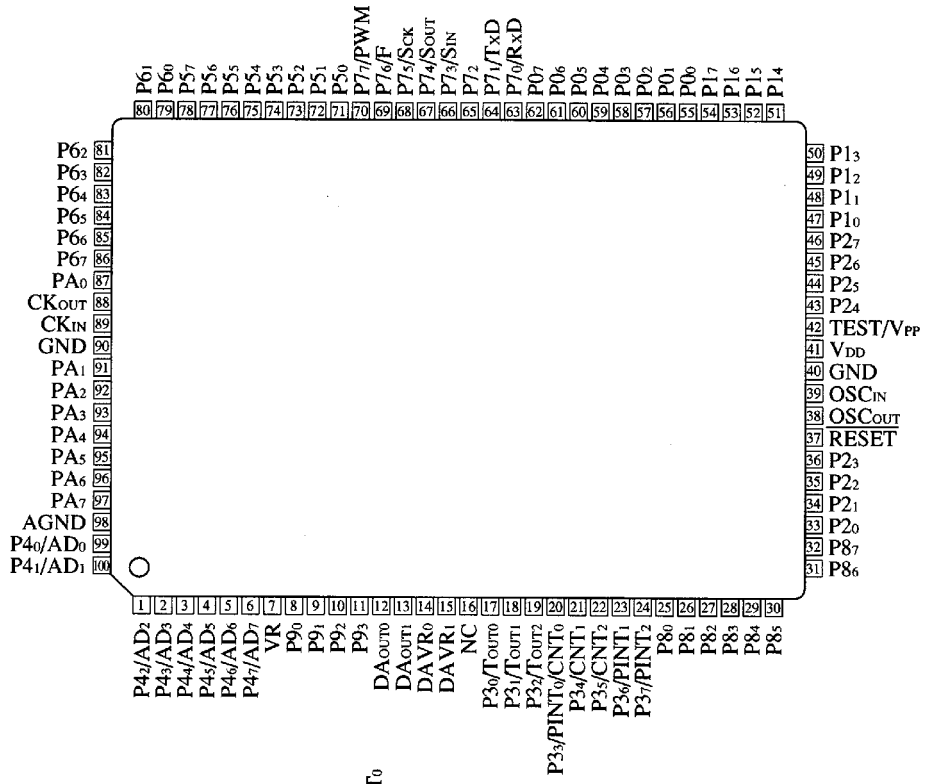
10. I/O ports
    - 2 input ports (each 8 bits) (one port also serves as A/D input)
      The pull-up resistor of one port can be turned on/off by software.
    - 2 output ports (each 8 bits)
      These are large current output pins.
    - 8-bit × 6 I/O ports and 4-bit × 1 I/O port
      The pull-up resistors can be turned on/off by software.
11. Timer/event counter
    - Timer/event counter 16-bit × 1, 8-bit × 5
    - These timers can output PWM (period and duty cycle of 1 channel are variable, duty cycle of 3
    - Watchdog timer 8-bit × 1
    - Clock timer 8-bit × 1
12. Serial interface
    - SIO 8-bit clock sync. × 1
    - UART 8-bit clock async. × 1
13. A/D converter
    - Resolution 10-bit
    - Channel 8 channels
14. D/A converter
    - Resolution 8-bit (4-bit for waveform generator)
    - Channel 2 channels
15. Waveform generator
    - Internal waveform RAM 2 channels
    - User programmable 16 level waveforms
    - Combined with external circuit, DTMF waveform can be output.
16. Clock output
    - $P7_6$/F pin can be used to drive a buzzer (timer 5 output)
17. Operation power and voltage
    - 2.7 to 3.6 V : system clock frequency 3.0 MHz (MAX.)
    - 4.5 to 5.5 V : system clock freuqncy 6.0 MHz (MAX.)
      The LU8500F0/F1 can operate at the max. 12 MHz main clock if the operating voltage is in the range (2.7 to 5.5 V). However, the main clock frequency must be divided to the system clock according to the operating voltage range.
18. Package
    - LU8500F0 100-pin QFP (QFP100-P-1420)
    - LU8500F1 100-pin LQFP (LQFP100-P-1414) (Pin-pitch 0.5 mm)

<Flash memory features >

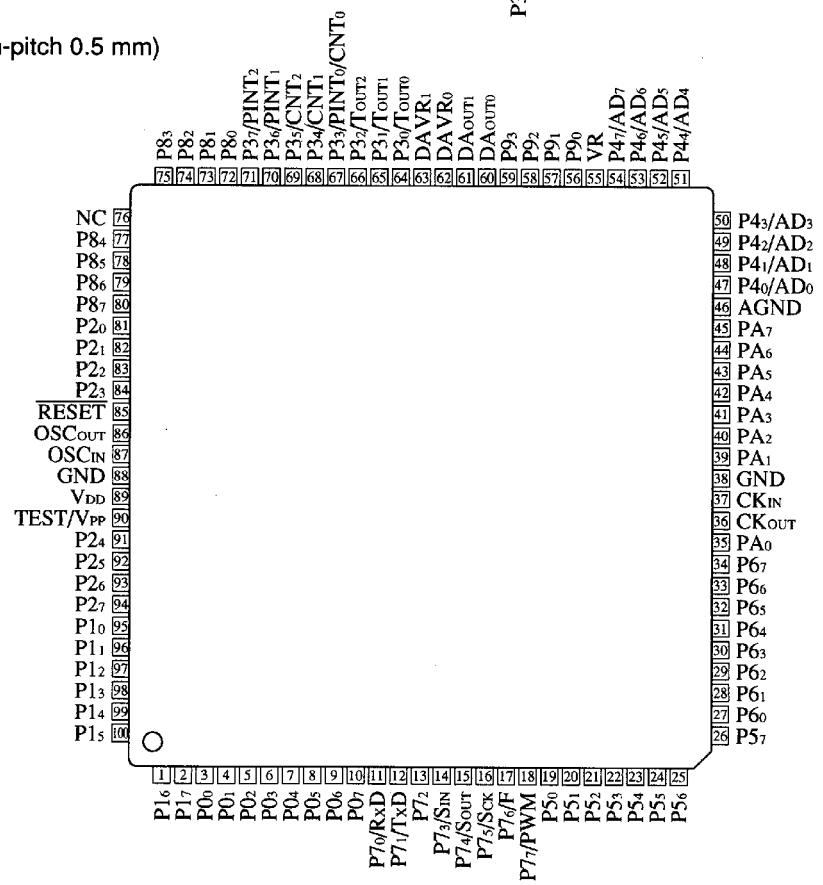
1. Writing method
   - Using instruction : in the same way as used for SHARP 8 M bits flash memory "LH28F008SA"
   - Auto byte write : through the command user interface (CUI)
   - Vpp = 12 V (external)
2. Erasing method
   - Auto block erase by CUI.
3. Block configuration
   - 8 blocks (1 block by 4k bytes, 7 blocks by 8k bytes)
   - Each block can be cleared independently.
4. Reliability
   - Write/erase cycle : 100
5. Three writing modes
   - PROM mode
     Program can be stored/erased by using general purpose PROM writer.
   - Serial mode (on-board mode)
     Data can be read/written/erased from PC.
   - Copy mode
     When the dedicated copy board is used, data stored in PROM can be copied into the internal flash memory.

■ Pin Connections

100-pin QFP



100-pin LQFP (Pin-pitch 0.5 mm)

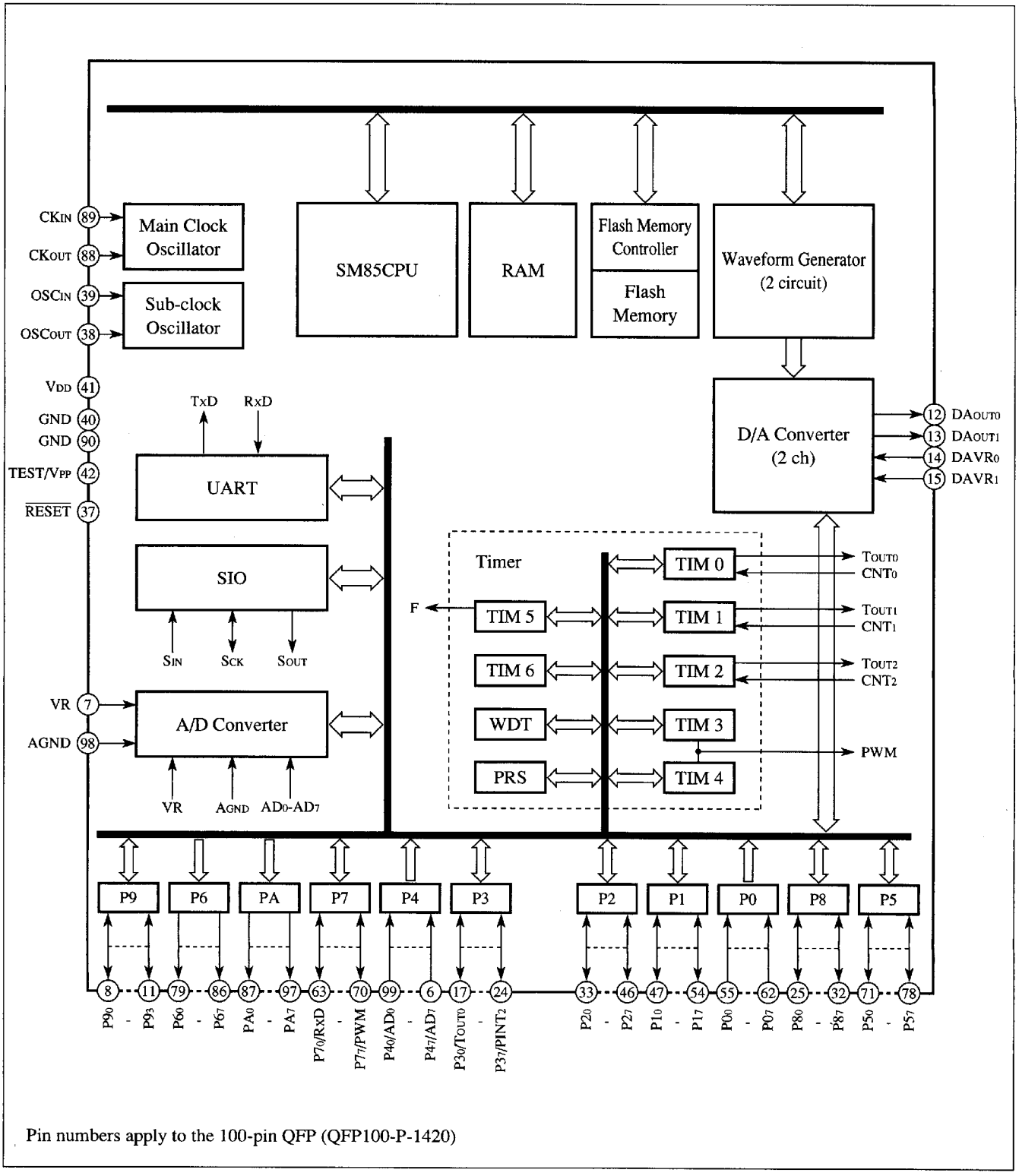


Top View

Pin Description

Pin name	I/O	Function
$P0_0$-$P0_7$	I	Input ports
$P1_0$-$P1_7$	I/O	I/O ports / External memory data I/O ports
$P2_0$-$P2_7$	I/O	I/O ports / External memory address output ports
$P3_0$/T_{OUT0}-$P3_2$/T_{OUT2}	I/O	I/O ports / Timer outputs (T_{OUT0}, T_{OUT1}, T_{OUT2})
$P3_3$/$PINT_0$/CNT_0	I/O	I/O port / External interrupt input / Capture trigger input / Event count input ($PINT_0$/CNT_0)
$P3_4$/CNT_1, $P3_5$/CNT_2	I/O	I/O ports / Event count inputs (CNT_1/CNT_2)
$P3_6$/$PINT_1$, $P3_7$/$PINT_2$	I/O	I/O ports / External interrupt inputs ($PINT_1$/$PINT_2$)
$P4_0$/AD_0-$P4_7$/AD_7	I	Input ports / Analog input ports (AD_0-AD_7)
$P5_0$-$P5_7$	I/O	I/O ports / External memory address output ports
$P6_0$-$P6_7$	O	Output ports (Large current output : 10 mA) (By mask option, the port can be configured as a N-ch open drain pin)
$P7_0$/RxD	I/O	I/O port / UART data input
$P7_1$/TxD	I/O	I/O port / UART data output
$P7_2$	I/O	I/O port
$P7_3$/S_{IN}	I/O	I/O port / SIO data input
$P7_4$/S_{OUT}	I/O	I/O port / SIO data output
$P7_5$/S_{CK}	I/O	I/O port / SIO transfer clock I/O
$P7_6$/F	I/O	I/O port (Buzzer output)
$P7_7$/PWM	I/O	I/O port (PWM output)
$P8_0$-$P8_7$	I/O	I/O ports
$P9_0$-$P9_3$	I/O	I/O ports
PA_0-PA_7	O	Output ports (Large current output : 10 mA) (By mask option, the port can be configured as a N-ch open drain pin)
$DAVR_0$, $DAVR_1$	I	D/A converter reference voltage input ports
$DAout_0$, $DAout_1$	O	D/A converter output ports
VR	I	A/D converter high-level reference voltage input port
AGND	I	A/D converter low-level reference voltage input port
CK_{IN}, CK_{OUT}	I, O	Oscillator pins for main clock (Connecting crystal oscillator)
OSC_{IN}, OSC_{OUT}	I, O	Oscillator pins for subclock (Connecting 32.768 kHz crystal oscillator)
$\overline{RESET}$	I	Hardware reset signal input port
TEST/V_{PP}	I	Test pin (Connect to GND nomally)/writting high voltage pin
V_{DD}, GND	I	Power supply pin, GND pin (Also serving as the D/A ground pin)

Block Diagram



Pin numbers apply to the 100-pin QFP (QFP100-P-1420)

■ Absolute Maximum Ratings

Parameter		Symbol	Condition	Rating	Unit
Supply voltage		V_{DD}		−0.3 to +6.5	V
Write voltage		V_{PP}		−0.2 to +14	V
Input voltage		V_I		−0.3 to V_{DD}+0.3	V
Output voltage		V_O		−0.3 to V_{DD}+0.3	V
Maximum output current	High	I_{OH}	All output pins	4.0	mA
	Low	I_{OL1}	$P6_0$-$P6_7$, PA_0-PA_7	30	mA
		I_{OL2}	All output pin except $P6_0$-$P6_7$, PA_0-PA_7	4.0	mA
Total output current	High	ΣI_{OH}	All output pins	20	mA
	Low	ΣI_{OL1}	$P6_0$-$P6_7$, PA_0-PA_7	100	mA
		ΣI_{OL2}	All output pin except $P6_0$-$P6_7$, PA_0-PA_7	20	mA
Operating temperature		T_{opr}		−20 to +70	℃
Store temperature		T_{stg}		−55 to +125	℃

■ Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit	Note
Supply voltage	V_{DD}	at 3 V mode	2.7 to 3.6	V	
		at 5 V mode	4.5 to 5.5		
System clock cycle	t_{SYS}	V_{DD}=4.5 to 5.5 V	0.17 to 61	μs	
		V_{DD}=2.7 to 3.6 V	0.33 to 61		
Maximum system clock frequency	f_{smax}	V_{DD}=4.5 to 5.5 V	6.0	MHz	
		V_{DD}=2.7 to 3.6 V	3.0		
Maximum main clock frequency	f_{main}	V_{DD}=4.5 to 5.5 V	12.0	MHz	
		V_{DD}=2.7 to 3.6 V	6.0		1
Subclock frequency	f_{sub}	V_{DD}=2.7 to 3.6 V	32.768	kHz	
		V_{DD}=4.5 to 5.5 V			
Operating temperature	t_{opr}		−20 to +70	℃	

Note 1. The system clock is divided-by-2 main clock. When deriving the system clock from a clock source other than divided-by-2 main clock, the main clock can be set to match the systm clock frequency.

■ DC Electrical Characteristics

(V_{DD}=2.7 to 3.6 V, Ta=−20 to +70 ℃)

Parameter		Symbol	Condition	Rating			Unit	Note
				MIN.	TYP.	MAX.		
Input voltage		V_{IH1}		0.8V_{DD}		V_{DD}	V	2
		V_{IL1}		0		0.2V_{DD}		
		V_{IH2}		V_{DD}−0.3		V_{DD}	V	3
		V_{IL2}		0		0.3		
Input current		I_{IH1}	V_{IN}=V_{DD}, V_{DD}=3.0 V			10	μA	4
		I_{IL1}	V_{IN}=0 V, V_{DD}=3.0 V			−10		
		I_{IL2}	V_{IN}=0 V, V_{DD}=3.0 V	−10	−25	−50	μA	5
Output voltage		V_{OH1}	I_{OH}=−0.6 mA, V_{DD}=3.0 V	V_{DD}−0.5			V	6
		V_{OL1}	I_{OL}=6.0 mA, V_{DD}=3.0 V			1.0		
		V_{OH2}	I_{OH}=−0.6 mA, V_{DD}=3.0 V	V_{DD}−0.5			V	7
		V_{OL2}	I_{OL}=0.6 mA, V_{DD}=3.0 V		0			
A/D conversion	Resolution		VR=V_{DD}=3.0 V f_{sys}=3.0 MHz		10		bits	
	Differential linear tolerance				±1.0	±2.5	LSB	
	Linear tolerance				±3.0	±5.0	LSB	
	Combined tolerance				±4.0	±6.0	LSB	
D/A conversion	Resolution		DAVR=V_{DD}=3.0 V		8.0		bits	8
	Output voltage range			0.8		V_{DD}−0.8	kΩ	
	Total tolerance				±0.03	±0.06	V	
Current consumption		I_{DD}	f_{sys}=3.0 MHz		9.0	15	mA	9
		I_{DDH}	f_{sys}=3.0 MHz, HALT mode		1.0	2.0		
		I_{DDS1}	OSC running, STOP mode		20	40	μA	10
		I_{DDS2}	OSC in stop, STOP mode		1.0	6.0	μA	11

Note 2. Applied to pins $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_2$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P7_1$, $P7_2$, $P7_4$, $P7_6$, $P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$, CK_{IN}

Note 3. Applied to pins $\overline{RESET}$, OSC_{IN}, $P0_0$-$P0_7$, $P3_3$-$P3_7$, $P7_0$, $P7_3$, $P7_5$

Note 4. Applied to pins (with pull-up resistors disconnected) $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$

Note 5. Applied to pins $\overline{RESET}$
(with pull-up resistors disconnected) $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$

Note 6. Applied to pins $P6_0$-$P6_7$, PA_0-PA_7

Note 7. Applied to pins $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_3$
$P0_0$ ($\overline{RD}$), $P0_1$ ($\overline{WR}$) (in external memory expansion mode)

Note 8. Applied to pins $DAOUT_0$, $DAOUT_1$

Note 9. Without load V_{DD}=3.0 V, main clock frequency=16 MHz

Note 10. Without load V_{DD}=3.0 V, OSC running (32.768 kHz), VR=GND, constant input signal

Note 11. Without load V_{DD}=3.0 V, OSC_{IN}=GND, VR=GND, constant input signal

(V_{DD}=4.5 to 5.5 V、 Ta=−20 to +70 ℃)

Parameter		Symbol	Condition	Rating			Unit	Note
				MIN.	TYP.	MAX.		
Input voltage		V_{IH1}		0.8V_{DD}		V_{DD}	V	12
		V_{IL1}		0		0.2V_{DD}		
		V_{IH2}		V_{DD}−0.5		V_{DD}	V	13
		V_{IL2}		0		0.5		
Input current		I_{IH1}	V_{IN}=V_{DD}, V_{DD}=5.0 V			−10	μA	14
		I_{IL1}	V_{IN}=0 V, V_{DD}=5.0 V			10		
		I_{IL2}	V_{IN}=0 V, V_{DD}=5.0 V	−40	−75	−150	μA	15
Output voltage		V_{OH1}	I_{OH}=−1.0 mA, V_{DD}=5.0 V	V_{DD}−0.5			V	16
		V_{OL1}	I_{OL}=10 mA, V_{DD}=5.0 V			2.0		
		V_{OH2}	I_{OH}=−1.0 mA, V_{DD}=5.0 V	V_{DD}−0.5			V	17
		V_{OL2}	I_{OL}=1.0 mA, V_{DD}=5.0 V		0			
A/D conversion	Resolution		VR=V_{DD}=5.0 V f_{sys}=6.0 MHz		10		bits	
	Differential linear tolerance				±1.0	±2.5	LSB	
	Linear tolerance				±3.0	±5.0	LSB	
	Combined tolerance				±4.0	±6.0	LSB	
D/A conversion	Resolution		DAVR=V_{DD}=5.0 V		8.0		bits	18
	Output voltage range			0.8		V_{DD}−0.8	kΩ	
	Total tolerance				±0.05	±0.10	V	
Current consumption		I_{DD}	f_{sys}=6.0 MHz		20	30	mA	19
		I_{DDH}	f_{sys}=6.0 MHz, HALTmode		3.0	6.0		
		I_{DDS1}	OSC running STOP mode		30	60	μA	20
		I_{DDS2}	OSC in stop, STOP mode		1.0	10	μA	21

Note 12. Applied to pins P10-P17, P20-P27, P30-P32, P40-P47, P50-P57, P71, P72, P74, P76, P77, P80-P87, P90-P93, CK_{IN}

Note 13. Applied to pins $\overline{RESET}$, OSC_{IN}, P00-P07, P33-P37, P70, P73, P75

Note 14. Applied to pins (with pull-up resistors disconnected) P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P70-P77, P80-P87, P90-P93

Note 15. Applied to pins $\overline{RESET}$
(with pull-up resistors disconnected) P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P87, P90-P93

Note 16. Applied to pins P60-P67, PA0-PA7

Note 17. Applied to pins P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P87, P90-P93
P00 ($\overline{RD}$), P01 ($\overline{WR}$) (in external memory expansion mode)

Note 18. Applied to pins $DAOUT_0$, $DAOUT_1$

Note 19. Without load V_{DD}=5.0 V, main clock frequency=12 MHz

Note 20. Without load V_{DD}=5.0 V, OSC running (32.768 kHz), VR=GND, constant input signal

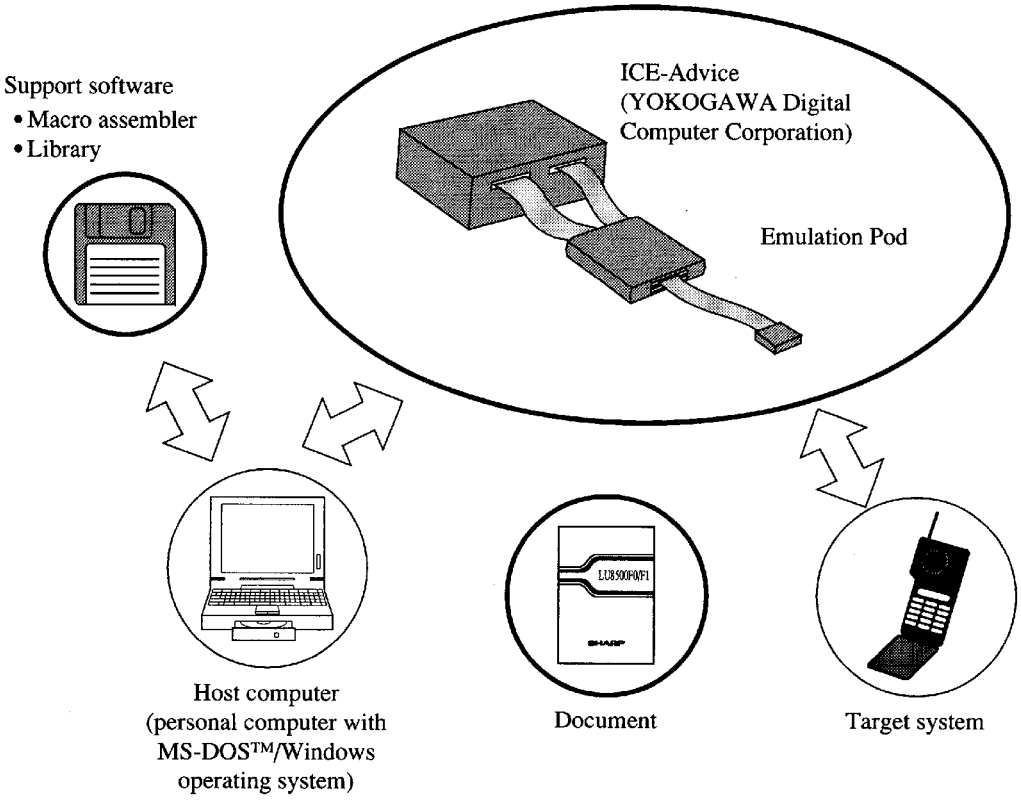
Note 21. Without load V_{DD}=5.0 V, OSC_{IN}=GND, VR=GND, constant input signal

■ LU8500F0/F1 Development Support System

The software program for LU8500F0/F1 can be developed through a system consisting of a personal computer (MS-DOS™)* serving as a host, an in-circuit emulator and many types of development deveices for user's system evaluation.

If a GP-IB interface is used in place of the standard RS-232C interface, programs can be transferred to an emulator at high speed.

* MS-DOS™ is a trademark of Microsoft Corporation.



ICE	Debugger	Support language
YOKOGAWA Digital Computer Corptoration AD200-S56/PP150A	Micro VIEW-G (Windows)	· Assembler (SHARP) · Structured assembler / C compiler (ADaC Corporation)

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- ● Telecommunication equipment (except for trunk lines)
- ● Test and measurement equipment
- ● Industrial control
- ● Audio visual equipment
- ● Consumer electronics

■ Measures such as fail-safe function and redandant desigh should be taken to ensure reliability and safety when SHARP devices are used for or in connection with equipment that requires higher reliability such as :
- ● Main frame computers
- ● Transportation control and safety equipment (i.e. aircraft, trains, automobiles, etc.)
- ● Traffic signals
- ● Gas leakage sensor breakers
- ● Alarm equipment
- ● Various safety devices, etc.

■ SHARP devices shall not be used for or in connection with equipment that requires an extremely high level of reliability and safety such as :
- ● Military and aero space applications
- ● Telecommunication equipment (trunk lines)
- ● Nuclear power control equipment
- ● Medical and other life suport equipment (e.g., scuba)

Contact a SHARP representative in advance when intending to use SHARP devices for any "specific" applications other than those recommended by SHARP or when it is unclear which category mentioned above controls the intended use.

If the SHARP devices listed in this publication fall in the scope of strategic products described in the Foreign Exchange and Foreign Trade Control Law, it is necessary to obtain export permission or approval under the law in order to export such SHARP devices.

Contact and consult with a SHARP representative if there are any questions about the contents of this publication.

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