LUP12N65 / LUF12N65

650V N-Channel Enhancement Mode MOSFET

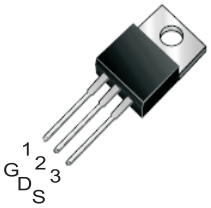
Product General Description

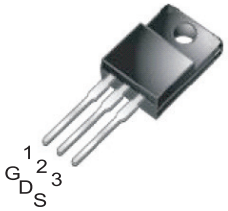
These enhancement mode power filed effect transistors havebeen advanced technology design to provide low on-state resistance, high avalanche energy. These devices are well suited for popular AC-DC applications, active power factor correction, ballasts based on half-bridge topology.

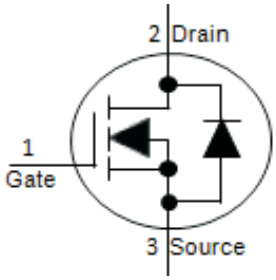
Features

12A , 650V, $R_{DS(ON)}$=0.8Ω@V_{GS}=10V, I_D=6.0A

- Low On-state Resistance
- Fast Switching
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current







Marking and Order Information

TYPE	MARKING	PACKAGE	PACKING
LUP12N65	P12N65	TO-220	50PCS/TUBE
LUF12N65	F12N65	TO-220F	50PCS/TUBE

Absolute Maximum Ratings and Thermal Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	ULP12N65	ULF12N65	Units
Drain-Source Voltage	V_{DS}	650		V
Gate-Source Voltage	V_{GS}	±30		V
Continuous Drain Current	I_D	12	12	A
Pulsed Drain Current [1)]	I_{DM}	48	48	A
Avalanche Energy with Single Pulse I_{AS}=12A, VDD=90V, L=12mH	E_{AS}	990		mJ
Maximum Power Dissipation T_c=25°C Derating Factor	P_D	175 1.4	52 0.42	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 to +150		°C
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	0.7	2.4	°C/W
Junction-to Ambient Thermal Resistance	$R_{\theta JA}$	62.5	100	°C/W

Note : 1. Maximum DC current limited by the package

IMPROVE PRODUCT DESIGN,FUNCTIONS AND RELIABILITY WITHOUT NOTICE

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Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	650	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	2.0	-	4.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}= 10V, I_D= 6.0A	-	0.66	0.8	Ω
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	-	-	10	uA
Gate Body Leakage	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA
Dynamic						
Total Gate Charge	Q_g	V_{DS}=520V, I_D=12A, V_{GS}=10V	-	46.8	62	nC
Gate-Source Charge	Q_{gs}		-	9.2	-	
Gate-Drain Charge	Q_{gd}		-	14.6	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=325V, I_D=12A V_{GS}=10V, R_G=25Ω	-	16.2	24	ns
Turn-On Rise Time	t_r		-	26.8	42	
Turn-Off Delay Time	$t_{d(off)}$		-	56	98	
Turn-Off Fall Time	t_f		-	24.6	38	
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V f=1.0MH$_Z$	-	1800	2450	pF
Output Capacitance	C_{oss}		-	145	195	
Reverse Transfer Capacitance	C_{rss}		-	16	22	
Source-Drain Diode						
Max. Diode Forward Current	I_S	-	-	-	12	A
Max.Pulsed Source Current	I_{SM}	-	-	-	48	A
Diode Forward Voltage	V_{SD}	I_S=12A , V_{GS}=0V	-	-	1.4	V
Reverse Recovery Time	t_{rr}	V_{GS}=0V, I_F=12A di/dt=100A/us	-	450	-	ns
Reverse Recovery Charge	Q_{rr}		-	5.0	-	uC

NOTE : Plus Test : Pluse Width ≤ 300us, Duty Cycle ≤ 2%.

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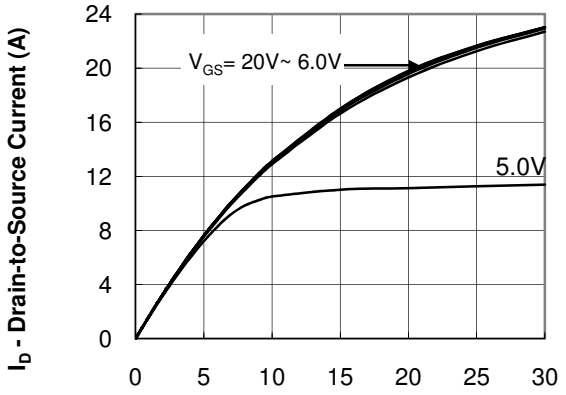
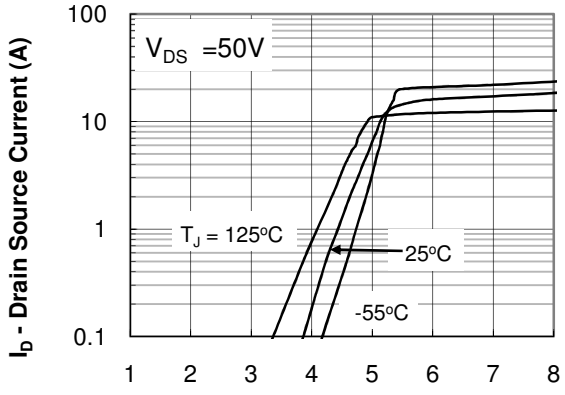
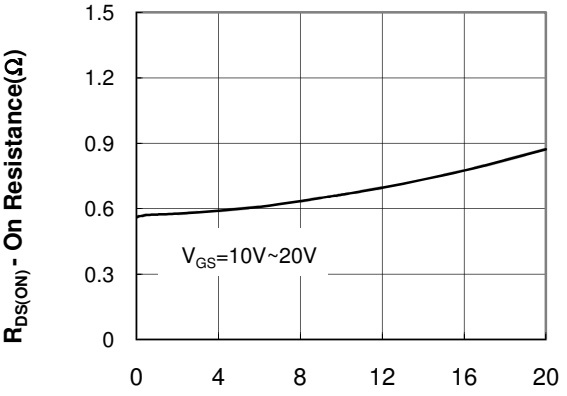
Typical Characteristics Curves (T_C=25℃, unless otherwise noted)



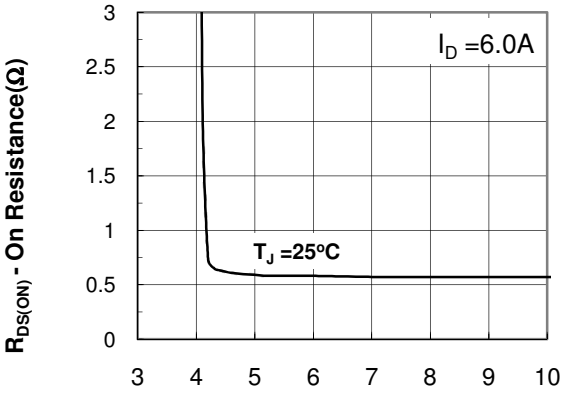
Output Characteristic



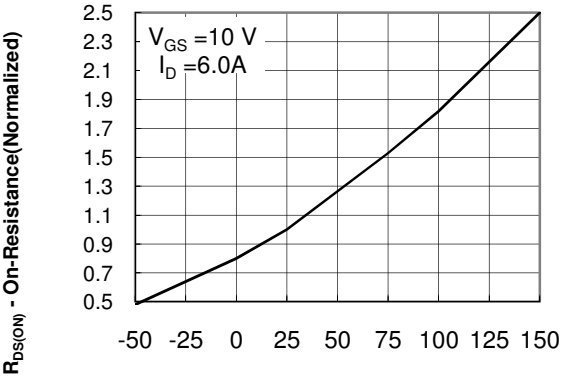
Transfer Characteristic



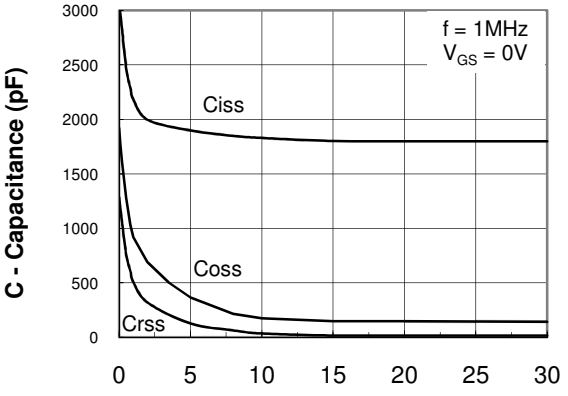
On Resistance vs Drain Current



On Resistance vs Gate to Source Voltage



On Resistance vs Junction Temperature



Capacitance

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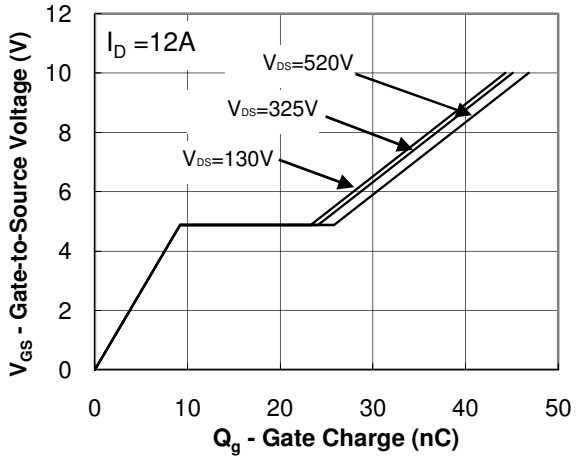
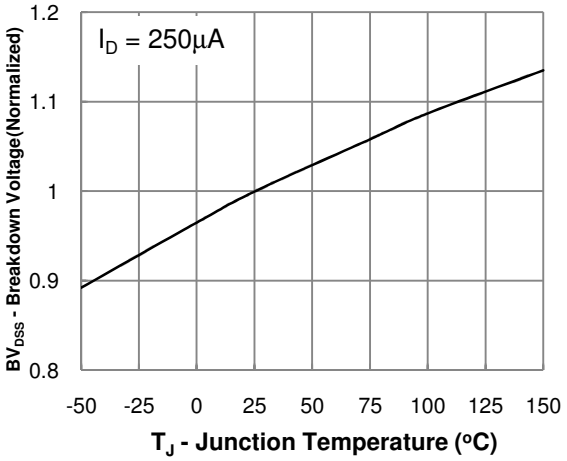
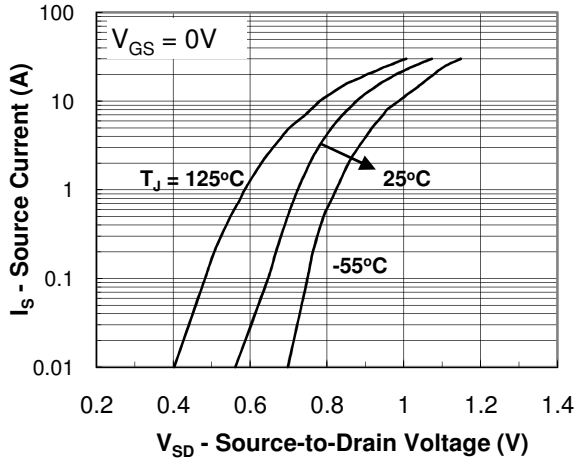
Typical Characteristics Curves (T_C=25℃, unless otherwise noted)



Gate Charge Waveform



Breakdown Voltage vs Junction Temperature



Source-Drain Diode Forward Voltage