

# SANYO Semiconductors DATA SHEET



# **FM Transmitter IC with Stereo Modulation**

#### **Overview**

The LV2283VB is an FM Transmitter IC. MPX block makes stereo modulated, composite signal from L and R sound inputs. RF VCO includes FM modulation function. PLL synthesizer determines RF output frequency with I<sup>2</sup>C control.

## Application

- Portable Memory Player
- Portable HDD Player
- Wireless Headphone

#### Features

- (Audio) Pilot tone system stereo modulation, audio attenuation
- (RF) VCO, programmable gain driver amplifier
- (PLL) 70 to 110MHz 100kHz step
- (Bus control) I<sup>2</sup>C bus control
- (Regulator) 2.8V LDO regulator

# **Specifications**

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max	Pin 6	7.0	V
Maximum input voltage	V <sub>IN</sub> max		V <sub>CC</sub> +0.3	V
Minimum input voltage	V <sub>IN</sub> min		-0.3	V
Allowable power dissipation	Pd max	Ta $\leq$ 85°C, Mounted on a specified board*	500	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

\* Specified board : 114.3mm×76.1mm×1.6mm, glass epoxy circuit board.

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# LV2283VB

#### **Recommended Operating Conditions** at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V <sub>CC</sub>	Pin 6	3.3	V
Operating supply voltage range	V <sub>CC</sub> op	Pin 6	2.8 to 5.5	V

## AC Characteristics Ta = 25°C, V<sub>CC</sub> = 3.3V, I<sup>2</sup>C bits = Default state, L and R input = 1kHz, 450mVrms,

unless otherwise noted

Decemeter	Symbol	Conditions		Unit			
Parameter	Symbol	Conditions	min	typ	max	Unit	
Circuit current	ICC	No input signal, Pin 6 current		8	10	mA	
Standby current ISTB		No input signal, I <sup>2</sup> C bit "STB" = "1",			1.0	μA	
		Pin 6 current					

#### Audio and MPX Blocks

Devenuetor	Questi al Questi times			11.5		
Parameter	Symbol	Conditions	min	typ	max	Unit
Maximum audio input	VA max	Pin 1 and 24 input 900				mVrms
Audio input frequency	FAF	Pin 1 and 24 input         20         15k		Hz		
Channel separation	SEP	Pin 7, composite output, L $\rightarrow$ R, R $\rightarrow$ L	20	35		dB
Channel balance CB		Pin 7, composite output	-2	0	2	dB
Total harmonic distortion	THD	Pin 7, composite output		0.1	0.3	%
Pilot tone output level	PMOD	I <sup>2</sup> C bits "ST" ="1"	0.5	0.85	1.2	mVp-p
Composite output level	MPXOUT		3.3	3.8	4.3	mVrms
Audio mute	MUTE	I <sup>2</sup> C bit "MUTE" = "1"	30	35		dB
Audio attenuation adjustment step ATTSTEP		I <sup>2</sup> C bit "ATT2 – ATT0" = "000" to "111",	1.5	2	2.5	dB
	EX000 (4)	totally 8 steps.		70		
Crystal oscillator frequency (1)	FXOSC (1)	Pin 21 and Pin 22		76		kHz

#### **RF Blocks**

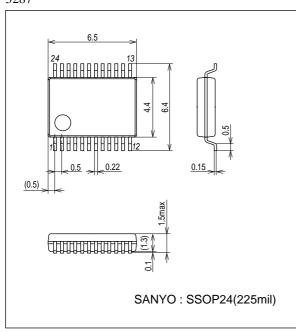
Parameter	Questi al Constitues			11-2		
Parameter	Symbol	Conditions	min	typ	max	Unit
RF output RFOUT f = 98MHz, I <sup>2</sup> C		f = 98MHz, I <sup>2</sup> C bit "RF2 - RF0" = "011",	109	112	115	dBμV
		Pin 12 output				
RF output adjustment step	RFSTEP	$I^{2}C$ bit "RF2 - RF0" = "000" to "111",	0.4	0.9	1.4	dB
		totally 8 steps. Pin 12 relative output.				
RF frequency	FRF	100kHz step	70		110	MHz

#### PLL Blocks

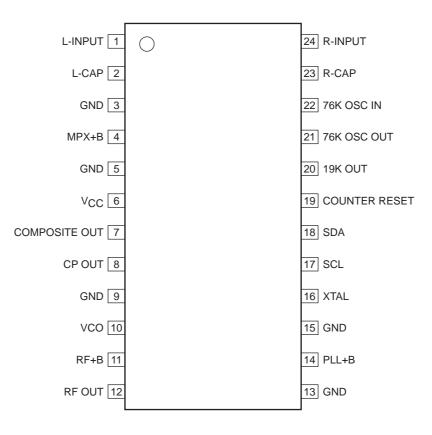
Deremeter	Symbol Conditions			Unit		
Parameter	Symbol	Conditions	min	typ	max	Unit
I <sup>2</sup> C input "High" voltage	VH		0.8V <sub>CC</sub>		V <sub>CC</sub> +0.3	V
I <sup>2</sup> C input "Low" voltage	VL		-0.3		0.2V <sub>CC</sub>	V
19kHz output voltage	V19K	Pin 20. 19kHz output. I <sup>2</sup> C bit "19K" = "1". Load impedance = $47k\Omega$ .	0.6V <sub>CC</sub>	0.8V <sub>CC</sub>		Vp-р
RF input frequency	FPLL	Step = 100kHz, See table 1	70		110	MHz
Crystal oscillator frequency (2)	FXOSC (2)	Pin 16		16		MHz
External clock frequency	FEXT	External clock injection to Pin 13 instead of 16MHz crystal oscillation. When the LSI is standby mode, external clock should be stop.	1		24	MHz
CP output current	ICP	CP voltage = 1.4V		30		μA

# Package Dimensions

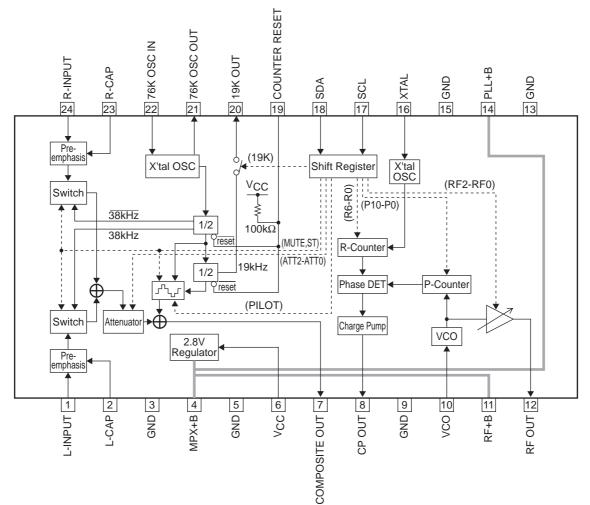
unit : mm (typ) 3287



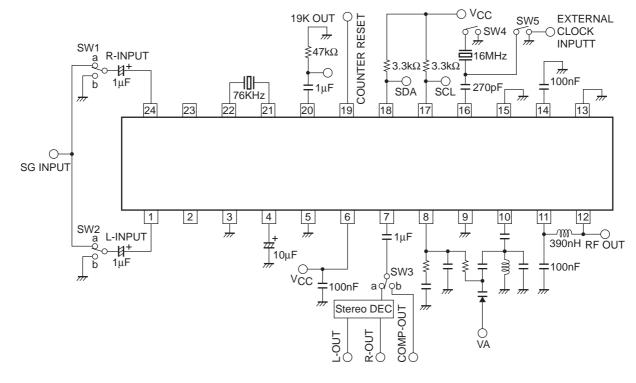
# **Pin Assignment**



# **Block Diagram**



# **AC Testing Circuit**



Pin Nac     Pin Name     DC Voltage (N)     Description     Equivalent Circuit       1     L-INPUT     0     Left channel input. If audio source DC voltage is not 0V, AC coupling capacitance is required. Pre-emphasis capacitance should be required between pin 1 (24) and 2 (23).     0     6       2     L-CAP     0     See Pin 1     0     1000000000000000000000000000000000000
1       L-INPUT       0       Left channel input. If audio source DC voltage is not 0V. AC coupling capacitance is not 0V. AC coupling capacitance should be required between pin 1 (24) and 2 (23).         2       L-CAP       0       See Pin 1         3       GND       0         4       MPX+B       2.8       LDO regulator output for audio frequency and MPX blocks. External decoupling capacitance is required.         5       GND       0         6       VCC       3.3         7       COMPOSITE       0.05         0.05       Stereo modulated output.       6
3       GND       0         4       MPX+B       2.8       LDO regulator output for audio frequency and MPX blocks. External decoupling capacitance is required.       6         5       GND       0       6         6       V <sub>CC</sub> 3.3       3         7       COMPOSITE OUT       0.05       Stereo modulated output.       6         4       Image: Composition of the stere of the s
4       MPX+B       2.8       LDO regulator output for audio frequency and MPX blocks. External decoupling capacitance is required.         5       GND       0         6       V <sub>CC</sub> 3.3         7       COMPOSITE OUT       0.05         0UT       Stereo modulated output.       6         4       4       4         12kΩ ≸       12kΩ ≸
and MPX blocks. External decoupling capacitance is required.       b     and MPX blocks. External decoupling capacitance is required.       and MPX blocks. External decoupling capacitance is required.       and MPX blocks. External decoupling capacitance is required.       b     and MPX blocks. External decoupling capacitance is required.       and MPX blocks. External decoupling capacitance is required.       b     and MPX blocks. External decoupling capacitance is required.       and MPX blocks. External decoupling capacitance is required.       b     and matching capacitance is required.       b     and matching capacitance is required.       b     and matching capacitance is required.       c     and matching capacitance is require
6     V <sub>CC</sub> 3.3       7     COMPOSITE OUT     0.05     Stereo modulated output.
7     COMPOSITE OUT     0.05     Stereo modulated output.       6     4       12kΩ ≢       7     2kΩ ≢
OUT $6$
8       CP OUT       -       Charge pump current output.         6       11       30μA         9       9

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Pin No.	Pin Name	DC Voltage (V)	Description	Equivalent Circuit
10	vco	2.2	Transistor BASE terminal for Colpitz oscillator.	
11	RF+B	2.8	LDO regulator output for RF blocks.	
12	RF OUT	2.8	Collector output. Inductance should be connected Between pin 11 and pin 12 for getting resonant frequency and making pin12 DC bias 2.8V.	$ \begin{array}{c} 6\\ 11\\ 12\\ 12\\ 13\\ 13\\ 13\\ 13\\ 13\\ 13\\ 13\\ 13\\ 13\\ 13$
13	GND	0		
14	PLL+B	2.8	LDO regulator output for digital blocks.	
15	GND	0		
	55	,		

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# LV2283VB

Continued	from preceding pag			
Pin No.	Pin Name	DC Voltage (V)	Description	Equivalent Circuit
16	XTAL	2.0	16MHz crystal is needed for PLL reference frequency. If external clock is injected to Pin 16, frequency should be from 1MHz to 24MHz and N (integer) × 200kHz. When the IC is Standby mode, external clock should be stop.	
17	SCL	-	I <sup>2</sup> C clock input.	$\begin{array}{c} 6 \\ \hline \\ 17 \\ \hline \\ 15 \end{array} \longrightarrow CMOS \ Logic \ Input \\ \hline \\ 15 \end{array}$
18	SDA	-	I <sup>2</sup> C data input.	$\begin{array}{c} 6 \\ \hline \\ 18 \\ \hline \\ 15 \end{array}  W  CMOS \ Logic \ Input \\ \hline \\ 15 \end{array}$
19	COUNTER RESET	3.3	Usually pin 19 should be kept "Logic High" or opened (pull up 100kΩ makes pin 19 "Logic High" automatically). When pin 19 is "Logic Low" level, internal frequency counter from 76kHz to 19kHz is reset.	$ \begin{array}{c} 6 \\ 18 \\ 19 \\ 18 \\ CMOS Logic Input \\ 15 \\ 15 \\ 15 \\ 15 \\ 100 k\Omega \\ CMOS Logic Input \\ 15 \\ 15 \\ 100 k\Omega $
20	19K OUT	-	19kHz output (same phase as pilot tone). When I2C bit "19K"=0, Pin 20 is kept "Logic Low" level.	6 20 CMOS Logic Output (15
21	76K OSC OUT	2.0	For stereo modulator pilot signal and sub carrier. 76kHz crystal should be connected between Pin 21 and Pin 22	6 14 21 $1k\Omega$ $1k\Omega$ $1k\Omega$ $1k\Omega$ 1 1 1 1 1 1 1 1 1 1

Continued	Continued from preceding page.								
Pin No.	Pin Name	DC Voltage (V)	Description	Equivalent Circuit					
22	76K OSC IN	0.7	See Pin 21	See Pin 21					
23	R-CAP	0	See Pin 1	See Pin 21					
24	R-INPUT	0	See Pin 1	See Pin 21					

# I<sup>2</sup>C Bus Definition

#### Table 1. I<sup>2</sup>C Bus Write Data Format

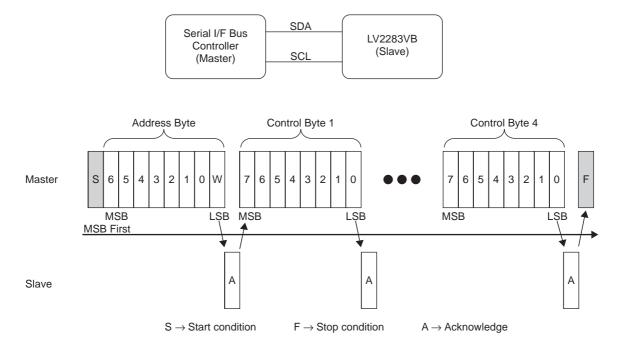
News	D. (	Bit						1011		
Name	Byte	MSB (1)							LSB	ACK
Address Byte	1	AD7	AD6	AD5	AD4	AD3	AD2	AD1	R/W	
		1	1	0	1	0	0	0	0	A
Control Byte 1	2	P10	P9	P8	P7	P6	P5	P4	P3	
		0	1	1	1	1	0	1	0	A
Control Byte 2	3	P2	P1	P0	19K	ST	PILOT	STB	MUTE	
		1	0	0	0	1	1	0	0	A
Control Byte 3	4	RES1	RES0	RF2	RF1	RF0	ATT2	ATT1	ATT0	
		0	0	1	1	1	0	1	1	A
Control Byte 4	5	R6	R5	R4	R3	R2	R1	R0	TEST	
		1	0	1	0	0	0	0	0	A

(1) : MSB is transmitted first.

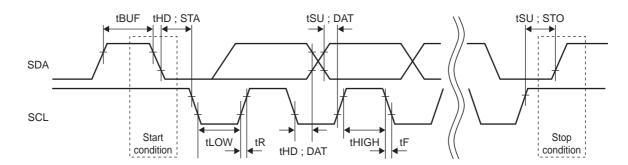
#### Table 2. I<sup>2</sup>C Write Mode Description

Bit	Name	Description
AD7 – AD1	Address bit	LV2283VB requires address bits.
R/W	Read/Write	"0" for Write mode (Write mode only).
A	Acknowledge	
P10 – P0	Programmable counter	11 bit Programmable counter. P0 = LSB, P10 = MSB.
		RF Frequency = (P10x2 <sup>10</sup> + P9x2 <sup>9</sup> + P1x2 <sup>1</sup> + P0) x 100kHz
		Default state = "01111010100" (980)
19K	19kHz output	19K OUT (Pin 20) ON / OFF. "19K" = "0" for no output. "1" for 19kHz output (same phase as pilot tone).
		Default state = "0"
ST	MONO/ST selection	Monaural/Stereo transmission mode selection. "ST" is set "0" for monaural mode (no pilot tone), "1" for
		stereo transmission. Default state = "1"
PILOT	Pilot tone output	"1" for normal operation (default). "0" for NO pilot tone in composite output even if ST bit = "1" (Stereo
		mode).
STB	Standby	"1" for standby mode. Default state = "0" for normal operation.
MUTE	Audio mute	"1" for Audio mute. Default state = "0" for normal operation.
RES1, RES0	Reserved bits	Reserved bits. Default state = "00" for normal operation.
RF2 – RF0	RF output adjustment	RF output voltage adjustment with 8 degree, 1dB steps. "RF2, RF1, RF0" = "111" for maximum. "000" is
		minimum RF output. Default state = "111"
ATT2 – ATT0	Audio attenuator	Audio attenuator for FM modulation fine adjustment is set by "ATT2, ATT1, ATT0" with 8 degree,
		2dB steps. "111" is for 0dB attenuation. "000" is for 14dB attenuation. Default state = "011".
R6 – R0	Reference counter	7 bit Programmable counter. R0 = LSB, R6 = MSB.
		Reference frequency should be set 100kHz.
		{Crystal oscillator frequency (Pin 16)} / {(R6x $2^{6}$ + R5x $2^{5}$ + R1x $2^{1}$ + R0) x 2} = 100kHz.
		Default state = "1010000" (80 × 2).
TEST	Test mode	For IC testing. Set "0" for normal operation.
		"1" for counter testing mode. Default state = "0"

# I<sup>2</sup>C Bus Operation



**Time chart** 



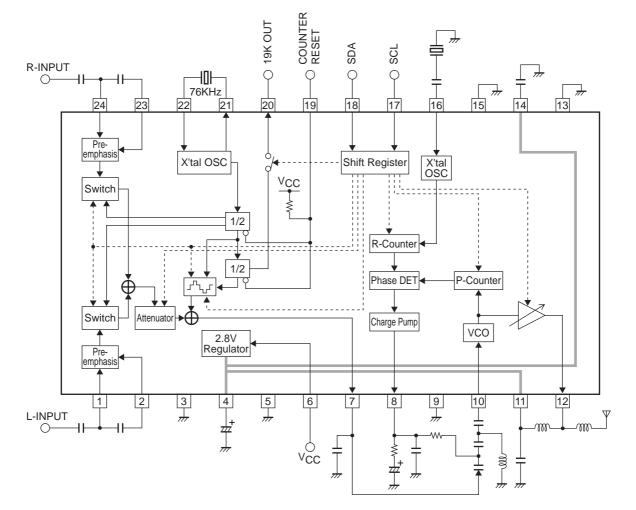
#### Table 3. Timing specification

Parameter	Symbol	Ratings			Linit
		min	typ	max	Unit
SCL clock frequency	fSCL			100	kHz
Bus free time between a STOP and START condition	tBUF	4.7			μs
Hold time START condition	tHD ; STA	4.0			μs
LOW period of the SCL clock	tLOW	4.7			μs
HIGH period of the SCL clock	tHIGH	4.0			μs
Data hold time	tHD ; DAT	0.0			μs
Data set-up time	tSU ; DAT	250			ns
Rise time of both SDA and SCL signals	tR			1000	ns
Fall time of both SDA and SCL signals	tF			300	ns
Set-up time for STOP condition	tSU ; STO	4.0			μs

I<sup>2</sup>C Bus AC Characteristics : Temp=25°C V<sub>CC</sub> = 3.3V

Note : I<sup>2</sup>C Bus is a registered trademark of the Philips Co..

# **Application Circuit**



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