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LV23401V

Bi-CMOS IC

1-chip Tuner IC with built-in FLL for Home Stereo System

Overview

The LV23401V is a AM/FM one-chip tuner IC for home stereo system.

Functions

- AM tuner
- FM tuner
- MPX stereo decoder
- FLL tuning system

Features

- All the adjustment work of external parts is unnecessary.
- CCB control with easy command base
- External parts are reduced by LOW-IF frequency (FM=225kHz, AM=53kHz) adoption.
- The high sensitivity reception is achieved in low noise MIX input circuit.
- All bands of Japan-U.S.-Euro can be received by the soft program change (76MHz to 108MHz).
- With built-in FLL(Frequency Locked Loop) tune function
- Soft mute and stereo blend function (seven stages programmed control possible)
- With built-in adjacent channel obstruction removal function
- With built-in stereo pilot cancellation function
- For EN55020-S1 standard (European immunity)
- With built-in power save function

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Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max	Analog block supply voltage	10.0	V
Maximum output voltage	V _O max	Digital block supply voltage	4.5	V
Maximum input voltage	V _{IN1} max	CE, DI, CL	*1) Vref2+0.35	V
	V _{IN2} max	CLK IN	4.5	V
Allowable power dissipation	Pd max	Ta ≤ 70 °C *2)	450	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

*1) Vref2 = 22 pin voltage

*2) When mounted on the specified printed circuit board (114.3mm × 76.1mm × 1.6mm), glass epoxy

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Operating Condition at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}	Analog block supply voltage	9.0	V
Operating supply voltage range	V _{CC} op	Resister 1Eh Bit 1(LEVSHIF)=0	4.5 to 6.5	V
		Resister 1Eh Bit 1(LEVSHIF)=1	8.5 to 9.5	V

* Stabilize the service voltage so as not to cause the voltage charge by the noise etc.

Interface block allowable operation range at Ta = -20 to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input "H" level voltage	V _I H1	CE, DI, CL	2.3		3.435	V
	V _I H2	CLK IN	2.3		3.435	V
Input "L" level voltage	V _I L1	CE, DI, CL	0		0.5	V
	V _I L2	CLK IN	0		0.3	V
Output voltage	V _O	D0	0		4.0	V
Crystal frequency	f _{IN}	CLK IN		32.768		kHz
Crystal frequency deflection	f devi1	For the standard European immunity	-50		+50	ppm
	f devi2	When standard non-corresponds European immunity	-150		+150	ppm
Crystal vibrator load capacity	CL	*	4	12.5		pF

* The evaluation request to the crystal maker is recommended because it changes by the substrate and the circuit constant used.

Operating Characteristics at Ta = 25°C, V_{CC} = 9.0V with the designated circuit.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain (at no input)	I _{CC} FM	No input in FM mode. 15 pin supply current.	25	35	45	mA
	I _{CC} AM	No input in AM mode. 15 pin supply current.	14	24	34	mA
Power save current drain	I standby	15 pin supply current power save : Register 1Fh_bit0 = 0		0.25	0.7	mA
V _{DD} output voltage	V _{DD}	22 pin voltage (reference value)	(2.772)	3.3	(3.435)	V
V _{DD} drop-out voltage	V _{DD_drop}	22 pin voltage. Drive mode at 10mA. *Drive current maximum = 10mA		0.15		V
[FM receive characteristics] : fc = 98MHz, V _{IN} = 60dBμV, fm = 1kHz, De-emphasis = 50μs, IF = 225kHz, BW = 50% MONO : 75kHz dev. STEREO : L+R = 67.5kHz dev., Pilot = 7.5kHz dev. Volume level = 3, Soft mute = off, Soft stereo = off, Resister 1Eh Bit 1(LEVSHIF) = 1, 9 pin output, IHF-BPF						
S/N 50dB Sensitivity	SN50	Input level that becomes S/N=50dB		17	24	dBμV
S/N 30dB Sensitivity	SN30	Input level that becomes S/N=30dB		12	18	dBμV
IHF Sensitivity	IHF	Input level that becomes THD=3%		12	20	dBμV
Signal-to-noise ratio	SN	MONO	62	70		dB
	SN-ST1	STEREO	58	66		dB
Total harmonic distortion	THD1	MONO		0.5	1.5	%
	THD1-ST	STEREO		0.5	2.5	%
	THD2	MONO, 150kHz dev.		1.5	5	%
	THD3	MONO, V _{IN} = 120dBμV		0.6	2.5	%

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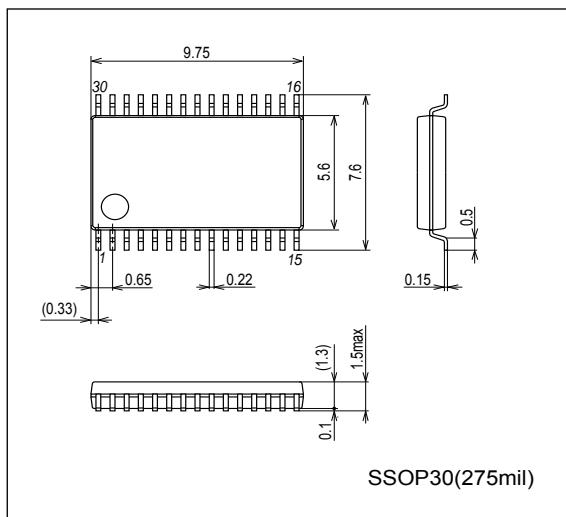
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Demodulation output	V _{O0}	MONO, V _{OL} = 0 (reference value)	(218)	(327)	(489)	mVrms
	V _{O1}	MONO, V _{OL} = 1 (reference value)	(291)	(436)	(652)	mVrms
	V _{O2}	MONO, V _{OL} = 2 (reference value)	(366)	(549)	(821)	mVrms
	V _{O3}	MONO, V _{OL} = 3 (reference value) *In-house management = Typ ± 3.0dB	518	775	1160	mVrms
MPX output	V _{O_MPX}	6 pin output	100	200	300	mVrms
Channel balance	CB	10 pin output / 9 pin output	-1	0	+0	dB
SD operation level	SD	FS_S = 4	17	25	33	dBμV
Stereo operation level	ST	FS_S = 4	17	25	33	dBμV
Stereo separation	Sep	Both channels of 9 pins and 10 pins are measured. *In-house management value ≥25dB	25	40		dB
De-emphasis deflection	Deemp50	fm = 10kHz, 15kHz LPF OFF	-12.5	-10	-7.5	dB
	Deemp75	fm = 10kHz, 15kHz LPF OFF		-13		dB
Carrier leakage	CL	STEREO S/N, 15kHz LPF OFF	30	40		dB
Pilot margin (Pilot lighting sensitivity)	ST-ON	L+R = 67.5kHz, Pilot-mod	0.6		5.5	%
AM suppression ratio	AMR	400Hz AM 30% mod.	40	65		dB
Mute attenuation	MUTE		60	75		dB
[AM receive characteristics] : fc = 1MHz, V _{IN} = 94dBμV, fm = 400Hz, 30% mod, IF = 53kHz, BW = 50% Volume level = 3, Soft mute = 4, Resister 1Eh Bit 1(LEVSHIF) = 1, 9 pin output, 15kHz LPF OFF						
S/N 20dB Sensitivity	SN20	Input level that becomes S/N=20dB		49	65	dBμV
	SN20-L	fc = 603kHz (reference value)		(55)	(65)	dBμV
	SN20-H	fc = 1404kHz (reference value)		(49)	(65)	dBμV
Signal-to-noise ratio	SN		42	50		dB
Total harmonic distortion	THD1			0.6	2.8	%
	THD2	V _{IN} = 104dBμV		0.8	2.8	%
Detected output	V _{O0}	VOL = 0 (reference value)	(55)	(78)	(109)	mVrms
	V _{O1}	VOL = 1 (reference value)	(69)	(98)	(138)	mVrms
	V _{O2}	VOL = 2 (reference value)	(87)	(123)	(173)	mVrms
	V _{O3}	VOL = 3	110	155	218	mVrms
Channel balance	CB	10 pin output / 9 pin output	-1	0	+1	dB
AGC response	AGC1	Input level difference that output level becomes -10dB. Soft mute = 3 (reference value)	(52)	(62)		dB
	AGC2	Soft mute = 4	47	57		dB
Frequency response	Hi-cut	fm = 4kHz	-22	-17	-12	dB
SD operation level	SD	AGC = ON, FS = 4 *In-house management = 46 to 65dBμV	46	54	65	dBμV
Mute attenuation	MUTE	15kHz LPF ON	50	65		dB

Package Dimensions

unit : mm

3191B



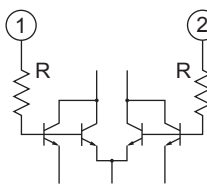
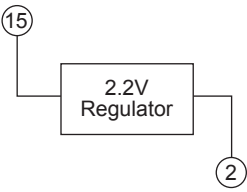
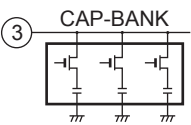
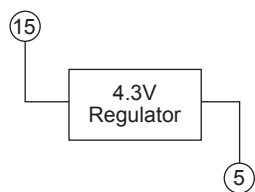
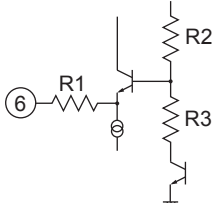
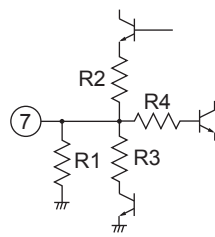
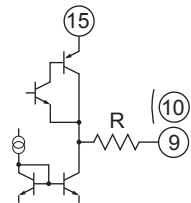
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Pin function

pin	pin name	Description	Remark	DC_bias
1	AM ANT	AM antenna	It connects it to 2pin through the matching coil or the bar antenna.	
2	AM ref	AM reference voltage	It connects it to 1pin through the matching coil or the bar antenna.	2.0V
3	AM CAP	AM capacitor bank	It connects it to GND through an external inductor of recommendation 240 μ H.	
4	GND1	AM antenna GND	Connect to GND	
5	Vref1	Analog reference voltage	It connects it to GND through the capacitor of 1 μ F.	
6	MPX OUT	Detected output	LC72725 and connection when RDS is used	
7	AM AGC	AM AGC	It connects it to GND through the capacitor of 4.7 μ F	
8	GND2	Analog GND	Connect to GND	
9	L OUT	L-ch audio output	The DC level changes by setting Resistor 1Eh bit1 (LEVSHIF) to adjust the output level according to the V _{CC} potential.	
10	R OUT	R-ch audio output		
11	V _{CC} Low	Low voltage mode	It is short with 15pin when using it with V _{CC} < 6.0V or less.	
12	AM LCF	AM low cutting filter	It connects it to GND through the capacitor of 0.047 μ F	
13	SD OUT	SD detecting phase output		
14	ST OUT	ST detecting phase output		
15	V _{CC}	Supply voltage		
16	CLK IN	Reference clock input	The crystal is recommended to be used. It is also possible to input directly clock signals (square wave GND standard).	
17	ST ADJ	Pilot margin adjustment pin	It connects it to GND through 180k Ω	
18	CE	address/data switching timing		
19	CL	Communication clock		
20	DI	Data input		
21	DO	Data output	It connects it to 22 pin through 10k Ω	
22	Vref2	V _{DD} voltage output	3.3V voltage output pin. It is also possible to supply the current to other IC up to 10mA.	
23	GND3	Logic GND	Connect to GND	
24	L1	Local oscillation circuit	It connects it to 25 pin through 33nF.	
25	Vref3	Reference voltage for local oscillation circuit	It connects it to GND through the capacitor of 100 μ F	
26	L2	Local oscillation circuit	It connects it to 25 pin through 33nF.	
27	SD ADJ	SD = ON sensitivity adjustment pin	It connects it to GND through 22k Ω	
28	FLL CAP	FLL low pass filter	It connects it to 25 pin through 0.1 μ F.	
29	GND4	FM antenna GND	Connect to GND	
30	FM ANT	FM antenna	Input impedance 75 Ω .	

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Description of Pin Functions

No.	Pin name	Voltage (V)	Internal Equivalent Circuit	Remarks
1	AM-ANT	2.2V		AM antenna input pin. The AM antenna coil is connected between 2pin. R = 100Ω
2	AM-REF	2.2V		AM standard bias pin.
3	AM-CAP	-		AM Tuning for tune pin. (AM Capacitor Bank)
4	GND1	0V		Analog (AM_FE) GND pin.
5	VREF1	4.3V		Analog (tuner area) standard bias pin. VREF = 4.3V
6	MPX-OUT	2.5V		FM demodulation output pin. R1 = 100Ω R2 = 23kΩ R3 = 1kΩ
7	AM RF-AGC	-		AGC pin for AM-RF department Gain control. R1 = 2MΩ R2 = 5kΩ R3 = 250Ω R4 = 1kΩ
8	GND2	0V		Analog (tuner) GND pin.
9 10	L-OUT R-OUT	2.5V (It is 3.3V for LEVSHIF = 1)		L-ch (R-ch) output pin. R = 100Ω R _{OUT} = 150Ω

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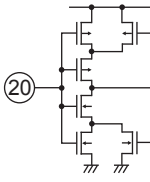
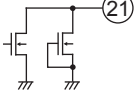
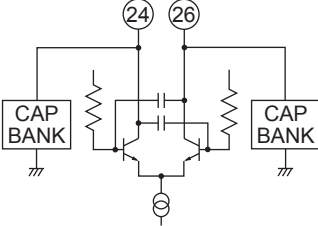
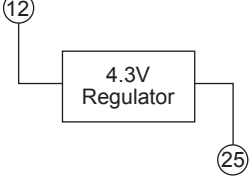
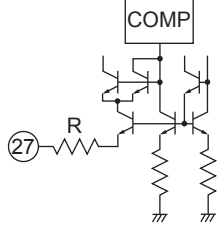
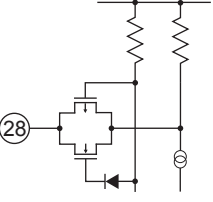
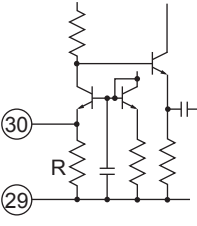
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No.	Pin name	Voltage (V)	Internal Equivalent Circuit	Remarks
11	V _{CC} -Low	-		It is short 11pin with 15pin when using it with V _{CC} < 6.0V.
12	AM LCF	2.2V		AM Low-cut Filter pin. R1 = 250Ω R2 = 100kΩ R3 = 100kΩ R4 = 50kΩ R5 = 50kΩ
13	SD-OUT	V _{DD}		SD indicator output pin. Active Low output R = 100kΩ
14	ST-OUT	V _{DD}		FM stereo indicator output pin. Active Low output R = 100kΩ
15	V _{CC}	V _{CC}		Analog area supply voltage pin. 8.5 to 9.5V are impressed at Resister 1Eh bit 1(LEVSHIF) = 1, and it is short at "0" with V _{CC} _Low.
16	CLK_IN	2.1V		Clock connection pin for internal standard. 32.768kHz crystal is connected. R = 100Ω
17	ST-ADJ	3.7V		Stereo lighting sensitivity adjustment pin. It connects it to GND through 180kΩ. R = 24kΩ
18	CE	-		Chip enable pin. Pin assumed to be high-level when serial data input (DI) and serial data output (DO).
19	CL	-		Data clock input pin Clock that takes data and synchronization when serial data input (DI) and serial data output (DO).

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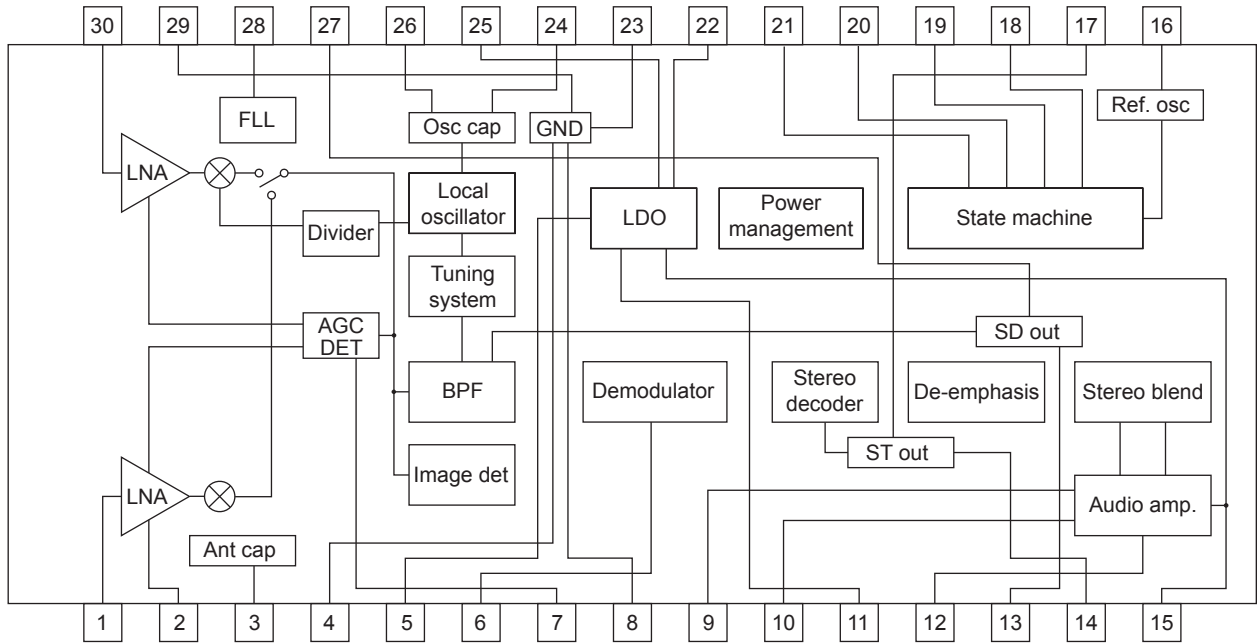
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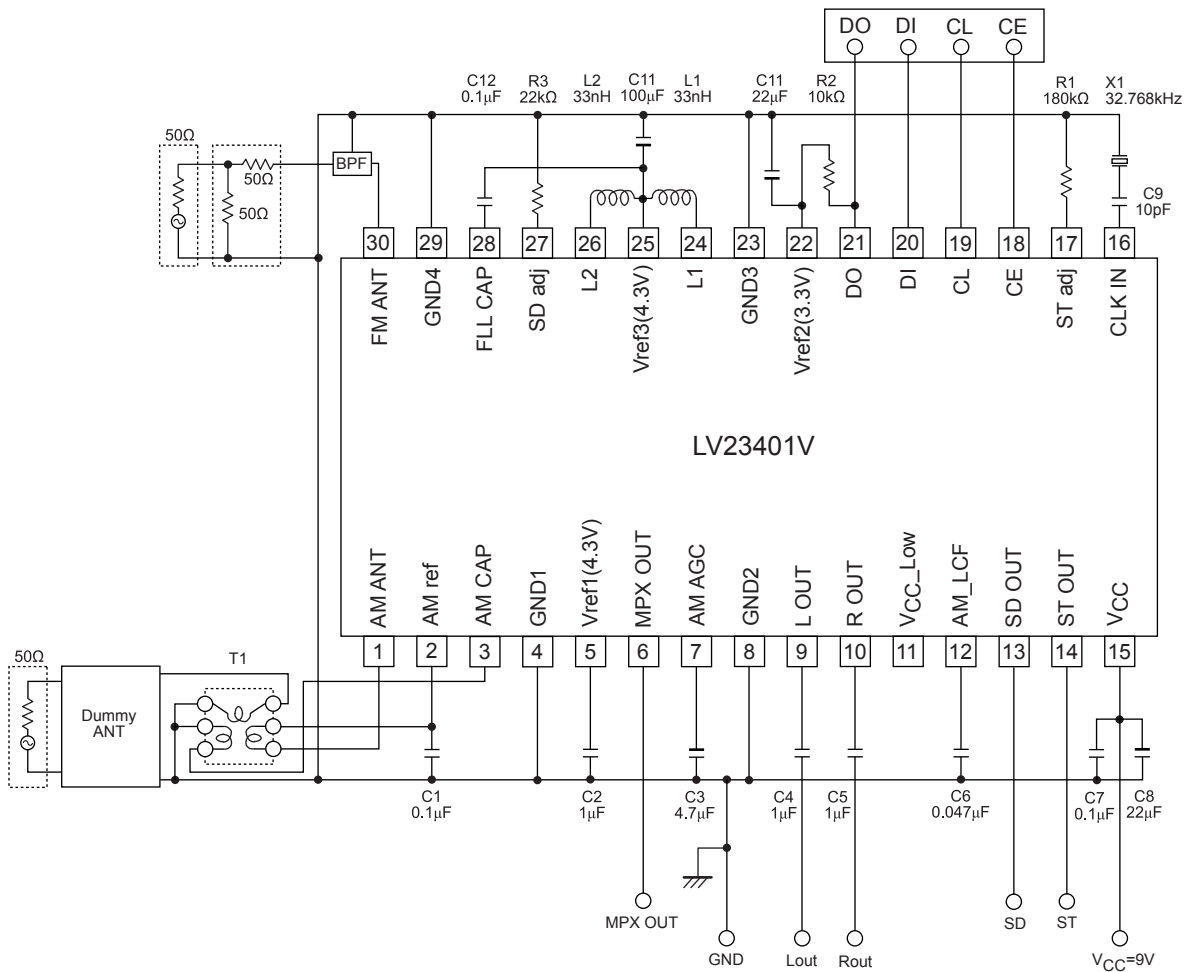
No.	Pin name	Voltage (V)	Internal Equivalent Circuit	Remarks
20	DI	-		Serial data input pin. Input pin of the serial data transmitted by controller.
21	DO	-		Serial data output pin. Serial data output pin to controller.
22	V _{DD}	3.3V		Logic area standard bias pin. V _{DD} = 3.3V
23	GND3	0V		Digital area (control block) GND pin.
24 26	L1 L2	4.3V		OSC coil connect pin. 33nH is connected between 25pin.
25	VREF2	4.3V		OSC area standard bias pin. VREF2 = 4.3V
27	SD-ADJ	0.1V		SD lighting sensitivity adjustment pin. It connects it to GND through 22kΩ. R = 100Ω
28	FLL-CAP	-		LPF pin for internal FLL control. R = 80kΩ
29	GND4	0V		Analog (FMRF) GND pin.
30	FM-ANT	0.9V		FM antenna input pin. R = 1.5kΩ R _{IN} = 75Ω

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Block Diagram

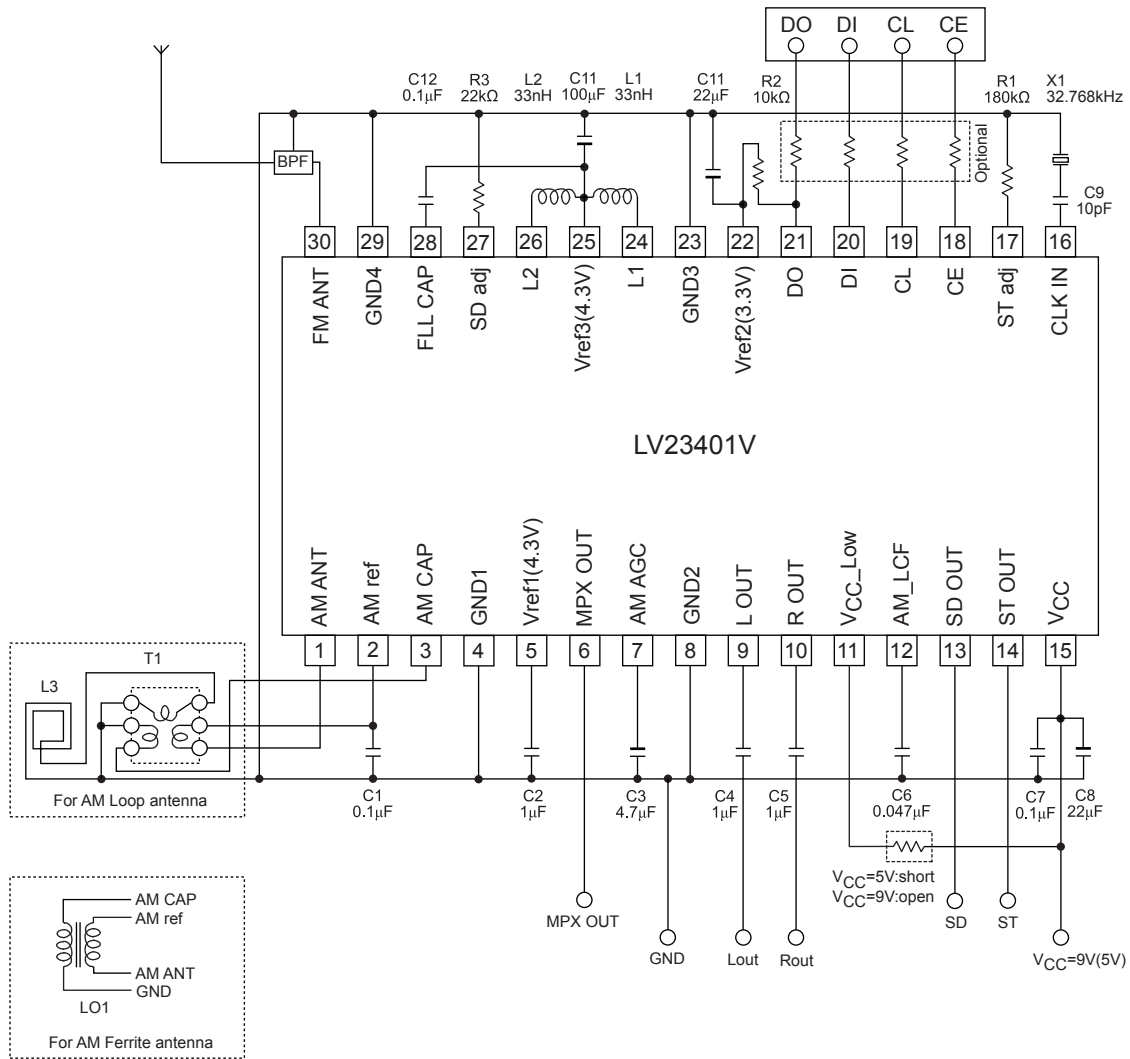


Measurement circuit



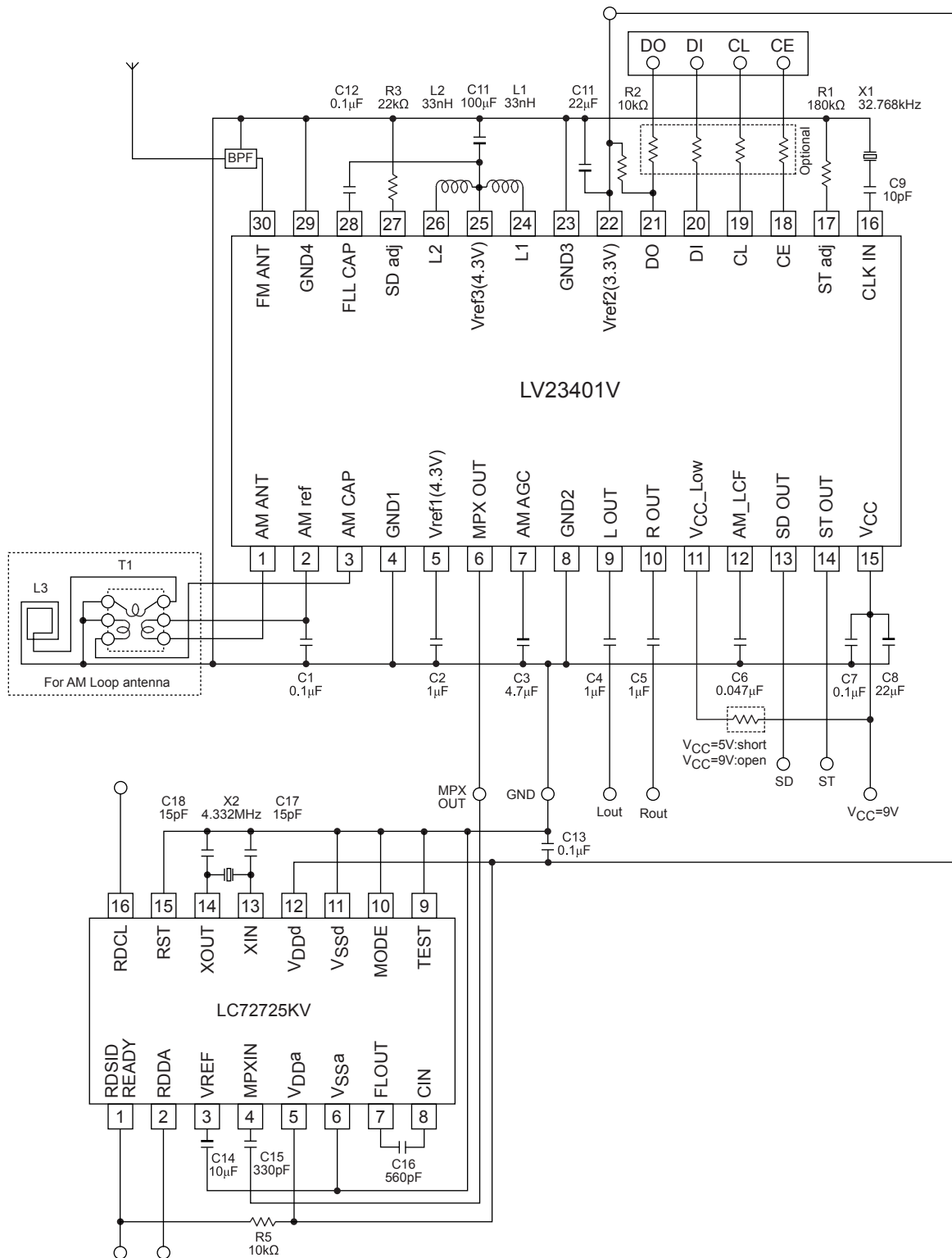
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Example of applied circuit 1



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Example of applied circuit 2



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Used parts

Component	Parameter	Value	Tolerance	Type	Supplier
L1	Local Osc Coil	33nH	5%	LL2012-FHL33NJ	TOKO
L2	Local Osc Coil	33nH	5%	LL2012-FHL33NJ	TOKO
L3	AM Loop antenna	18.1μH	5%	4910-CSL18R1JN1	SAGAMI
T1	AM RF matching	-	-	A90326057	COILS
				#7003RNS-A1109YZS	TOKO
C1	Ripple Filter	0.1μF			
C2	Ripple Filter	1μF			
C3	AM RF AGC Capacitor	4.7μF			
C4	Coupling Capacitor	1μF			
C5	Coupling Capacitor	1μF			
C6	AM Low-cut Filter	0.047μF			
C7	Supply Bypass Capacitor	0.1μF			
C8	Supply Bypass Capacitor	22μF			
C9	Correction Capacitor	10pF			
C10	Supply Bypass Capacitor	22μF			
C11	Ripple Filter	0.1μF			
C12	Osc Filter	0.1μF			
C13	Ripple Filter	0.1μF			
C14	Ripple Filter	10μF			
C15	Coupling Capacitor	330pF			
C16	Coupling Capacitor	560pF			
C17	Correction Capacitor	15pF			
C18	Correction Capacitor	15pF			
R1	Reference Resistor	180Ω			
R2	Pulled-up Resistor	10kΩ			
R3	Reference Resistor	22kΩ			
R4	Reference Resistor	33kΩ			
R5	Pulled-up Resistor	10kΩ			
BPF	FM ANT BPF	-	-	GFMB7	SOSHIN
X1	Crystal	32.768kHz	100ppm	VT-200-F(12.5pF)	SEIKO
X2	Crystal	4.332MHz	100ppm	AT-49	DAISHINKI
LO1	AM Ferrite antenna	260μH	TBD	-	-

* L1 must be used when you receive an Eastern European band (65MHz to 75MHz) and L2 must use 39nH.

* Inquire match (C9, C17, C18) of X1 and the X2 crystal of the crystal maker together with the substrate used.

Interface specification

1) LV23401 Interface specification

LV23401 is controlled by the C²B (Computer Control Bus) cereal bus format.

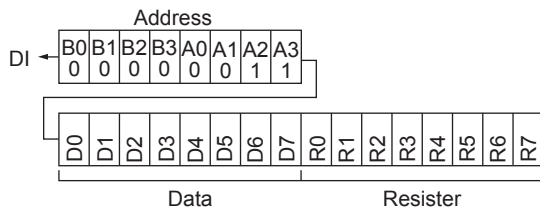
C²B is a bus to achieve it economically surely format as for the communications between LSI in the system with two or more LSI. Because it is single master's system, the processing of a complex arbitration is unnecessary. Therefore, the load of hardware is reduced, and the system configuration that is economically abundant becomes possible.

Moreover, neither a lot of kinds of controller and interface doing nor special hardware is easily needed by serial I/O with software. C²B is thought between LSI in the equipment, and the communications between equipment that need a long line are not targeted.

2) C2B data composition

DI control data (cereal data input) composition

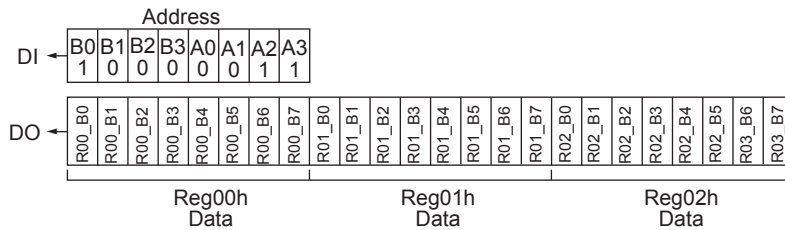
IN mode



LV23401V is controlled by the bus format composed of the sub-address (register) that stores the data of the device address of 8bit (address) and each 8bit. "C0" is input from LSB to the start as an address when the serial data is input to LV23401V, the device that controls is specified, and the mode as the data input is fixed. It inputs from LSB in order of data (bit setting) → register synchronizing with data clock (CL) after the address is input and the data input can be concluded.

Composition of the DO control data (serial data output)

OUT mode



"C1" is input from LSB to the start as an address when the serial data is output from LV23401V, the controlled device is specified, and the mode as the data output is fixed. The subsequent data is output from DO pin synchronizing with lock (CL) after the address is input LSB from one with small register number. The output of data is ended by setting CE pin to Low.

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3) Description of the Register of LV23401

Register 00h – CHIP_ID – Chip identify register (Read-Only)

7	6	5	4	3	2	1	0
ID[7:0]							
Bit 7-0 : ID[7:0] : 8-bit CHIP ID. LV23400 : 18h							
Note : To abort the command, write any value in this register.							

Register 01h – CHIP_REV – Chip Revision identify register (Read-Only)

7	6	5	4	3	2	1	0
Revision[7:0]							
Bit 7-0 : ID[7:0] : 8-bit Chip revision ES1 : 00h							
Note : To abort the command, write any value in this register.							

Register 02h – RADIO_STAT – Radio station status (Read-Only)

7	6	5	4	3	2	1	0
IM_STAT	IM_FS[1:0]		MO_ST	FS[2:0]		TUNED	
Bit 7 : IM_STAT : State of image evasion code 0 = Eternal operation (It is possible to write it.) 1 = The image evasion is being processed. (Writing is improper.)							
Note : This bit operates only when Resister 14h_bit7 (IM_EVAS) is set to "1". The data writing processing to LV23401 when this bit is "1" is prohibited.							
Bit 6 - 5 : IM_FS : Image bureau electric field strength 0 : Image bureau none 1 : 0 2 : 0dB to 10dB compared with the hope bureau. 3 : The level of the image bureau is +10dB or more stronger than that of the hope bureau.							
Bit 4 : MO_ST : MONAURAL/STEREO display 0 = Stereo reception (Compelling the monaural setting is also the same.) 1 = Receiving in stereo mode.							
Bit 3 - 1 : FS[2:0] : Field strength 0 : Field strength < 10dBμV 1 : Field strength 10 to 20dBμV 2 : Field strength 20 to 30dBμV ••• 3 : Field strength > 70dBμV							
Bit 0 : TUNED : Radio-tuning flag 0 = No tuning. 1 = The tuning.							
Note : When the frequency tuning succeeds, this bit is set. This flag is cleared under the following three conditions. 1. PW_RAD = 0 2. Do the tuning of the frequency. 3. When FLL becomes outside the correction range							
Only when the TUNED flag is changed from one into 0, the RAD_IF interrupt flag is set. When the status of TUNED changes from 0 into one, the interrupt is not generated.							

Register 04h – TNPL – Tune position low (Read-Only)

7	6	5	4	3	2	1	0
TUNEPOS[7:0]							
Bit 7-0 : TUNEPOS[7:0] : Current RF frequency (Low 8bit)							

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Register 05h – TNP_H_STAT – Tune position high / status (Read-Only)

7	6	5	4	3	2	1	0
ERROR[1:0]		TUNEPOS[12:8]					
Bit 7 – 6 :		ERROR[1:0] : Error code					
		ERROR[1:0]		Remark			
		0		OK, Command end (No Error)			
		1		DAC Limit Error			
		2		Command forced End			
		3		Command busy (executing it)			
Bit 5 – 0 :		TUNEPOS[13:8] : Current RF frequency (High 5 bit)					

Register 06h – COUNT_L – Counter low (Read-Only)

7	6	5	4	3	2	1	0
COUNT[7:0]							
Bit 7 – 0 :		COUNT[7:0] : Counter value (Low 8bit)					

Register 07h – COUNT_H – Counter High (Read Only)

7	6	5	4	3	2	1	0
COUNT[15:8]							
Bit 7 – 0 :		COUNT[15:8] : Counter value (High 8bit)					

Register 08h – IF_{OSC} – DAC for IF OSC (Read/Write)

7	6	5	4	3	2	1	0
IFOSC[7:0]							
Bit 7 – 0 :		IFOSC[7:0] : IF Oscillator DAC					

Register 09h – IF_{BW} – DAC for IF – Filter Band width (Read/Write)

7	6	5	4	3	2	1	0
IFBW[7:0]							
Bit 7 – 0 :		IFBW[7:0] : IF Band-pass Filter Band DAC					

Register 0Bh – STEREO_{OSC} – DAC for Stereo Decoder OSC (Read/Write)

7	6	5	4	3	2	1	0
SDOSC[7:0]							
Bit 7 – 0 :		SDOSC[7:0] : Stereo Decoder Oscillator DAC					

Register 0Ch – RF_{OSC} – DAC for RF OSC (Read/Write)

7	6	5	4	3	2	1	0
RFCAP[7:0]							
Bit 7 – 0 :		RFOSC[7:0] : RF Oscillator DAC					

Register 0Dh – RFCAP – RF Cap bank (Read/Write)

7	6	5	4	3	2	1	0
RFCAP[7:0]							
Bit 7 – 0 :		RFCAP[7:0] : RF Oscillator Capacitor bank					

Register 0Eh – AMCAP1 – AM-ANT Cap bank1 (Read/Write)

7	6	5	4	3	2	1	0
AMCAP[7:0]							
Bit 7 – 0 :		AMCAP[7:0] : AM Antenna Capacitor bank					
Note : The AM antenna capacitor bank is composed of 12 bits. High 4 bits are arranged in AMCTRL register.							

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Register 0Fh – AMCTRL – AM Station Control (Read/Write)

7	6	5	4	3	2	1	0																								
AMDIV[2:0]			AM_CAL	ACAP11	ACAP10	ACAP9	ACAP8																								
Bit 7 – 5 : AMDIV[2:0] : AM Clock Divider Bit 7 : AM_CD2 : AM Clock Divider bit 2. Bit 6 : AM_CD1 : AM Clock Divider bit 1. Bit 5 : AM_CD0 : AM Clock Divider bit 0. Note : AMCD[2:0] uses the frequency of FM belt even for the AM belt to lower. Set the machine of the AM dividing frequency to turning off at FM mode. <table style="margin-left: 40px; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">AM_CD[2:0]</th> <th style="text-align: center;">Rate of dividing frequency</th> <th style="text-align: center;">Rough estimate AM-RF frequency (In kHz)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0,1</td> <td style="text-align: center;">Divider OFF</td> <td style="text-align: center;">0 (FM mode)</td> </tr> <tr> <td style="text-align: center;">2</td> <td style="text-align: center;">224</td> <td style="text-align: center;">338 – 483</td> </tr> <tr> <td style="text-align: center;">3</td> <td style="text-align: center;">160</td> <td style="text-align: center;">474 – 676</td> </tr> <tr> <td style="text-align: center;">4</td> <td style="text-align: center;">112</td> <td style="text-align: center;">676 – 966</td> </tr> <tr> <td style="text-align: center;">5</td> <td style="text-align: center;">80</td> <td style="text-align: center;">947 – 1353</td> </tr> <tr> <td style="text-align: center;">6</td> <td style="text-align: center;">64</td> <td style="text-align: center;">1183 – 1692</td> </tr> <tr> <td style="text-align: center;">7</td> <td style="text-align: center;">48</td> <td style="text-align: center;">1578 - 2256</td> </tr> </tbody> </table>								AM_CD[2:0]	Rate of dividing frequency	Rough estimate AM-RF frequency (In kHz)	0,1	Divider OFF	0 (FM mode)	2	224	338 – 483	3	160	474 – 676	4	112	676 – 966	5	80	947 – 1353	6	64	1183 – 1692	7	48	1578 - 2256
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3	160	474 – 676																													
4	112	676 – 966																													
5	80	947 – 1353																													
6	64	1183 – 1692																													
7	48	1578 - 2256																													
Bit 4 : NA (0 Fixation) Bit 3 – 0 : AMCAP[11:8] : AM antenna capacitor bank. Bit 3 : AMCAP_bit11 Bit 2 : AMCAP_bit10 Bit 1 : AMCAP_bit9 Bit 0 : AMCAP_bit8																															

Register 10h – DO_REF_CLK_CNF – Do output mode and reference clock configuration (Read/Write)

7	6	5	4	3	2	1	0										
IPOL	DO_SEL[1:0]		EXT_CLK_CFG[1:0]		FS_S[2:0]												
Bit 7 : IPOL : Indicator (DO pin _SD/ST mode) polarity 0 = SD/ST Active Low (The same state change as 13pin – SD pin / 14pin – ST pin) 1 = SD/ST Active High (State change opposite to 13pin – SD pin / 14pin – ST pin) Note : This bit doesn't influence the polarity of the serial data. Bit 6 -5 : DO_SEL : DO pin select (DO pin output mode select) <table style="margin-left: 40px; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">DO_SEL[1:0]</th> <th style="text-align: center;">DO pin</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00</td> <td style="text-align: center;">Serial data output mode</td> </tr> <tr> <td style="text-align: center;">01</td> <td style="text-align: center;">ST pin mode</td> </tr> <tr> <td style="text-align: center;">10</td> <td style="text-align: center;">SD pin mode</td> </tr> <tr> <td style="text-align: center;">11</td> <td style="text-align: center;">Local position confirmation mode</td> </tr> </tbody> </table>								DO_SEL[1:0]	DO pin	00	Serial data output mode	01	ST pin mode	10	SD pin mode	11	Local position confirmation mode
DO_SEL[1:0]	DO pin																
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01	ST pin mode																
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11	Local position confirmation mode																
DO pin is used by observing the position (Upper heterodyne / Lower heterodyne) of a state of SD pin/ST pin besides the serial data output and local OSC. * The state of DO pin changes synchronizing with SD pin / ST pin when DO_SEL is set to (01b) or (10b). * The state of DO pin changes by the position of Local OSC when DO is set to (11b). Lower heterodyne = 0, Upper heterodyne = 1 * Set DO_SEL to (00b) when you output the serial data. Bit 4 – 3 : EXT_CLK_CFG[1:0] : External clock setting <table style="margin-left: 40px; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">EXT_CLK_CFG[1:0]</th> <th style="text-align: center;">Reference clock</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00</td> <td style="text-align: center;">Off</td> </tr> <tr> <td style="text-align: center;">01</td> <td style="text-align: center;">The external clock is supplied.</td> </tr> <tr> <td style="text-align: center;">10</td> <td style="text-align: center;">32768Hz Crystal oscillation</td> </tr> <tr> <td style="text-align: center;">11</td> <td style="text-align: center;">Unused</td> </tr> </tbody> </table>								EXT_CLK_CFG[1:0]	Reference clock	00	Off	01	The external clock is supplied.	10	32768Hz Crystal oscillation	11	Unused
EXT_CLK_CFG[1:0]	Reference clock																
00	Off																
01	The external clock is supplied.																
10	32768Hz Crystal oscillation																
11	Unused																
Bit 2 – 0 : FS_S[2:0] : SD(Station Detector) operate level setting (distinguishes at the FS level)																	

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Register 11h – IF_SEL – IF frequency selection (Read/Write)

7	6	5	4	3	2	1	0																																																																																																																
FLL_MOD		AMIF[2:0]			FMIF[3:0]																																																																																																																		
<p>Bit 7 : FLL_MOD : FLL operation mode 0 : Smoothing filter = OFF 1 : Smoothing filter = ON</p> <p>Bit 6 -4 : AMIF[2:0] : IF frequency setting when AM mode is selected</p> <table border="1" style="margin-left: 40px; border-collapse: collapse; text-align: center;"> <tr> <th colspan="8">AMIF[2:0]</th> </tr> <tr> <th>0</th> <th>1</th> <th>2</th> <th>3</th> <th>4</th> <th>5</th> <th>6</th> <th>7</th> </tr> <tr> <td>20kHz</td> <td>31kHz</td> <td>42kHz</td> <td>53kHz</td> <td>64kHz</td> <td>75kHz</td> <td>86kHz</td> <td>97kHz</td> </tr> </table> <p>Bit 3 – 0 : FMIF[3:0] : IF frequency setting when FM mode is selected (kHz)</p> <table border="1" style="margin-left: 40px; border-collapse: collapse; text-align: center;"> <tr> <th rowspan="2">SE_</th> <th rowspan="2">RF_</th> <th colspan="16">FMIF[3:0]</th> </tr> <tr> <th>0</th> <th>1</th> <th>2</th> <th>3</th> <th>4</th> <th>5</th> <th>6</th> <th>7</th> <th>8</th> <th>9</th> <th>10</th> <th>11</th> <th>12</th> <th>13</th> <th>14</th> <th>15</th> </tr> <tr> <td>AM</td> <td>SEL</td> <td>0</td> <td>1</td> <td>2</td> <td>3</td> <td>4</td> <td>5</td> <td>6</td> <td>7</td> <td>8</td> <td>9</td> <td>10</td> <td>11</td> <td>12</td> <td>13</td> <td>14</td> <td>15</td> </tr> <tr> <td>0</td> <td>0</td> <td>112.5</td> <td>125</td> <td>137.5</td> <td>150</td> <td>162.5</td> <td>175</td> <td>187.5</td> <td>212.5</td> <td>225</td> <td>237.5</td> <td>250</td> <td>262.5</td> <td>275</td> <td>287.5</td> <td>312.5</td> <td>325</td> </tr> <tr> <td>0</td> <td>1</td> <td>112.5</td> <td>127.5</td> <td>142.5</td> <td>157.5</td> <td>157.5</td> <td>172.5</td> <td>187.5</td> <td>202.5</td> <td>217.5</td> <td>232.5</td> <td>247.5</td> <td>262.5</td> <td>277.5</td> <td>292.5</td> <td>307.5</td> <td>322.5</td> </tr> </table>								AMIF[2:0]								0	1	2	3	4	5	6	7	20kHz	31kHz	42kHz	53kHz	64kHz	75kHz	86kHz	97kHz	SE_	RF_	FMIF[3:0]																0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	AM	SEL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	0	112.5	125	137.5	150	162.5	175	187.5	212.5	225	237.5	250	262.5	275	287.5	312.5	325	0	1	112.5	127.5	142.5	157.5	157.5	172.5	187.5	202.5	217.5	232.5	247.5	262.5	277.5	292.5	307.5	322.5
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Register 12h – REF_CLK_MOD – Slope correction (Read/Write)

7	6	5	4	3	2	1	0
REFMOD[7:0]							
Bit 7 – 0 : REFMOD[7:0] : Reference clock correction							
<p>Note : As for this register, a set value is different according to the crystal connected with 16pin and the input clock. Inform of a set value of this register when you adopt the applications other than an example of applied circuit and recommended parts of this specifications.</p>							

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Register 13h – SM_CTRL – Statemachine control (Read/Write)

7	6	5	4	3	2	1	0
FLL_ON	CLKS_SE[2:0]			nSD_PM	nIF_PM	DM_SE[1:0]	
<p>Bit 7 : FLL_ON : FLL control 0 = FLL OFF 1 = FLL ON</p> <p>Bit 6 – 4 : CLKS_SE : Clock course select 0 = No select 1 = The source of the stereo decoder oscillator is effective. 2 = The source of the IF oscillator is effective. 3 = The source of the AM antenna oscillator is effective. 4 = The source of the FM-RF oscillator is effective. 5 = The source of the AM-RF oscillator is effective. 6 – 7 = no select</p> <p style="padding-left: 40px;">Note : Bit[6-4] selects the source of the oscillator. Select the arbitrary source that to be adjusted and to be measured.</p> <p>Bit 3 : nSD_PM : Stereo decoder clock PLL mute 0 = SD PLL OFF (Adjustment) 1 = SD PLL ON (Operation usually)</p> <p>Bit 2 : nIF_PM : IF PLL mute 0 = IF PLL OFF (Adjustment) 1 = IF PLL ON (Operation usually)</p> <p>Bit 1 – 0 : CM_SE : Command mode select 0 = Command no select 1 = Measurement mode 2 = Adjustment mode 3 = Radio tuning (reception frequency adjustment) mode</p> <p style="padding-left: 40px;">Note : This bit is used to select the command mode. Select the arbitrary command to be executed. The command is executed by setting TARGET_VAL_L/H.</p> <p style="padding-left: 40px;">Command execution time : SD calibration = 540ms IF calibration = 134ms RF(FM) tuning = 105ms RF(AM) tuning = 158ms * Stand-by at time to have provided for the above-mentioned before all processing including reading the register value after having executed the command.</p>							

Register 14h – REF_CLK_PRS – Reference clock pre-scalar (Read/Write)

7	6	5	4	3	2	1	0
IM_EVAS	Reserved	WAIT_SEL	A<_FINE	REFPRE[3:0]			
<p>Bit 7 : IM_EVAS : Image evasion function ON/OFF 0 = The image bureau is not evaded. 1 = The image bureau is evaded. (recommendation)</p> <p>Bit 6 : Reserved : 0 fixation</p> <p>Bit 5 : WAIT_SEL : Selection after tuning at mute release standby time 0 = 8ms standby 1 = 4ms standby</p> <p>Bit 4 : AM_FINE : Selection at AM_ANT adjustment standby time 0 = No standby after switch of DAC 1 = 2ms standby after switch of DAC</p> <p>Bit 3 – 0 : REFPRE[3:0] : Standard Clock Pre-scalar 0 = 1:1 1 = 1:2 2 = 1:4 ••• 15 = 1:32768</p>							

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Register 15h – REF_CLK_DIV – Reference clock divider (Read/Write)

7	6	5	4	3	2	1	0
REFDIV[7:0]							
Bit 7 – 0 : REFDIV[7:0] : Standard clock divider 0 : Rate of dividing frequency = 1 1 : Rate of dividing frequency = 2 ... 255 : Rate of dividing frequency =256							

Register 16h – TARGET_VAL_L – Target Value Low Register (Read/Write)

7	6	5	4	3	2	1	0
TARGET[7:0]							
Bit 7 – 0 : TARGET[7:0] : Target Frequency Low 8bit : Targeted value of radio tuning and oscillator adjustment : Low byte							

Register 17h – TARGET_VAL_H – Target Value High Register (Read/Write)

7	6	5	4	3	2	1	0
TARGET[15:8]							
Bit 7 – 0 : TARGET[15:8] : Target Frequency High 8 bit : Targeted value of radio tuning and oscillator adjustment : High byte Note : When subordinate position 8bit of the frequency of the target is set when it is on, and high rank of the frequency of the target 8bit is set to this register afterwards, the command is executed as for the radio power.							

TUNEPOS and TARGET :

- 1kHz interval at AM
- 10kHz interval at FM

Register 18h – RADIO_CTRL1 – Radio control 1 (Read/Write)

7	6	5	4	3	2	1	0
IQC_CTR	IFPOL	OSC_LEV[1:0]		DEEM	VOL[1:0]		EN_AMHC
Bit 7 : IQC_CTR : I/Q phase conversion 0 = Operational mode usually (Upper heterodyne) 1 = I/Q phase conversion : Image measures (Lower heterodyne) Note : When the local is switched as an image measures, it uses it.							
Bit 6 : IF polarity conversion in State Machine. 0 = The IF frequency is added to a local frequency. (Operational usually) 1 = The IF frequency is subtracted by a local frequency. (Image measures)							
Bit 5 – 4 : OSC_LEV[1:0] : RF-OSC oscillation level setting 0 = Minimum oscillation level 3 = Maximum oscillation level * A possible level adjustment and "2" are assumed to be a recommended value at each interval of 3dB.							
Bit 3 : DEEN : De-emphasis time constant switch 0 = 50μs : Japan, South Korea, China, and Europe 1 = 75μs : The United States							
Bit 2 – 1 : VOL[1:0] : Volume setting 0 = Minimum (VOL0) ... 3 = Maximum (VOL3)							
Bit 0 : EN_AMHC : AM high cut filter ON/OFF 0 = AM hi-cut filter function OFF 1 = AM hi-cut filter function ON							

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Register 19h – RADIO_CTRL2 – Radio control 2 (Read/Write)

7	6	5	4	3	2	1	0
Reserved	Reserved	EN_AMM	Reserved	IF_AGC_LEV	RF_AGC_LEV[1:0]		EN_RFAGC
<p>Bit 7 : Reserved : 0 fixation</p> <p>Bit 6 : Reserved : 1 fixation</p> <p>Bit 5 : EN_AMM : AM mute ON/OFF 0 = AM mute function OFF 1 = AM mute function ON</p> <p>Bit 4 : Reserved : 0 fixation</p> <p>Bit 3 : IF_AGC_LEV : IF-AGC level control 0 = AGC slow mode 1 = AGC first mode</p> <p>Bit 2 – 1 : RF_AGC_LEV[1:0] : RF-AGC level control 0 = AGC slow mode 1 = AGC normal mode 3 = AGC first mode</p> <p>Bit 0 : EN_RFAGC : RF-AGC ON/OFF 0 = AGC OFF 1 = AGC ON (Operational usually)</p>							

Register 1Ah – RADIO_CTRL3 – Radio control 3 (Read/Write)

7	6	5	4	3	2	1	0
AMOSC_GA[2:0]			AMOSC_DL[2:0]			AMAGC_SP[1:0]	
<p>Bit 7 – 5 : AMOSC_GA[2:0] : AM antenna oscillator gain control 0 = Minimum level 7 = Maximum level</p> <p>Bit 4 – 2 : AMOSC_DL[2:0] : AM oscillator detection level 0 = Minimum level 7 = Maximum level</p> <p>Bit 1 – 0 : AMSGC_SP[1:0] : AM oscillator AGC speed 0 = Slow mode 3 = First mode</p>							

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Register 1Ch – STEREO_CTRL1 – Stereo control 1 (Read/Write)

7	6	5	4	3	2	1	0
CRC[1:0]		SS_SP2	SS_SP1	NA	PICAN_EN	FOSTEREO	ST_M
Bit 7 – 6 : CRC[1:0] : Capture range control 0 = Narrowband mode 1 = Recommended value 3 = Wideband mode Bit 5 : SS_SP2 : STEREO sensitivity speed 2 (First mode) 0 : First mode = OFF 1 : First mode = ON - Recommended value Bit 4 : SS_SP1 : STEREO sensitivity speed 1 (Slow mode) 0 : Slow mode = OFF - Recommended value 1 : Slow mode = ON Bit 3 : NA Bit 2 : PICAN_EN : Pilot cancel function ON/OFF 0 = OFF 1 = ON Bit 1 : FOSTEREO : Compulsion stereo 0 = Operational usually 1 = Compulsion stereo mode Bit 0 : ST_M : STEREO/MONAUURAL setting 0 = Stereo function ON (Operational usually) 1 = Stereo function OFF (Compulsion monaural)							

Register 1Dh – STEREO_CTRL2 – Stereo control 2 (Read/Write)

7	6	5	4	3	2	1	0
NA			FOAMAGC	Reserved	NA	CPAJ[1:0]	
Bit 7 – 5 : NA Bit 4 : FOAMAGC 0 : Compulsion AGC = OFF 1 : Compulsion AGC = ON Bit 3 : Reserved : 0 fixation Bit 2 : NA Bit 1 – 0 : CPAJ[1:0] : Channel separation adjustment 0 = Sub career level minimum 7 = Sub career level maximum							

Register 1Eh – RADIO_CTRL4 – Radio control 4 (Read/Write)

7	6	5	4	3	2	1	0
SOFTST[2:0]			SOFTMU[2:0]			LEVSHIF	FO_SOFTT
Bit 7 – 5 : SOFTST[2:0] : Soft stereo function setting 0 : Soft stereo function = OFF 7 : Soft stereo function = Lev7 (Max) Bit 4 – 2 : SOFTMU[2:0] : Soft audio mute function setting 0 : Soft mute function = OFF 7 : Soft mute function = Lev7 (Max) Bit 1 : LEVSHIF : Audio line DC level shift 0 = Normal DC level (V _{CC} =5.0V supply) 1 = DC level shift (V _{CC} =9.0V supply) Bit 0 : FO_SOFTST : Compulsion soft stereo function setting 0 : Compulsion soft stereo function = ON 1 : Compulsion soft stereo function = OFF * Set it to "0" when corresponding to European immunity standard.							

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Register 1Fh – RADIO_XTRL5 – Radio control 5 (Read/Write)

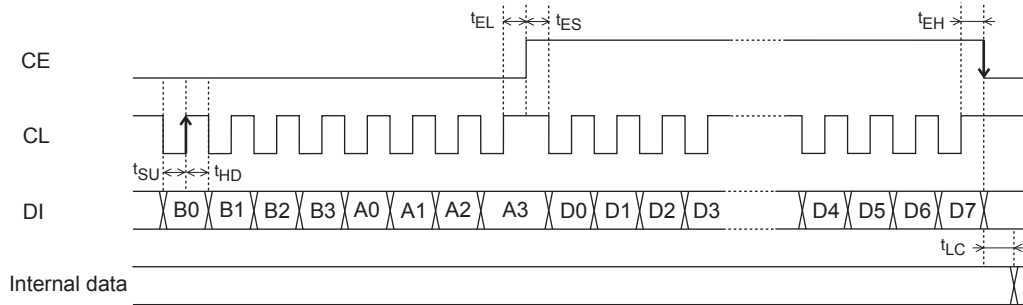
7	6	5	4	3	2	1	0
RF_SEL	IFRIM	nAGC_SPD	SE_FM/AM	AMP_CTR	MUTE	NA	PW_RAD
<p>Bit 7 : RF_SEL : RF frequency range setting 0 = Normal (Japan / USA / Europe) 1 = Eastern Europe (65MHz to 74MHz)</p> <p>Bit 6 : IFRIM : IF oscillator limit setting 0 : Max = 350kHz (FM mode) 1 : Max =150kHz (AM mode)</p> <p>Bit 5 : nAGC_SPD : IF AGC speed setting 0 = Hi speed (FM mode) 1 = Normal (AM mode)</p> <p>Bit 4 : SE_FM/AM : AM/FM mode select 0 = FM mode 1 = AM mode</p> <p>Bit 3 : AMP_CTR : Audio amplifier ON/OFF 0 = OFF 1 = ON</p> <p>Bit 2 : MUTE : Audio mute function ON/OFF 0 = Mute ON 1 = Mute OFF</p> <p>Bit 1 : AM_CAL : AM calibration (Oscillation mode) 0 = AM calibration impropriety (Operational usually) 1 = AM calibration mode (AM antenna frequency setting time) Note : Set this bit to "1" when you measure the frequency of the AM antenna.</p> <p>Bit 0 : PW_RAD : Radio circuit power 0 = Power OFF (Power save) 1 = Power ON</p> <p>* 1 : After the V_{CC} voltage is impressed, PW_RAD of Register 1Fh_bit0 is automatically set to "0" in 50ms. * 2 : When the V_{CC} voltage is dropped once, content of registers other than PW_RAD becomes irregular. * 3 : The content of the register change set at the power save becomes effective, and any command processing cannot be executed. * 4 : The standby time of 1200ms is necessary, the circuit with stability (PW_RAD = 0 → 1) after the power save returns. * 5 : Tune RF again after the power save returns. * 6 : A built-in each oscillator including the RF bureau departure and all other analogue part circuit operation stop at the power save. * 7 : The standby time of 200ms is necessary after the switch of the band to AM before counting IF after adjusting the first RF.</p>							

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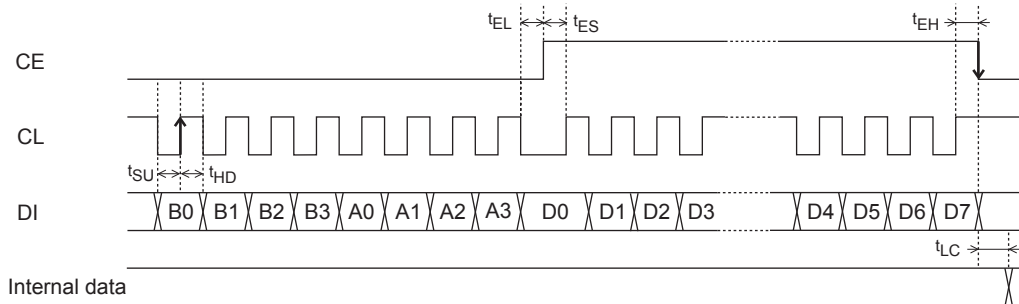
4) C²B communication timing specification

Serial data input (IN1/IN2) $t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} \geq 0.75\mu s$ $t_{LC} < 0.75\mu s$

CL : Normally Hi

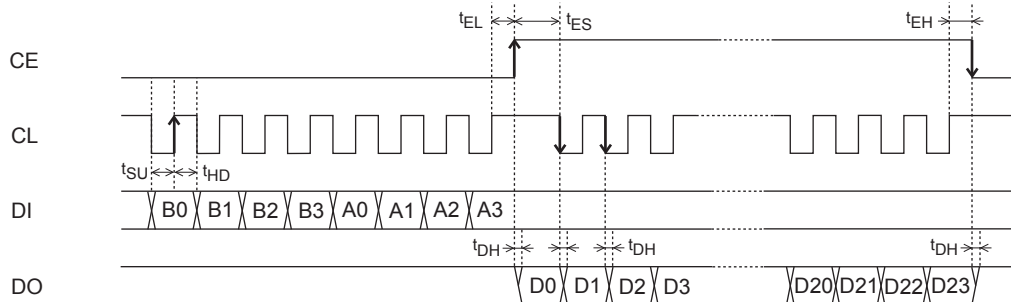


CL : Normally Low

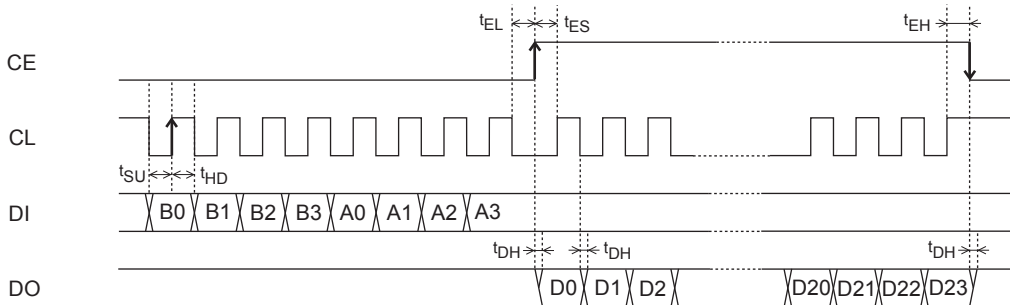


Serial data output (OUT) $t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} \geq 0.75\mu s$ $t_{DC}, t_{DH} < 0.35\mu s$

CL : Normally Hi



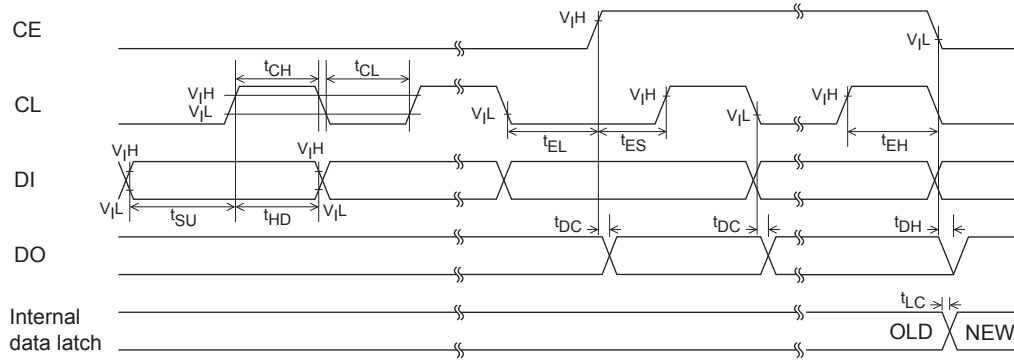
CL : Normally Hi



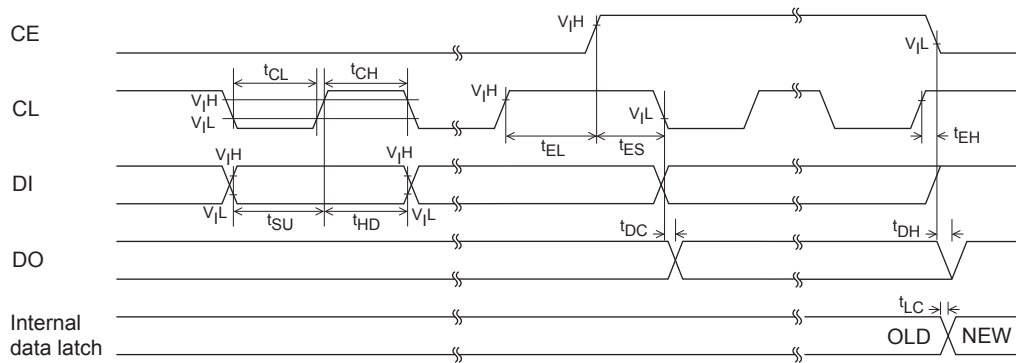
(Note) DO pin is an Nch open drain pin, so that the data varying time (t_{DC} and t_{DH}) differs depending on the pull-up resistance and substrate capacity.

LV23401V

Serial data timing



<< When CL stops at the "L" level >>



<< When CL stops at the "H" level >>

Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	t_{SU}	DI, CL		0.75			μs
Data hold time	t_{HD}	DI, CL		0.75			μs
Clock "L" level time	t_{CL}	CL		0.75			μs
Clock "H" level time	t_{CH}	CL		0.75			μs
CE wait time	t_{EL}	CE, CL		0.75			μs
CE setup time	t_{ES}	CE, CL		0.75			μs
CE hold time	t_{EH}	CE, CL		0.75			μs
Data latch change time	t_{LC}					0.75	μs
Data output time	t_{DC}	DO, CL	Differs depending on the pull-up resistance and substrate capacity			0.35	μs
	t_{DH}	DO, CE					

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