

# SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV24250LS

# Bi-CMOS LSI Compact Portable Equipment 1-Chip FM Tuner IC

## **Overview**

The LV24250LS is an I<sup>2</sup>C-controlled single-chip FM tuner IC that integrates external components which are necessary for tuning in a compact VQLP package with dimensions of only 3.5mm×3.5mm.

## Features

- FM FE
- FM IF
- MPX stereo decoder
- FLL Tuning
- Standby

## **Specifications**

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max	Analog block supply voltage	5.0	V
	V <sub>DD</sub> max	Digital block supply voltage	4.0	V
Maximum input voltage	V <sub>IN</sub> 1 max	SCL, SDA, Int	V <sub>DD</sub> +0.3	V
	V <sub>IN</sub> 2 max	External_clk_in	V <sub>DD</sub> +0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C *	140	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

\*: When mounted on the specified printed circuit board (40.0mm × 50.0 mm × 0.8mm), Four layers glass epoxy (2S2P)

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#### **Operating Conditions** at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V <sub>CC</sub>	Analog block supply voltage	3.0	V
	V <sub>DD</sub>	Digital block supply voltage	3.0	V
Operating supply voltage range	V <sub>CC</sub> op		2.6 to 3.6	V
	V <sub>DD</sub> op		2.5 to 3.6	V
	V <sub>IO</sub> op	Interface voltage	2.2 to 3.6	V

Note : Supply voltage V\_{IO} equal V\_{DD}, or V\_{IO} \leq V\_{DD} & V\_{IO}  $\geq$  2.2 V

\* Stabilize the service voltage so as not to cause the voltage change by the noise etc.

# **Operating Characteristics** at Ta = 25°C, $V_{CC}$ = 3.0V, $V_{DD}$ = 3.0V, Volume =15/16, Soft Mute = 1/Soft Stereo = off with the designated test circuit

Output level set with Radio Control 1 of control register map (0Dh Bit0, Bit1, Bit5 set to '1', '1')

Control 2 of control register map (0Dh Bit1 set to '1')

In addition, Set IF OSC = 170kHz, IF BW = 100% (Radio Control 1 : 0D Bit6, Bit7 set to '1', '1')

		,		Ratings		
Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I <sub>CC</sub> A	Analog block at 60dBµV EMF input		12	17	mA
(in operation)	ICCD	Digital block at 60 dBµV EMF input		0.3	0.8	mA
Current drain	ICCA	Analog standby mode		3	30	μA
(in standby)	ICCD	Digital standby mode		3	30	μA
FM receive band	F_range	Refer to PCB mounting conditions to cover the FM receive band of 76M to 108MHz	76		108	MHz
FM receive characteristics; MONO	: fc = 80MHz, fr	m = 1kHz, 22.5kHzdev. Note that Soft_mute = 1, S	Soft_stereo fur	nction OFF, IH	IF-BPF used	
3dB sensitivity	-3dB LS	60dBμV, 22.5kHzdev output standard, -3dB input.		5	17	dBµV EMF
Practical sensitivity 1	QS1	Input at S/N = 30dB De-emphasis = 75µs, SG open display		8	16	dBμ\ EMF
Practical sensitivity 2 (Reference)	QS2	Input at S/N = 26dB De-emphasis = 75µs, SG terminal display		1.10		μV
Demodulation output	Vo	60dBμV EMF, pin 19 output	80	110	160	mVrm
Channel balance	СВ	60dBµV EMF, pin 18 output/pin 19 output	-2	0	2	dB
Signal-to-noise ratio	S/N	60dBμV EMF, pin 19 output	48	58		dB
Total harmonic distortion 1 (MONO)	THD1	60dBμV EMF, pin 19 output, 22.5kHz dev.		0.4	1.5	%
Total harmonic distortion 2 (MONO)	THD2	60dBμV EMF, pin 19 output, 75.0kHz dev.		1.3	3	%
Field intensity display level	FS	Reg1Dh_bit0 = OFF Input level at which Reg02h_bit1-3 change from 1 to 2.	3	10	20	dBμV EMF
Mute attenuation	Mute-Att.	60dBμV EMF, pin 19 output	60	70		dB
FM receive characteristics ; STER	EO characterist	t <b>ics :</b> fc = 80MHz, fm = 1kHz, V <sub>IN</sub> = 60dBμV EMF	, Pilot = 10%	(7.5kHzdev), N	MPX-Filter us	sed
Separation	SEP	L-mod, pin 19 / pin 18 output L+R signals = 30% (22.5kHz dev.)	20	35		dB
Total harmonic distortion (Main)	THD-ST1	Main-mod (for L + R input), 19 output IHF BPF L+R signals = 30% (22.5kHzdev.)		0.6	1.8	%

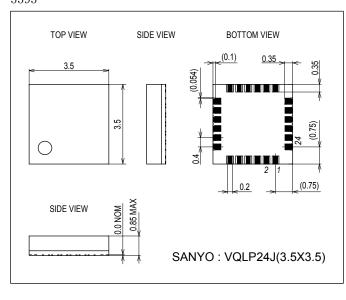
#### Interface block allowable operation range at Ta = -20 to $+70^{\circ}$ C, V<sub>SS</sub> = 0V

Devenuetor	Querra ha a l	Conditions		Ratings		Unit
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V <sub>DD</sub>		2.5		3.6	V
Digital block input	VIH	High-level input voltage range	0.7V <sub>DD</sub>		V <sub>DD</sub>	V
	VIL	Low-level input voltage range	0		0.1V <sub>DD</sub>	V
Digital block output	IOL	Output current at Low level	2.0			mA
	V <sub>OL</sub>	Output voltage at Low level I <sub>OL</sub> = 2mA			0.6	V
External clock operating frequency	fclk_ext	Clock frequency for external input	32k	32.768k	20M	Hz

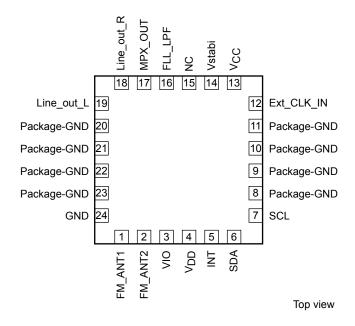
Note : External clock input (pin 12) allows also input of the sine wave signal.

## **Package Dimensions**

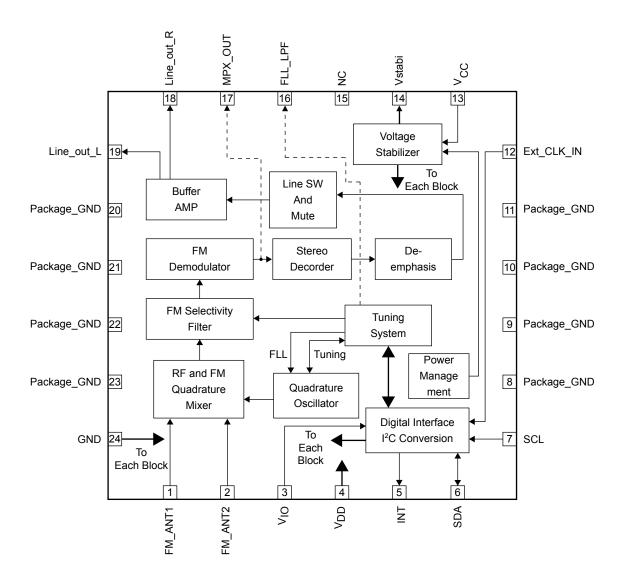
unit : mm (typ) 3393



## **Pin Assignment**



## **Block Diagram**



## **Pin Function**

Pin No.	Pin name	Description	Pin voltage	Internal equivalent circuit
1 2	FM-ANT1 FM-ANT2	Antenna input For pin 1 single input, pin 2 is set to AC_GND via capacity	1V	ANT2 ANT2
3	V <sub>I/O</sub>	Digital interface supply voltage Power pin dedicated to the interface input/output elements	V <sub>I/O</sub>	$V_{DD}$ $V_{I/O}$ $3$ to each interface block
4	V <sub>DD</sub>	Digital supply voltage Power pin for digital block	V <sub>DD</sub>	VDD (4)
5	INT	Interrupt line Output pin dedicated to interrupt (hardware output: used for options)		
6	SDA	Digital interface DATA ine Bidirectional data line. Pull up to Vio line with $3.3k\Omega$ to $10k\Omega$ resistor		C − − − − − − − − − − − − − − − − − − −
7	SCL	Digital interface Clock line		
8 9 10 11	Package-GND	GND for package-shield BND pin for package shield	(GND)	
12	Ext_CLK_IN	Reference clock-source input for measurement External standard CLK input pin.		

Continued on next page.

Pin No.	Pin name	Description	Pin voltage	Supplement
13	V <sub>CC</sub>	Analog supply voltage Power pin for analog (tuner) block	V <sub>CC</sub>	V <sub>CC</sub> 13 Bias Regulater 777
14	Vstabi	Stabilizer voltage Local oscillator reference bias pin. NC pin to be used	2.6V	Vcc Vstabi. line for each block Ustabi. line for each block Ucc Bias Regulater OSC block
15	. NC	Keep this open		
16	FLL_LPF	LPF for FLL LPF pin for noise decrease when FLL operates. Capacity(0.47µF to 1.0µF) is added this pin and between Vstabi pin of 14pin. NC pin to be used		
17	MPX_OUT	MPX-signal output Stereo decoder input monitor pin. NC pin to be used	2.3V	Vstabi 100Ω 17 WV 4 100Ω
18	LINE-OUT-R	Radio Rch Line-output Audio R_ch output	1.2V	Vstabi Vstabi
19	LINE-OUT-L	Radio Lch Line-output Audio L_ch output	1.2V	
20 21 22 23	Package-GND	GND for package-shield GND pin for package shield	(GND)	
24	GND	GND (Analog and Digital GND) GND pin for analog (FM tuner) block and digital (control) block	(GND)	

## Format of Bus Transfers

Bus transfers are primarily based on the I2C primitives

- Start condition
- Repeated start condition
- Stop condition
- Byte write
- Byte read

Start, restart, and stop conditions are specified as shown in Table 1 below.

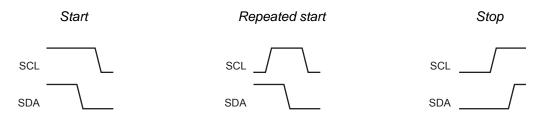


Fig. 1 the I<sup>2</sup>C start, repeated start and stop conditions.

For details, like timing, etc., refer to specifications of I<sup>2</sup>C.

8-bit write

8-bit data is sent from the master microcomputer to LV24250LS.

Data bit consists of MSB first and LSB last.

Data transmission is latched at the rising edge of SCL in synchronization with the SCL clock generated at the master IC. Do not change data while SCL remains HIGH.

LV24250LS outputs the ACK bit between eighth and ninth falling edges of SCL

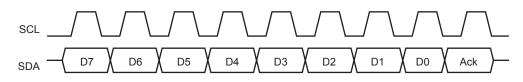


Fig. 2 Signal pattern of the I<sup>2</sup>C byte write

Read is of the same form as write, only except that the data direction is opposite. Eight data bits are sent from LV24250LS to the master while Ack is sent from the master to LV24250LS.

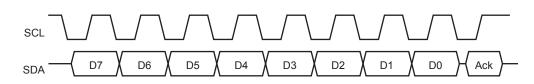


Fig. 3 Signal pattern of the I<sup>2</sup>C byte read

The serial clock SCL is supplied from the master side. It is essential that data bit is output from LV24250LS in synchronization with the falling edge while the master side performs latching at the rising edge.

#### LV24250LS latches ACK at the rising edge.

The sequence to write data D into the register A of LV24250LS is shown below.

- Start condition
- write the device address (C0h)
- write the register address, A
- write the target data, D
- stop condition

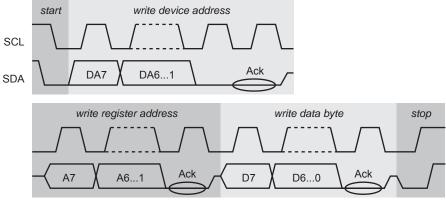


Fig. 4 Register write through I<sup>2</sup>C

When one or more data has been provided for writing, only the first data is allowed to be written.

#### Read sequence

- start condition
- write the device address (C0h)
- write the register address, A
- repeated start condition (or stop + start in a single master network)
- write the device address + 1 (C1h)
- read the register contents D, transmit NACK (no more data to be read)
- stop condition

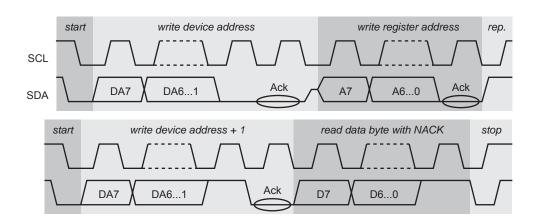


Fig. 5 Register read through I<sup>2</sup>C

## Interrupt Pin INT

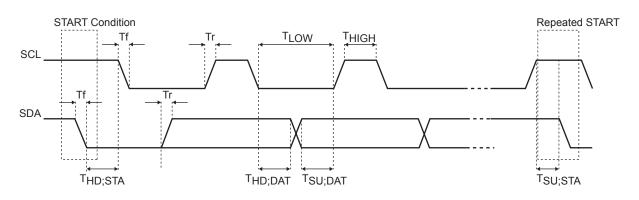
LV24250LS has the dedicated interrupt output pin. For the active level to the host, either LOW or HIGH can be selected. The INT output pin is kept floating while the PWRAD bit is cleared during initialization.

Therefore, to avoid influence on the CPU side during initialization, it is recommended to secure the non-active state by means of the pull-up or pull-down resistor.

This enables direct INT output connection to non-masking interruption of the host CPU.

## Digital interface specification (interface specification : reference)

(1). Characteristics of SDA and SCL bus line relative to the I<sup>2</sup>C bus interface



Deventer	0 stat	Standard	-mode	High_Spee	ed-mode	
Parameter	Symbol	min	max	min	max	unit
SCL clock frequency	F <sub>SCL</sub>	0	100	0	400	kHz
Fall time of both SDA and SCL	Tf		300	20+0.1Cb	300	ns
Rise time of both SDA and SCL	Tr		1000	20+0.1Cb	300	ns
High time of SCL	T <sub>HIGH</sub>	4.0		0.6		μS
Low time of SCL	TLOW	4.7		1.3		μS
Hold time of STAT condition	T <sub>HD</sub> ; STA	4.0		0.6		μS
Hold time of Data	T <sub>HD</sub> ; DAT	0	3.45	0	0.9	μS
Set-up time of STAT condition	T <sub>SU</sub> ; STA	4.7		0.6		μS
Set-up time of STOP condition	T <sub>SU</sub> ; sto	4.0		0.6		μS
Set-up time of Data	T <sub>SU</sub> ; DAT	250		100		ns
Bus free time between a STOP and	T <sub>BUF</sub>	4.7		1.3		μS
Capacitivie load for each bus line	Cb		400		400	pF

\*Cb = Total capacitance of one bus line

#### (2). Register map (On Register Map)

#### Following is Sub address map of LV24250LS. Each register becomes 8-bit constitution.

Address	Register Name	Mode	Remark
00h	CHIP_ID	R/W	Chip ID
02h	RADIO_STAT	R	Status of Radio Station
0Bh	RFCAP	R/W	RF Cap bank
0Dh	RADIO_CTRL1	R/W	Radio Control 1
0Eh	RADIO_CTRL2	R/W	Radio Control 2
0Fh	RADIO_CTRL3	R/W	Radio Control 3
10h	TNPL	R	Tune Position Low
11h	TNPH_STAT	R	Tune Position High and Status
19h	REF_CLK_PRS	R/W	Reference clock pre-scalar
1Ah	REF_CLK_DIV	R/W	Reference clock divider
1Bh	REF_CLK_OFF	R/W	Reference clock offset
1Dh	SCN_CTRL	R/W	Scan control
1Eh	TARGET_VAL_L	R/W	Target value Low
1Fh	TARGET_VAL_H	R/W	Target value High

R : Read only register R/W : Read and Write register

#### (3). Register description (ON Contents of each Register)

## Register 00h – CHIP\_ID – Chip identify register (Read/Write)

			ID [7	7 : 0]		
bit 7-0 :	<b>ID [7 : 0] :</b> 8 LV24250LS	3-bit chip ID. :15h				

#### Register 02h – RADIO\_STAT – Radio station status (Read-Only)

7	6	5	4	3	2	1	0
RAD_IF	N/A	N/A	MO_ST		FS [2 : 0]		SF5DB
bit 7 :	RAD_IF : R	adio interrupt flag.					
	0 = no ini	terrupt					
	1 = interr	upt					
	Note :						
When status (fi	eld strength, stereo	/mono) changes, thi	s bit is set.				
If Interrupt of IF	RQ pin is enabled, Ir	nterrupt pin is set by	following IPOL reg	ister condition.			
This bit is clear	ed by register read.	In stand-by mode (	PW_RAD = 0), this	bit is 1			
bit 6-5 :	NA [1 : 0] :	NA 0 fixed					
bit 4 :	<b>MO_ST</b> : M	ono/stereo indicato	r				
	0 = Force	ed monaural					
	1 = Norm	nal (Receiving in ste	reo mode)				
bit 3-1	FS [2 : 0] :	Fieldstrength :					
	0 = Low 1	field strength					
	7 = High	field strength					
bit 0 :		eldstrength +5dB :					
	0 = FS5d						
	1 = FS5d	IR Ob					
For details, refer	to Application note.						

#### Register 0Bh – RFCAP – RF Cap bank (Read/Write)

7	6	5	4	3	2	1	0
			RFCA	P [7 : 0]			
bit 7-0 :	RFCAP [7 :	0]: RF Oscillator (	CAP bank				

$\begin{array}{llllllllllllllllllllllllllllllllllll$	VOL [1 : 0]
bit 6 : <b>IFBWSEL</b> : IF band width setting 0 = 50% 1 = 100% bit 5 : <b>VOL_2</b> : Volume setting For details, refer to Bit0,1 for RADIO_CTRL1 bit 4 : <b>DEEM</b> : de-emphasis $0 = 50\mu s$ : Korea, China, Europe, Japan $1 = 75\mu s$ : USA bit 3 : <b>ST_M</b> : Stereo/mono setting 0 = Stereo enabled 1 = Stereo disabled (mono mode)	
$1 = 170 \text{kHz}$ bit 6 :IFBWSEL : IF band width setting $0 = 50\%$ $1 = 100\%$ bit 5 :VOL_2 : Volume setting For details, refer to Bit0,1 for RADIO_CTRL1bit 4 :DEEM : de-emphasis $0 = 50\mu s$ : Korea, China, Europe, Japan $1 = 75\mu s$ : USAbit 3 :ST_M : Stereo/mono setting $0 = Stereo enabled1 = Stereo disabled (mono mode)$	
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1 = 100%bit 5 : $VOL_2$ : Volume setting For details, refer to Bit0,1 for RADIO_CTRL1bit 4 : $DEEM$ : de-emphasis $0 = 50\mu s$ : Korea, China, Europe, Japan $1 = 75\mu s$ : USAbit 3 : $ST_M$ : Stereo/mono setting $0 =$ Stereo enabled $1 =$ Stereo disabled (mono mode)	
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bit 4 : DEEM : de-emphasis $0 = 50\mu s : Korea, China, Europe, Japan$ $1 = 75\mu s : USA$ bit 3 : $ST_M : Stereo/mono setting$ 0 = Stereo enabled 1 = Stereo disabled (mono mode)	
0 = 50μs : Korea, China, Europe, Japan 1 = 75μs : USA bit 3 : ST_M : Stereo/mono setting 0 = Stereo enabled 1 = Stereo disabled (mono mode)	
<pre>1 = 75μs : USA bit 3 : ST_M : Stereo/mono setting 0 = Stereo enabled 1 = Stereo disabled (mono mode)</pre>	
bit 3 : ST_M : Stereo/mono setting 0 = Stereo enabled 1 = Stereo disabled (mono mode)	
0 = Stereo enabled 1 = Stereo disabled (mono mode)	
1 = Stereo disabled (mono mode)	
bit 2 : nMUTE : Audio Mute	
bit 2. INFOTE Additionate	
0 = Mute On	
1 = Mute Off	
bit 1-0 : VOL [1 : 0] : Volume Setting * It controls by Bit5 of RADIO_CTRL1 and combination 4Bit with Bit1 of RADIO_CTRL2.	
Vol_3 Vol_2 Vol_1 Vol_0	
$\begin{array}{ccccc} 0 & 0 & 0 \\ 0 & 0 & 0 \end{array} $ Minimum level $\begin{array}{cccc} 0 & 0 & 0 \end{array}$	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	
 1 1 1 1 1: Max level	

## Register 0Eh – RADIO\_CTRL2 – Radio control 2 (Read/Write)

7	6	5	4	3	2	1	0		
	SOFTST [2 : 0]			SOFTMU [2 : 0]	•	N/A	STABI_BP		
bit 7-5 :	SOFTST [2 : 0] : Soft Stereo setting								
	000b = Sc	ft stereo level 3							
	001b = Dis	sable soft stereo							
	010b = So	ft stereo level 1 (*)							
	100b = So	ft stereo level 2							
	Note : do	not use without the	se value.						
	(*) : recom	mended setting							
bit 4-2 :	SOFTMU [2								
	000b = Sc								
	001b = Disable soft audio mute								
	010b = So	ft audio mute level	1						
	100b = So	ft audio mute level	2 (*)						
	Note : do	not use without the	se value.						
	(*) : recom	mended setting							
bit 1 :	VOL_3 : Volu	ume setting							
	For details	s, refer to Bit0,1 for	RADIO_CTRL1	I					
bit 0 :	STABI_BP :	Internal regulator b	y-pass bit						
	0 = Interna	al regulator operate	(normal)						
	1 = Interna	al regulator by-pass							

7	6	5	4	3	2	1	0			
IPOL	SM_IE	RAD_IE	SD_PM	nIF_PM	EXT_CLK	CFG [1:0]	PW_RAD			
bit 7 :	IPOL : Inter	rupt (IRQ) Polarity	L	1 I			•			
	0 = IRQ a	active high								
	1 = IRQ a	active low								
bit 6 :		mmand end interru	pt							
	0 = Disab									
	1 = Enab	le								
bit 5 :	RAD_IE : R	adio Interrupt (field	strength/stereo ch	anges)						
	0 = Disab	ble								
	1 = Enab	le								
bit 4 :	SD_PM : Stereo decoder clock PLL mute									
	0 = SD PLL On (Normal Operation)									
	1 = SD PLL Off (Adjustment)									
bit 3 :	nIF_PM:IF	PLL mute								
	0 = IF PLL Off (Adjustment)									
	1 = IF PL	L On (Normal Oper	ation)							
bit 2-1 :	EXT_CLK_	CFG [1:0]: Exterr	nal Clock Setting							
	EXT_CLK_CFG	6 [1 : 0]	Reference clock							
	00		Off							
	01		NA:Do not use							
	10		Oscillator clock so	urce / 32						
		(for high frequency source)								
	11									
			(for low frequency	source)						
bit 0 :	PW_RAD :	Radio Circuit Powe	r							
	_	er Off (Stand-by).								
	1 = Powe	er On								
No	te : At the time of start	. PW RAD become	es 0 (Stand-by)							

## Register 10h – TNPL – Tune position low (Read-Only)

7	6         5         4         3         2         1         0									
	TUNEPOS [7 : 0]									
bit 7-0 :	bit 7-0 : TUNEPOS [7 : 0] : Current RF Frequency (Low 8bit)									

7	6	5	4	3	2	1	0	
	ERROR [2 : 0]		SM_IF	TUNED	NA	TUNEP	OS [9 : 8]	
bit 7-5 :	ERROR [2	: 0] : Error Code	·					
	ERROR [2 :	0]	Remark					
	0		OK, Command	l end (No Error)				
	1		Default value	after or during reset				
	2		Band Limit Err	or				
	3		DAC Limit Erro	or				
	6		Command for	ed End				
	7		Command bus	Command busy				
	0 = No In 1 = Interr	•	rupt nag					
This bit is set w		terrupt rupt		wed, the pin status is	changed, Reading	this register caus	es clearing.	
This bit is set w bit 3 :	1 = Interr hen the command is o	terrupt rupt		wed, the pin status is	s changed, Reading	this register cause	es clearing.	
	1 = Interr hen the command is o	terrupt upt over. When the IR adio tuning Flag		wed, the pin status is	s changed, Reading	this register cause	es clearing.	
	1 = Interr hen the command is o <b>TUNED</b> : R 0 = No tu 1 = Tune	iterrupt upt over. When the IR adio tuning Flag ine d	Q pin interrupt is allo		changed, Reading	this register caus	es clearing.	
	1 = Interr hen the command is o <b>TUNED</b> : R 0 = No tu 1 = Tune <b>Note</b> : This	terrupt upt over. When the IR adio tuning Flag ine d flag is set when T	Q pin interrupt is allo		changed, Reading	this register caus	es clearing.	
	1 = Interr hen the command is o <b>TUNED</b> : R 0 = No tu 1 = Tune <b>Note</b> : This This flag is o	terrupt upt over. When the IR adio tuning Flag ine d flag is set when T cleared under 3 c	Q pin interrupt is allo		changed, Reading	this register cause	es clearing.	
	1 = Interr hen the command is o <b>TUNED</b> : R 0 = No tu 1 = Tune <b>Note</b> : This This flag is (1) PW_RA	terrupt upt adio tuning Flag ine d flag is set when <sup>–</sup> cleared under 3 c D = 0	Q pin interrupt is allo		changed, Reading	this register caus	es clearing.	
	1 = Interr hen the command is o <b>TUNED</b> : R 0 = No tu 1 = Tune <b>Note</b> : This This flag is (1) PW_RA (2) Tuning F	terrupt upt adio tuning Flag ine d flag is set when <sup>–</sup> cleared under 3 c D = 0	Q pin interrupt is allo		changed, Reading	this register caus	es clearing.	
	1 = Interr hen the command is o <b>TUNED</b> : R 0 = No tu 1 = Tune <b>Note</b> : This This flag is (1) PW_RA (2) Tuning F	Iterrupt upt over. When the IR adio tuning Flag ine d flag is set when T cleared under 3 c D = 0 Frequency on searching	Q pin interrupt is allo		changed, Reading	this register caus	es clearing.	

## Register 19h – REF\_CLK\_PRS – Reference clock prescaler (Read/Write)

-					-					
7	6	5	4 3 2 1 0							
	REFPRE [2 : 0]	RE [2 : 0] REFMOD [4 : 0]								
bit [7 : 5] : REFPRE [2 : 0] : Reference Clock pre- scaler										
0 = 1 : 1										
	1 = 1 : 2									
	7 = 1:128									
bit [4 : 0] :	bit [4 : 0] : REFMOD [4 : 0] : 5-bit slope correction									

#### Register 1Ah – REF\_CLK\_DIV – Reference clock divider (Read/Write)

7	6	5	4	3	2	1	0			
REFDIV [7 : 0]										
Bit 7-0 :	0 : Divide 1 : Divide 	: <b>0]</b> : Reference Clo er Value = 1 er Value = 2 rider Value = 256	ock Divider							

## Register 1Bh –REF\_CLK\_OFF – Reference clock offset (Read/Write)

7	6	5	4	3	2	1	0
			REFOF	FS [7 : 0]			
Bit 7-0 :	REFOFFS	7:0]: Offset regist	ter for the spread of	f reference clock			

7	6	5	4	3	2	1	0
GRID	0 [1 : 0]	FLL_ON	FLL_MODE		FS [2 : 0]		SHF5DB
bit 7-6 :	GRID [1 : 0	] : FM station sear	ch frequency interval	:			1
	0 = IFSD	set					
	1 = 50kH	Iz grid					
	2 = 100k	Hz grid					
	3 = 200k	Hz grid					
bit 5 :	FLL_ON : F	LL Control					
	0 = FLL 0	OFF					
	1 = FLL (	ON					
	During se	etting of the FM fre	quency and during s	eek, keep this OF	F. Turn it ON after tur	ling.	
bit 4 :	Reserved : However,		ity is added to 16pin, a	und it uses it as Smoo	othing Filter(FLL_LPF	).	
bit 3-1 :		Field strength setting setting of IFSD.	ng at the time of FM	station search and	l a frequency adjustm	nent bit	
bit 0 :	SHF5DB : S	Scan stop level +5c	IB				

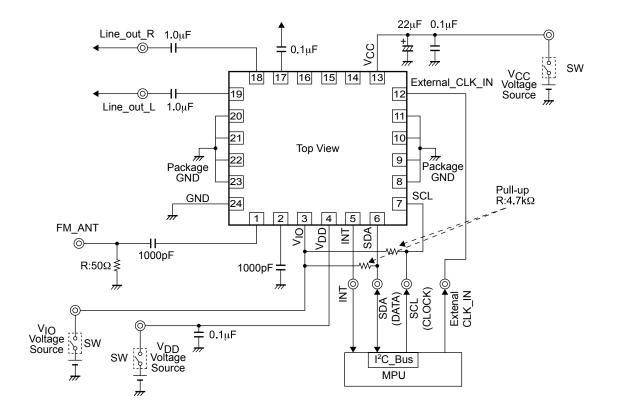
## Register1Eh – TARGET\_VAL\_L – Target Value Low Register (Read/Write)

7	<sup>'</sup> 6 5 4 3 2 1 0								
			TARGE	T [7 : 0]					
bit 7-0 :	TARGET [7	: 0] : Target freque	ncy low 8 bit :						
	Tuning frequency or Limit Frequency for FM Station Search								

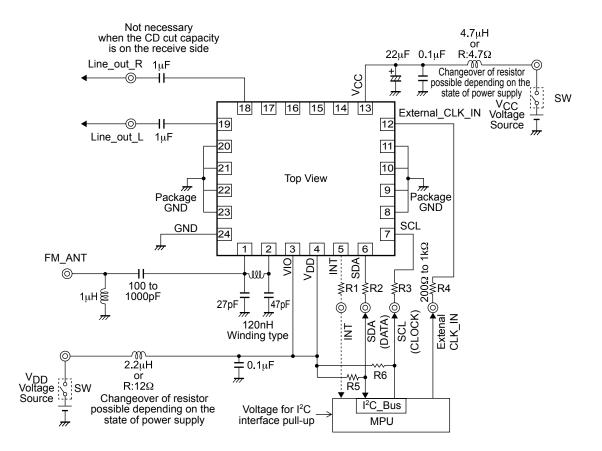
## Register 1Fh – TARGET\_VAL\_H – Target Value High Register (Read/Write)

7	6	5	4	3	2	1	0			
TARGET [15 : 8]										
bit 7-0 :	- Target v		libration, Tuning fre	quency value or lim has different definiti	, ,	or station search				
With radio power executed.	ON, lower eight bits	s of the target freque	ency are set. Then,	set higher eight bit	s of the target freque	ency to this register.	. The command is			

## **Test Circuit**



## **Application Circuit**

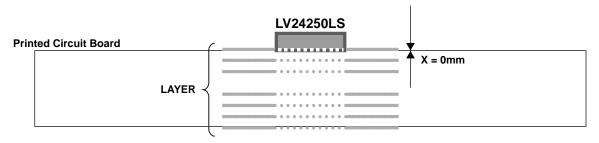


#### Cautions for mounting of IC

- Note1 : For external part constant, the recommended value is described. Since the constant may differ during actual use with the set mounted, be sure to consider optimization.
- Note2 : The single input antenna application has been described. The difference input is also possible (The signal input from 1pin and 2pin: Refer to the application note for details).
- Note3 : If the spike noise between MPU and IC is large during communication, it is recommended to add limiting resistors R1, R2, and R3 between MPU and IC. 0Ω at 1.8V.
- Note4 : To reduce noise from power supply, add a capacitor between V<sub>CC</sub> GND and between V<sub>DD</sub> GND.
- Note5 : The I<sup>2</sup>C bus communication line requires pull-up resistors R5 and R6. The commonly-employed resistance value is 4.7k (4.7k to 10k). Set the pull-up voltage to the same one of V<sub>IO</sub> of LV24250LS. (Supply from the same source as V<sub>IO</sub> and V<sub>DD</sub> is recommended.
- Note6 : Please use the INT pin arbitrarily. Recommended to open when unused. The INT pin becomes unstable at IC startup. To protect MPU from any effects during startup, it is recommended to add either the pull-up or pull-down resistor to set the non-active mode. (This is not necessary when the MPU can be set to non-active by a software during initialization.

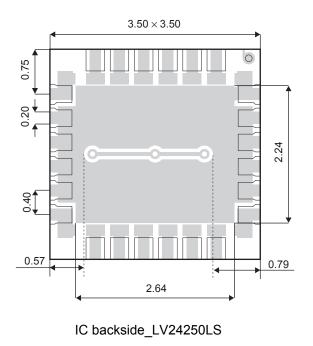
#### PCB Mounting Conditions to cover the FM Receiving Area of 76M to 108MHz

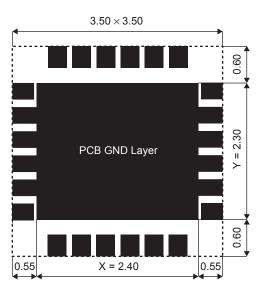
LV24250LS's PCB mounting conditions



• LV24250LS has an inductor for local oscillator on the package bottom side. In order to cover the receiving frequency range of 76MHz to 108MHz, provide the GND layer to the first layer of Side A of PCB that is directly below the package bottom side, as shown in the figure.

#### **Recommended layout of PCB substrate**





IC directly-below\_PCB recommended GND patten diagram

- With this SPL, the receiving frequency is measured under the following conditions :
- The X-value can be set freely between Min = 2.00mm and Max = 2.60mm with reference to IC. (The X-value for Sanyo Demo Board is 2.4mm.)
- The Y-value can be set freely between Min = 1.00mm and Max = 2.40mm with reference to IC. (The Y-value for Sanyo Demo Board is 2.30mm.)
- Avoid providing another wiring within 0.4mm of bottom layer of PCB\_GND as much as possible.

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