

SANYO Semiconductors DATA SHEET

CMOSIC

LV51141T — 1-Cell Lithium-Ion Battery Protection IC

Overview

The LV51141T is protection IC for rechargeable Li-ion battery by high withstand voltage CMOS process. The LV51141T protect single-cell Li-ion battery from over-charge, over-discharge, charge over-current and discharge over-current.

Features

• High accuracy detection voltage Over-charge detection ±25mV

Over-charge hysteresis $\pm 25 \text{mV}$ Over-discharge detection $\pm 25\%$ Charge over-current detection $\pm 0.3 \text{V}$ Discharge over-current detection $\pm 20 \text{mV}$

• Delay time (internal adjustment)

• Low current consumption Operation Typ. $3.0\mu A$

Over-discharge condition Max. 0.1µA

• 0V cell battery charging function

Specifications

Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		V _{SS} -0.3 to V _{SS} +7	V
Input voltage of V _M	V _M		V _{DD} -28 to V _{DD} +0.3	V
Output voltage of CO	VCO		V _M -0.3 to V _{DD} +0.3	V
Output voltage of DO	VDO		V _{SS} -0.3 to V _{DD} +0.3	V
Power dissipation	PD		350	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

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Electrical Characteristics at Topr = 25°C, unless otherwise specified

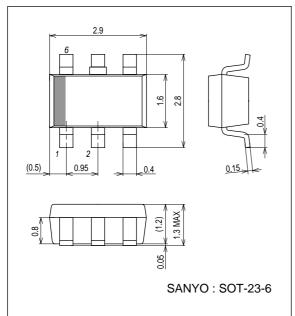
			Test	Ratings			
Parameter	Symbol	Conditions	circuit	min	typ	max	Unit
Detection voltage			I	I			ı
Over-charge detection voltage	VC		1	4.225	4.250	4.275	V
Over-charge hysteresis voltage	VHc		1	0.175	0.2	0.225	V
Over-discharge detection voltage	Vdc		1	2.925	3.000	3.075	V
Over-discharge reset voltage	VRdc		1	3.120	3.200	3.280	V
Charge over-current detection voltage	VIc		2	-1.000	-0.700	-0.400	V
Discharge over-current detection voltage	Vldc		2	0.100	0.120	0.140	V
Load short-circuiting detection voltage	Vshort	Based on V _{DD} , V _{DD} = 3.5V	2	-1.7	-1.3	-1.0	V
Input voltage			I	I			ı
Input voltage between V _{DD} and V _{SS}	V _{DD}	Internal circuit operating voltage	-	1.8		7.0	V
0V battery charge starting charger voltage	Vcha	Acceptable	3		0.9	1.4	V
Current consumption	I		l.	I.			ı
Current consumption on operation	lopr	$V_{DD} = 3.5V, V_{M} = 0V$	4		3.0	6.0	μА
Current consumption on shutdown	Isdn	V _{DD} = V _M = 1.8V	4			0.1	μА
Output resistance							
C _O : Pch ON resistance	Rcop	$C_O = 3.0V, V_{DD} = 3.5V,$	5	1.5	3.0	4.5	kΩ
		V _M = 0V					
C _O : Nch ON resistance	Rcon	$C_O = 0.5V, V_{DD} = 4.6V,$ $V_M = 0V$	5	0.5	1.0	1.5	kΩ
DO : Pch ON resistance	Rdop	$D_O = 3.0V, V_{DD} = 3.5V,$ $V_M = 0V$	5	1.7	3.5	5.0	kΩ
D _O : Nch ON resistance	Rdon	$D_O = 0.5V, V_{DD} = V_M = 1.8V$	5	1.7	3.5	5.0	kΩ
Discharge over-current release resistance	Rdwn	V _{DD} = 3.5V, V _M = 1.0V	5	15.0	30.0	60.0	kΩ
Detection delay time			I	I			ı
Over-charge detection delay time	tc	$V_{DD} = VC-0.2V \rightarrow VC+0.2V,$ $V_{M} = 0V$	6	0.70	1.0	1.30	S
Over-discharge detection delay time	tdc	$V_{DD} = Vdc+0.2V \rightarrow Vdc-0.2V,$ $V_{M} = 0V$	6	21.7	31.0	40.3	ms
Charge over-current detection delay time	tic	$V_{DD} = 3.5V, V_{M} = 0V \rightarrow -1.0V$	6	5.6	8.0	10.4	ms
Discharge over-current detection delay time	tidc	$V_{DD} = 3.5V, V_{M} = 0V \rightarrow 1.0V$	6	5.6	8.0	10.4	ms
Load short-circuiting detection delay time	tshort	$V_{DD} = 3.5V, V_{M} = 0V \rightarrow 3.5V$	6	190	370	550	μS
Release delay time							
Release delay time 1 Over-discharge release Charge over-current release (*1) Discharge over-current release Load short-circuiting release	trel1		6	1.0	2.0	3.0	ms
Release delay time 2 Over-charge release	trel2	$V_{DD} = VC+0.2V \rightarrow VC-0.2V,$ $V_{M} = 1.0V$	6	8.0	16.0	24.0	ms

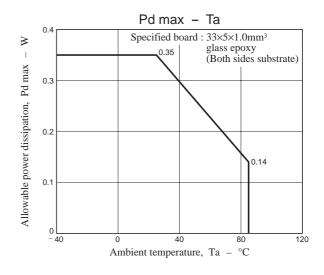
 $Note: {}^\star 1 \ Upon \ connecting \ to \ charger \ upon \ over-discharge, \ the \ delay \ time \ after \ recovery \ from \ over-discharge.$

Package Dimensions

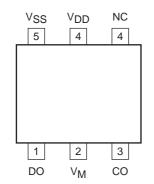
unit: mm (typ)

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Pin Assignment

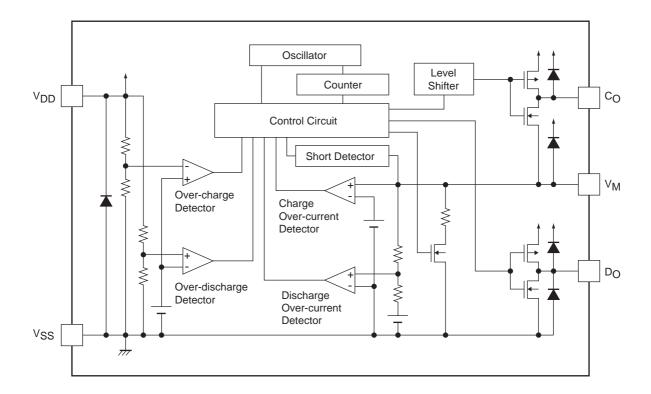


Top view

Pin Function

Pin No.	Pin Name	Description
1	DO	FET gate connection for discharge control (CMOS output)
2	VΜ	Voltage monitoring for charger negative
3	CO	FET gate connection for charge control (CMOS output)
4	NC	N/C
5	V_{DD}	Positive power input
6	V _{SS}	Negative power input

Block Diagram



Measurement Conditions

- Over-charge detection voltage, Over-charge hysteresis voltage --- [Circuit 1] Set V1 = 3.5V and V2 = 0V. Over-charge detection voltage VC is V1 at which VCO goes "Low" from "High" when V1 is gradually increased from 3.5V. Then IC is released from the over-charge state and VCO goes "High" from "Low" at the voltage "Measured VC-VHc" when V1 is gradually decreased. If V2 is set to the greater value than discharge over-current detection voltage VIdc in the over-charge state, VHc is canceled and then IC is released from the over-charge state at VC.
- Over-discharge detection voltage --- [Circuit 1] Set V1 = 3.5V and V2 = 0V. Over-discharge detection voltage Vdc is V1 at which VDO goes "Low" from "High" when V1 is gradually decreased from 3.5V. Next, set V2 under to charge over-current detection voltage Vlc. Then IC is released from the over-discharge state at Vdc and VDO goes "High" from "Low".
- Charge over-current detection voltage --- [Circuit 2] Set V1 = 3.5V and V2 = 0V. Charge over-current detection voltage VIc is V2 at which VCO goes "Low" from "High" when V2 is gradually decreased from 0V.
- Discharge over-current detection voltage --- [Circuit 2] Set V1 = 3.5V and V2 = 0V. Discharge over-current detection voltage VIdc is V2 at which VDO goes "Low" from "High" when V2 is gradually increased from 0V.
- Load short-circuiting detection voltage --- [Circuit 2] Set V1 = 3.5V and V2 = 0V. Load short-circuiting detection voltage Vshort is V2 at which VDO goes "Low" from "High" within a time between the minimum and the maximum value of load short-circuiting detection delay time tshort, when V2 is increased rapidly within 10µs.
- 0V battery charge starting charger voltage --- [Circuit 3] Set V1 = V2 = 0V and decrease V2 gradually. 0V battery charge starting charger voltage Vcha is V2 when VCO goes "High" (V1-0.1V or higher).

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• Current consumption on operation and shutdown --- [Circuit 4]

Set V1 = 3.5V and V2 = 0V on normal condition. IDD shows current consumption on operation Iopr.

Set V1 = V2 = 1.8V on over-discharge condition. IDD shows current consumption on shutdown Isdn.

• Co : Pch ON resistance, Co : Nch ON resistance --- [Circuit 5]

Set V1 = 3.5V, V2 = 0V and V3 = 3.0V. (V1-V3)/|ICo| is Pch ON resistance Rcop.

Set V1 = 4.6V, V2 = 0V and V3 = 0.5V. V3/|ICo| is Nch ON resistance Rcon.

• Do : Pch ON resistance, Do : Nch ON resistance --- [Circuit 5]

Set V1 = 3.5V, V2 = 0V and V4 = 3.0V. (V1-V4)/|IDo| is Pch ON resistance Rdop.

Set V1 = V2 = 1.8V and V4 = 0.5V. V4/|IDo| is Nch ON resistance Rdon.

• Discharge over-current release resistance --- [Circuit 5]

Set V1 = 3.5V, V2 = 0V at first. And then, set V2 = 1.0V. $V2/|IV_{M}|$ is discharge over-current release resistance Rdwn.

• Over-charge detection delay time, Release delay time 2 --- [Circuit 6]

Set V2 = 0V. Increase V1 from the voltage VC-0.2V to VC+0.2V rapidly within 10 μ s. Over-charge detection delay time tc is the time needed for VCO to go "Low" just after the change of V1.

Next, set V2 = 1V and decrease V1 from VC+0.2V to VC-0.2V rapidly within 10μ s. Over-charge release delay time trel 2 is the time needed for VCO to go "High" just after the change of V1.

• Over-discharge detection delay time, Release delay time 1 --- [Circuit 6]

Set V2 = 0V. Decrease V1 from the voltage Vdc+0.2V to Vdc-0.2V rapidly within 10 μ s. Over-discharge detection delay time tdc is the time needed for VDO to go "Low" just after the change of V1.

Next, set V2 = -1V and increase V1 from Vdc-0.2V to Vdc+0.2V rapidly within 10 μ s. Release delay time 1 trel1 in case of over-discharge is the time needed for VDO to go "High" just after the change of V1.

• Charge over-current detection delay time, Release delay time 1 --- [Circuit 6]

Set V1 = 3.5V and V2 = 0V. Decrease V2 from 0V to -1V rapidly within $10\mu s$. Charge over-current delay time tic is the time needed for VCO to go "Low" just after the change of V2.

Next, increase V2 from -1V to 0V rapidly within 10µs. Release delay time 1 trel1 in case of charge over-current is the time needed for VCO to go "High" just after the change of V2.

• Discharge over-current detection delay time, Release delay time 1 --- [Circuit 6]

Set V1 = 3.5V and V2 = 0V. Increase V2 from 0V to 1V rapidly within $10\mu s$. Discharge over-current delay time tide is the time needed for VDO to go "Low" just after the change of V2.

Next, decrease V2 from 1V to 0V rapidly within 10µs. Release delay time 1 trel1 in case of discharge over-current is the time needed for VDO to go "High" just after the change of V2.

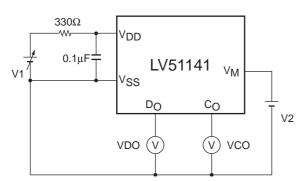
• Load short-circuiting detection delay time, Release delay time 1 --- [Circuit 6]

Set V1 = 3.5V and V2 = 0V. Increase V2 from 0V to 3.5V rapidly within 10 μ s. Load short-circuiting detection delay time tshort is the time needed for VDO to go "Low" just after the change of V2.

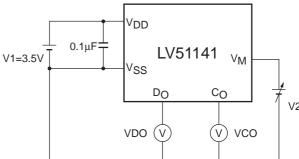
Next, decrease V2 from 3.5V to 0V rapidly within 10μs. Release delay time 1 trel1 in case of load short-circuiting is the time needed for VDO to go "High" just after the change of V2.

Measurement Circuits

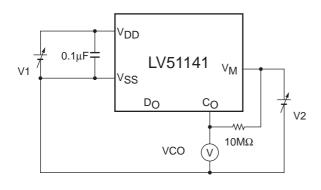
• Circuit 1



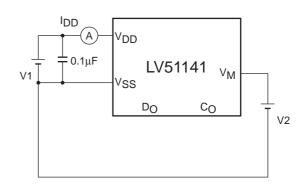
• Circuit 2



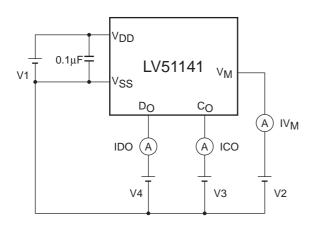
• Circuit 3



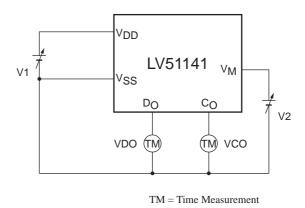
• Circuit 4



• Circuit 5

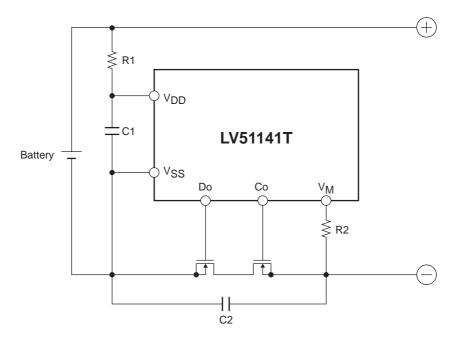


• Circuit 6



No.A1025-6/13

Application Circuit Example



External Components

Items	Symbol	Recommended value
Resistor 1	R1	330Ω
Capacitor 1	C1, 2	0.1μF
Resistor 2	R2	3.9kΩ

- The supply voltage (V_{DD}) to this IC is stabilized by R1 and C1. Moreover, R1 and R2 act as the current restriction resistances at the time of reverse-connecting a charger, or at the time of connecting a charger which outputs the voltage exceeding the absolute maximum rating of this IC. Be sure to connect these components.
- If the value of R1 is too large, the over-charge detection voltage will become high due to the current consumption of this IC. 330Ω is recommended.
- If the value of C1 is too small, this IC may be in a shutdown state at the time of the discharge over-current or the load short-circuiting. $0.1\mu F$ is recommended.
- Use the value within the limits shown in the table about the value of R2. In order to reduce the current at the time of reverse-connecting a charger, we recommend to choose R1 and R2 so that the sum total of resistance values is more than $4k\Omega$. The recommended value of R2 is $3.9k\Omega$.
- Note 1: The connection diagram and each value of external components shown above are just recommendation. Including a battery and FETs, determine the circuit after sufficient evaluation about your actual application.
- Note 2: The IC is susceptible to static electricity and some pins are easily damaged by it. Handle the IC carefully.

Description of Operation

• Normal condition

This IC monitors the battery voltage (V_{DD}) and the voltage of V_{M} terminal, and controls charge and discharge. If the battery voltage (V_{DD}) is in the range from the over-discharge detection voltage (V_{CD}) and the V_{M} terminal voltage is in the range from the charge over-current detection voltage (V_{CD}) to the discharge over-current detection voltage (V_{CD}) , this IC turns on both the charge and discharge control FETs. This state is called the normal condition, and charge and discharge are possible together.

• Discharge over-current detection, Load short-circuiting detection

When the discharge current becomes equal to or higher than the specified value under the normal condition, and if the V_M terminal voltage is in the range from the discharge over current detection voltage (VIdc) to the short-circuiting detection voltage (Vshort) and that state is maintained during more than the discharge over-current detection delay time (tidc), this IC turns off the discharge control FET to stop discharge. This state is called the discharge over-current condition.

At that time, if the V_M terminal voltage is equal to or higher than Vshort and that state is maintained during more than the load short-circuiting detection delay time (tshort), this IC turns off the discharge control FET to stop discharge. This state is called the load short-circuiting detection condition.

While load is connected, in both conditions, the V_M terminal voltage equals to V_{DD} potential due to the load, but it falls by the discharge over-current release resistance (Rdwn) when the load is removed and the resistance between (+) and (-) terminals of battery pack (refer to "Application Circuit Example") becomes larger than the value which enables the automatic return.

Then the V_M terminal voltage becomes less than VIdc, and if that state is maintained during more than the release delay time 1 (trel1), this IC returns to normal condition.

Note: The resistance value between (+) and (-) terminals of battery pack for automatic return changes with battery voltage (V_{DD}) or VIdc. The standard is expressed with the following equation.

Resistance value for automatic return = Rdwn \times (V_{DD} / VIdc - 1)

• Charge over-current detection

When the charge current becomes equal to or higher than the specified value under the normal condition, if the $V_{\rm M}$ terminal voltage becomes less than the charge over-current detection voltage (VIc) and that state is maintained during more than the charge over-current detection delay time (tic), this IC turns off the charge control FET to stop charge. This state is called the charge over-current detection condition.

Then the V_M terminal voltage becomes equals to or higher than VIc and that state is maintained during more than the release delay time 1 (trel1) when the charger is removed and the load is connected, this IC returns to the normal condition.

Note: If the V_M terminal voltage becomes equal to or less than V_{SS} -7V (typical), the charge over-current detection delay time (tic) changes as below.

8ms model \rightarrow 8ms (not changed) 125ms model \rightarrow 7ms (typical) 1.0s model \rightarrow 56ms (typical)

• Over-charge detection

When the battery voltage (V_{DD}) under the normal condition becomes equal to or higher than the over-charge detection voltage (VC) and that state is maintained during more than the over-charge detection delay time (tc), this IC turns off the charge control FET and stops charge. This state is called the over-charge detection condition. Release from the over-charge detection condition includes following three cases.

- (1) When V_{DD} falls to Vc-VHc without load and that state is maintained during more than the delay time 2 (trel2), this IC turns on the charge control FET and returns to the normal condition.
 - * VHc : Over-charge hysteresis voltage
- (2) When the load is installed and discharge starts, the discharge current flows through the internal parasitic diode of the charge control FET. Then the V_M terminal voltage rises to only the Vf voltage of the internal parasitic diode from V_{SS} potential. At this time, if the V_M terminal voltage is higher than the discharge over-current detection voltage (VIdc) and V_{DD} is equal to or less than VC, this IC returns to the normal condition when this state continues more than the delay time 2 (trel2).
- (3) In case (2), if the V_M terminal voltage is higher than the discharge over-current detection voltage (VIdc) and V_{DD} is equal to or higher than VC, battery is discharged until V_{DD} becomes less than VC, and then this IC returns to the normal condition when this state continues more than the delay time 2 (trel2).

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• Over-discharge detection

When the battery voltage (V_{DD}) under the normal condition becomes equal to or less than the over-discharge detection voltage (Vdc) and that state continues for more than the over-discharge detection time (tdc), this IC turns off the discharge control FET and stops discharging. This state is called the over-discharge detection condition. Recovery from the over-discharge detection condition is achieved only by connecting the charger.

• Return from over-discharge

When the charger is connected and charging starts, the charge current flows through the internal parasitic diode of the discharge control FET. If the V_M terminal voltage is higher than the charge over-current detection voltage (VIc), the IC returns to the normal condition when V_{DD} becomes equal to or higher than VRdc and this state continues more than the delay time1 (trel1).

If the V_M terminal voltage is lower than the charge over-current detection voltage (VIc), same as the above-mentioned case, the IC returns to the normal condition when V_{DD} becomes equal to or higher than Vdc and this state continues more than the delay time1 (trel1).

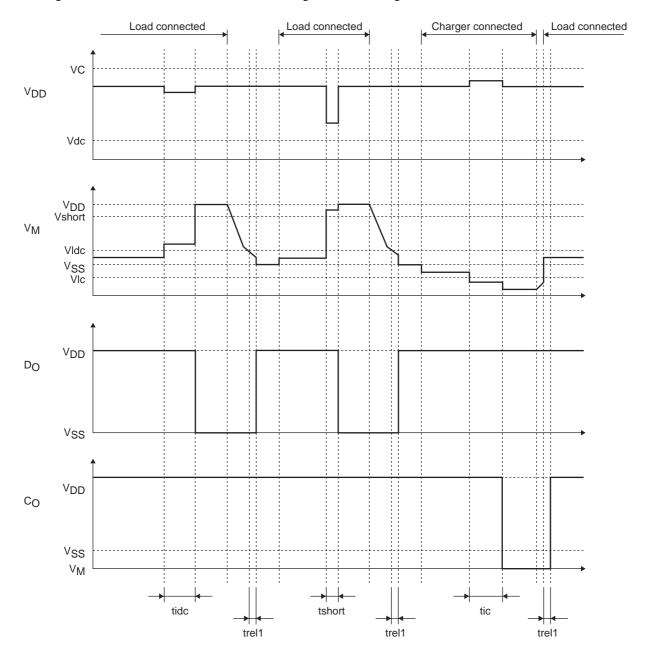
This IC stops all internal circuits (Shutdown condition) after detecting the over-discharge and reduces current consumption. (Max $0.1\mu A$, at $V_{DD} = 1.8V$)

• 0V battery charge function

If the voltage of charger (the voltage between V_{DD} and V_{M}) is larger than the 0V battery charge starting charger voltage (Vcha), 0V battery charge becomes possible when CO terminal outputs V_{DD} terminal potential and turns on the charge control FET.

Timing Chart

• Discharge over-current detection, Load short-circuiting detection, Charge over-current detection



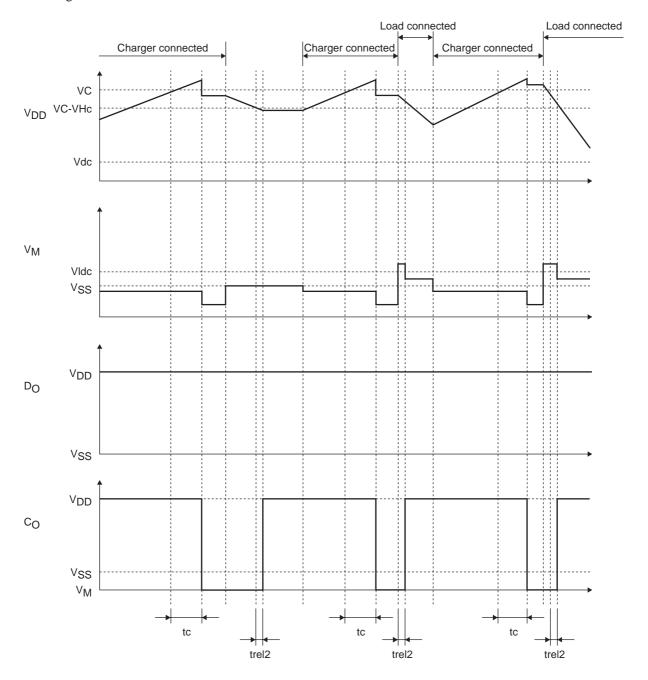
VC : Over-charge detection voltage
 Vdc : Over-discharge detection voltage
 VIc : Charge over-current detection voltage
 VIdc : Discharge over-current detection voltage

Vshort: Load short-circuiting detection voltage

tic : Charge over-current detection delay time
tidc : Discharge over-current detection delay time
tshort : Load short-circuiting detection delay time

trel1 : Release delay time 1

• Over-charge detection



VC : Over-charge detection voltage

Vdc : Over-discharge detection voltage

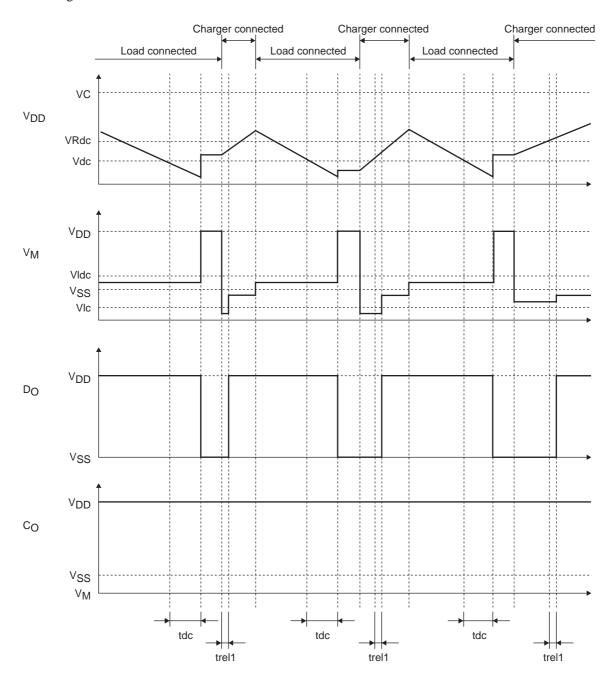
VHc : Over-charge hysteresis voltage

Vidc: Discharge over-current detection voltage

tc : Over-charge detection delay time

trel2: Release delay time 2

• Over-discharge detection



VC : Over-charge detection voltage tdc : Over-discharge detection delay time

Vdc : Over-discharge detection voltage trel1 : Release delay time 1

VRdc: Return from over-discharge voltage
Vic: Charge over-current detection voltage
Vidc: Discharge over-current detection voltage

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