

LV52207AXA



ON Semiconductor®

www.onsemi.com

Bi-CMOS LSI

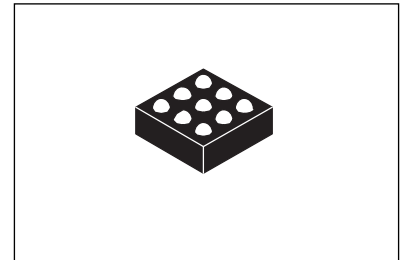
Dual channel LED Boost Driver with PWM and 1-Wire Dimming

Overview

The LV52207AXA is a high voltage boost driver for LED drive with 2 channels adjustable constant current sources.

Feature

- Operating Voltage from 2.7V to 5.5V
- Integrated 40V MOSFET
- 1-Wire 255 level digital and PWM dimming
- Supports CABC
- 600kHz Switching Frequency
- 37.5V OVP Threshold



WLP9, 1.31x1.31, 0.4mm pitch
(1.31mm x 1.31mm, Amax=0.625 mm)

Typical Applications

- LED Display Backlight Control

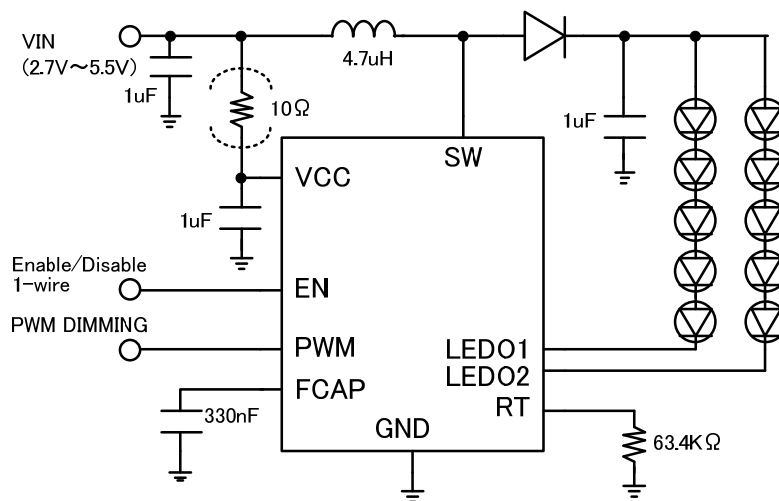


Fig1. 5x2 LED Application

ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

LV52207AXA

Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------|---------------------|-----------------|-------------|------|
| Maximum supply voltage | V _{CC} max | V _{CC} | 6 | V |
| Maximum Pin voltage1 | V1 max | SW | 40 | V |
| Maximum Pin voltage2 | V2 max | Other pin | 5.5 | V |
| Allowable power | Pd max | Ta=25°C *1 | 0.95 | W |
| Operating temperature | Topr | | -40 to +85 | °C |
| Storage temperature | Tstg | | -55 to +125 | °C |

*1 Mounted on a specified board: 70mm×70mm×1.6mm (4 layer glass epoxy)

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------|--------------------|----------------------|-------------|------|
| Supply voltage range1 | V _{CC} op | V _{CC} | 2.7 to 5.5 | V |
| PWM frequency | Fpwm | PWM pin input signal | 300 to 100k | Hz |
| MIN DUTY (PWM pin) | Dminpwm | PWM pin input signal | 0.9% | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics Analog block

at Ta=25°C, V_{CC}=3.6V, RT resistor=63.4kΩ unless otherwise specified

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------------------|-------------------|--|---------|------|-----------------|------|
| | | | min | typ | max | |
| Standby current dissipation | I _{cc1} | EN=PWM=L | | 0 | 2 | μA |
| DC/DC current dissipation1 | I _{cc2} | Device enable, switching 0.6 MHz and no load | | 0.7 | 1.2 | mA |
| FB Voltage | V _{fb} | LEDO1, 2=20mA | | 0.2 | | V |
| Output Current1 | I _{o1} | LEDO1 LEDO2 LEDISET=20mA Duty=100% | 19.6 | 20 | 20.4 | mA |
| Output Current Matching1 | I _{om1} | LEDO1 LEDO2 LEDISET=20mA Duty=100% (I _{MAX} - I _{AVG}) / I _{AVG} | | 0.3 | 2 | % |
| LEDO1, 2 max current | I _{max} | LEDO1 LEDO2 | 40 | | | mA |
| LEDO1, 2 leak current | I _{lk} | LEDO1 LEDO2 | | | 1 | μA |
| OVP Voltage | V _{ovp} | SW_pin over voltage threshold | 36 | 37.5 | 39 | V |
| LEDO_OVP Voltage | V _{Lovp} | LEDO_pin over voltage threshold LEDO DC rising | 4.2 | 4.5 | 5.0 | V |
| SWOUT ON resistance | R _{on} | I _L =100mA | | 300 | | mΩ |
| NMOS Switch Current Limit | I _{LIM} | | 1 | 1.5 | | A |
| OSC Frequency | F _{osc} | | 500 | 600 | 750 | kHz |
| High level input voltage | V _{INH} | EN PWM | 1.2 | | V _{CC} | V |
| Low level input voltage | V _{INL} | EN PWM | 0 | | 0.4 | V |
| Under Voltage Lockout | V _{uvlo} | VIN falling | | 2.2 | | V |
| EN pin output voltage for Acknowledge | V _{ack} | R _{pullup} =15kΩ | | | 0.4 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

LV52207AXA

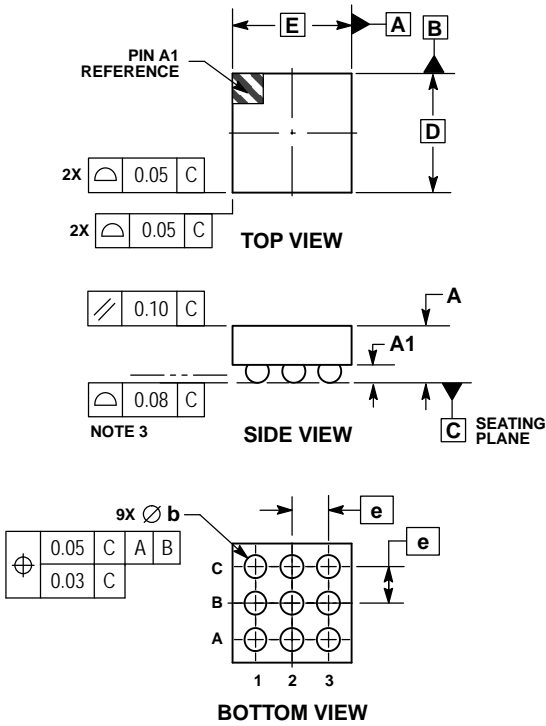
Recommended EN PWM Timing at $T_a=25^{\circ}\text{C}$, $V_{CC}=3.6\text{V}$, unless otherwise specified

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|---------|-----------------|-------------------|-----|-----|---------------|
| | | | min | typ | max | |
| Dimming mode selectable time | Tsel | | 1 | | 2.2 | ms |
| Delay time to start digital mode detection | Tw0 | | 100 | | | μs |
| Low time to switch to digital mode | Tw1 | | 260 | | | μs |
| EN pin low time to shutdown | Toffen | | 2.5 | | | ms |
| PWM pin low time to shutdown | Toffpwm | | 20 | | | ms |
| 1-wire start time for digital mode programming | Tstart | | 2 | | | μs |
| 1-wire end time for digital mode programming | Tend | | 2 | | 360 | μs |
| 1-wire High time of bit 0 | Th0 | Bit detection=0 | 2 | | 180 | μs |
| 1-wire Low time of bit 0 | TI0 | Bit detection=0 | $T_{h0} \times 2$ | | 360 | μs |
| 1-wire High time of bit 1 | Th1 | Bit detection=1 | $T_{I1} \times 2$ | | 360 | μs |
| 1-wire Low time of bit1 | TI1 | Bit detection=1 | 2 | | 180 | μs |
| DCDC startup delay | Tdel | | | 5 | | ms |
| Delay time of Acknowledge | Tackd | | | | 2 | μs |
| Duration of Acknowledge | Tack | | | | 512 | μs |

Package Dimensions

unit : mm

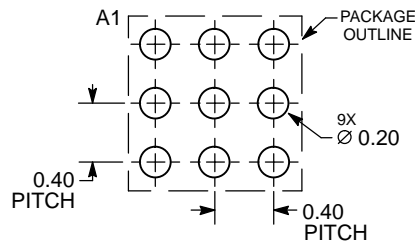
WLCSP9, 1.31x1.31
CASE 567HX
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

| MILLIMETERS | | |
|-------------|----------|-------|
| DIM | MIN | MAX |
| A | --- | 0.625 |
| A1 | 0.16 | 0.26 |
| b | 0.21 | 0.31 |
| D | 1.31 BSC | |
| E | 1.31 BSC | |
| e | 0.40 BSC | |

RECOMMENDED SOLDERING FOOTPRINT*

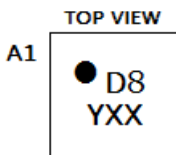


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

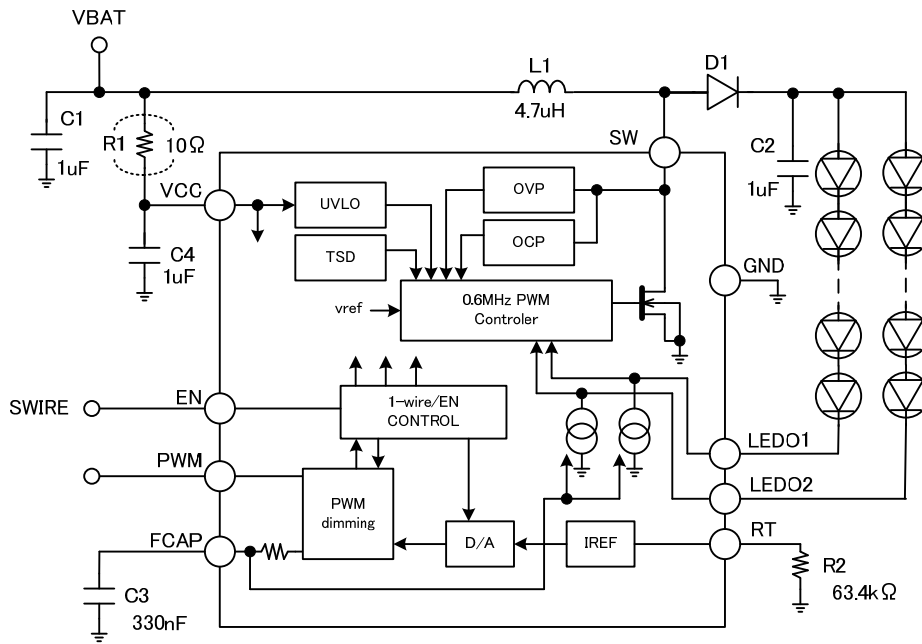
LV52207AXA is as follows.

MARKING DIAGRAM



D8 = Device Code
YXX = Assembly Lot Code

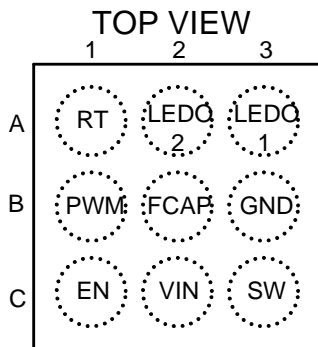
Block Diagram



L1 : VLS3012E-4R7M (TDK), VLF504015-4R7(TDK)
 VLS3012E-100M (TDK), VLF504015-100M(TDK)
 D1 : MBR0540T1 (ON semi), NSR05F40 (ON semi)
 C2 : GRM21BR71H105K (Murata), C1608X5R1H105K (TDK)

Fig2. Block Diagram

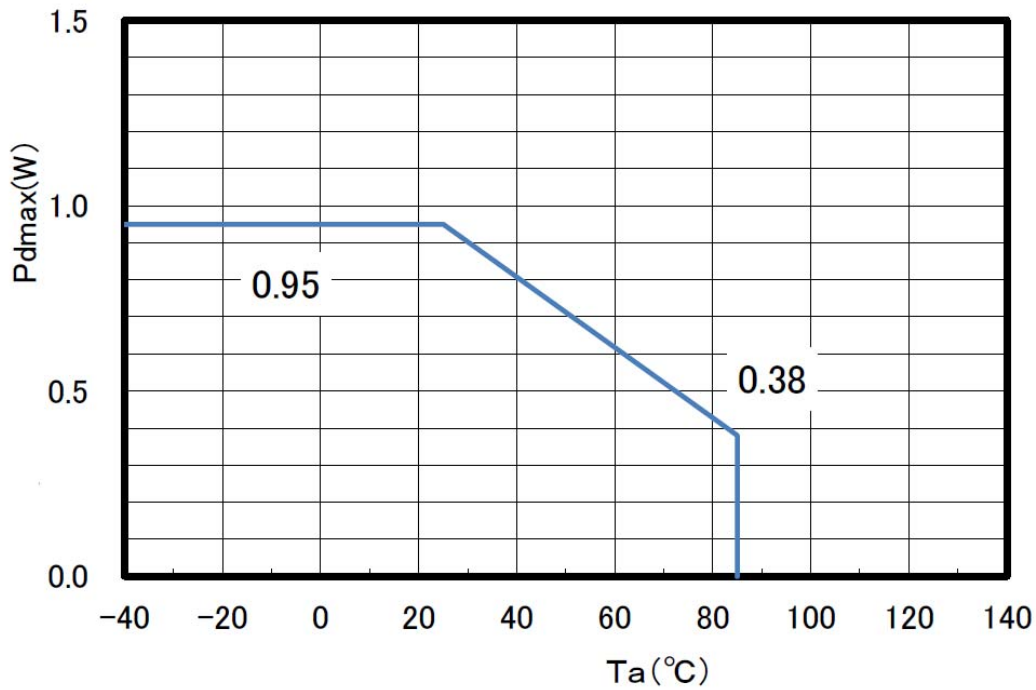
Pin Connection



Pin Function

| PIN # | Pin Name | Description |
|-------|----------|---|
| A1 | RT | Connecting a resistor terminal for Full scale LED current setting |
| A2 | LEDO2 | Constant Current Output_pin2 |
| A3 | LEDO1 | Constant Current Output_pin1 |
| B1 | PWM | PWM dimming input (active High). |
| B2 | FCAP | Filtering capacitor terminal for PWM mode |
| B3 | GND | Ground |
| C1 | EN | 1-wire control and Enable control input (active High). |
| C2 | VIN | Supply voltage. |
| C3 | SW | Switch pin. Drain of the internal power FET. |

Pd-Max



Mounted on a specified board : 70mm×70mm×1.6mm (4 layer glass epoxy)

LED Current Setting (max sink current)

LED_full current is set by an external resistor connected between the RT pin and ground.

$$I(\text{LED_full}) = 2113 \times (V(\text{RT})/R(\text{RT_res}))$$

V(RT) : RT_pin DC Voltage typ=0.6V

R(RT_res) : RT_pin resistor

RT_res=63.4kΩ : I(LED_full)=20mA

BRIGHTNESS CONTROL

The LV52207AXA controls the DC current of the dual channels. The DC current control is normally referred to as analog dimming mode.

The LV52207AXA can receive digital commands at the EN pin (1-wire digital interface) (**Digital Mode**) and the PWM signals at the PWM pin (PWM interface) (**PWM Mode**) for brightness dimming.

Dimming Mode Selection

Dimming Mode is selected by a specific pattern of the EN pin within Tsel(1ms) from the startup of the device every time.

Digital Mode

To enter Digital Mode, EN pin should be taken high for more than Tw0(100µs) from the first rising edge and keep low state for Tw1(260µs) before Tsel(1ms). When using Digital mode, the PWM pin should be kept high.

It is required sending the device address byte and the data byte to select LEDI. The bit detection is determined by the ratio of Th and Tl(See Fig5). The start condition for the bit transmission required EN pin high for at least Tstart. The end condition is required EN pin low for at least Tend. When data is not being transferred, EN pin is set in the “H” state. These registers are initialized with shutdown.

Start up and Shutdown

The device becomes enabled when EN pin is initially taken high. The dimming mode is determined within Tsel and the boost converter start up after Tdel. To place the device into shutdown mode, the SWIRE must be held low for Toff.

Digital MODE

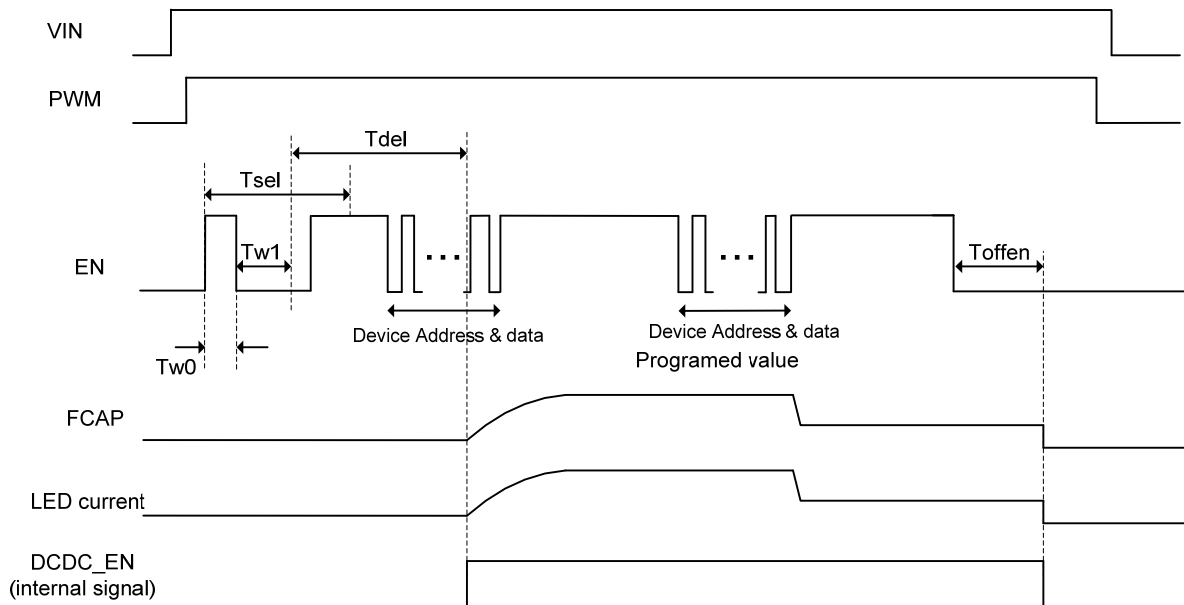


Fig3. Start up and shutdown diagram (**DIGITAL MODE**)

BOOST CONVERTER

The boost converter of the LV52207AXA integrates 40V 1.5A low side switch MOSFET and has a fixed switching frequency of 0.6MHz. The boost output voltage is automatically set by regulating LEDO1_DC and LEDO2_DC .

In order to improve the boost efficiency at light load, SKIP mode is automatically enabled under light load condition. Refer to Figure 14

1-Wire Programming

Figure 15 and Table 2 give an overview of the protocol used by LV52207AXA. A command consists of 24 bits, including an 8-bit device address byte and a 16-bit data byte. All of the 24 bits should be transmitted together each time, and the LSB bit should be transmitted first. In the LV52207AXA, the device address (DA7(MSB)to DA0(LSB)) is specified as “10001111”. AKct is setting for the acknowledge response. If the device address and the data byte are transferred on AKct=1, the ACK signal is sent from the receive side to the send side. The acknowledge signal is issued when EN pin on the send side is released and EN pin on the receive side is set to low state.

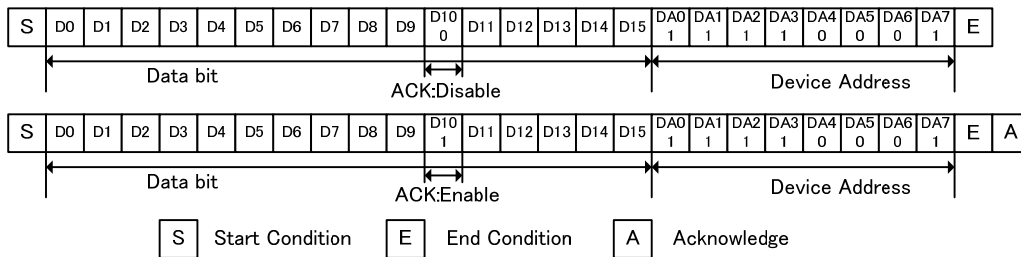


Fig4. Example of writing data

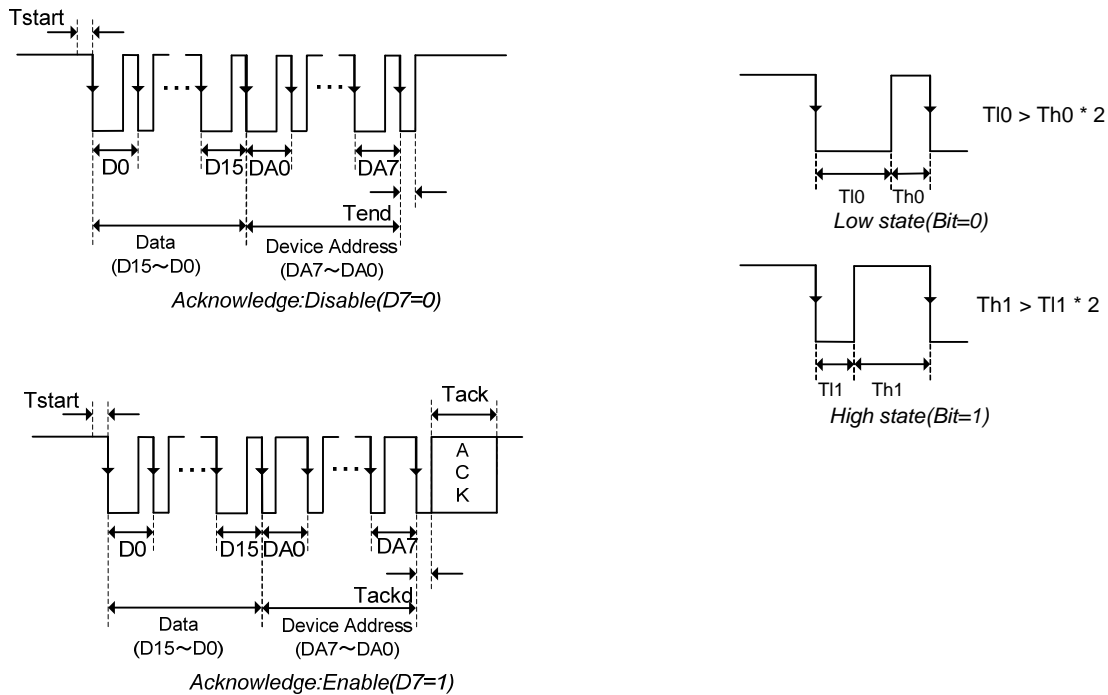


Fig5. Bit detection Diagram

LV52207AXA

| BITE | Register | BIT | Description |
|--------------------------|-----------|----------------------------|---|
| Device Address (0x8F) | DA7 | 23(MSB) | 1 |
| | DA6 | 22 | 0 |
| | DA5 | 21 | 0 |
| | DA4 | 20 | 0 |
| | DA3 | 19 | 1 |
| | DA2 | 18 | 1 |
| | DA1 | 17 | 1 |
| | DA0 | 16 | 1 |
| Data | D15 | 15 | Data bit 15 No information. Write 0 to this bit. |
| | D14 | 14 | Data bit 14 No information. Write 0 to this bit. |
| | D13 | 13 | Data bit 13 No information. Write 0 to this bit. |
| | D12 | 12 | Data bit 12 No information. Write 0 to this bit. |
| | D11 | 11 | Data bit 11 No information. Write 0 to this bit. |
| | AKct(D10) | 10 | 0 = Acknowledge disabled 1 = Acknowledge enabled |
| | D9 | 9 | Data bit 9 |
| | D8 | 8 | Data bit 8 |
| | D7 | 7 | Data bit 7 |
| | D6 | 6 | Data bit 6 |
| | D5 | 5 | Data bit 5 |
| | D4 | 4 | Data bit 4 |
| | D3 | 3 | Data bit 3 |
| | D2 | 2 | Data bit 2 |
| | D1 | 1 | Data bit 1 LSB of brightness code |
| D0 | 0(LSB) | Data bit 0 No information. | |

Table1. Bit Description

LED Current setting RT resistor=63.4KΩ (20mA)

LED current = I(LED_full) x code/255= LEDO1current=LEDO2current

| code | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | LED Current(mA) |
|------|----|----|----|----|----|----|----|----|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 Unavailable |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.22 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.30 |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0.38 |
| 4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0.47 |
| 5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0.55 |
| 6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0.63 |
| 7 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0.70 |
| 8 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0.78 |
| 9 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0.86 |
| 10 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0.94 |
| · | | | | | | | | | · |
| 246 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 19.30 |
| 247 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 19.38 |
| 248 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 19.46 |
| 249 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 19.54 |
| 250 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 19.61 |
| 251 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 19.69 |
| 252 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 19.77 |
| 253 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 19.84 |
| 254 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 19.93 |
| 255 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 20 *Default |

Table2. Data Register vs LED current sink

PWM Mode

The dimming mode is set to PWM mode when it is not recognized as a digital mode within Tsel. The LV52207AXA can receive the PWM signals at the PWM pin (PWM interface)(**PWM Mode**) for brightness dimming. When using PWM interface, the EN pin should be kept high. If EN pin is H, PWM pin alone is used to enable and disable the IC. When EN pin is H and PWM pin is H, this IC is enable. When EN pin more than 2.5ms are low or when PWM pin more than 20ms are low, the IC is disable.

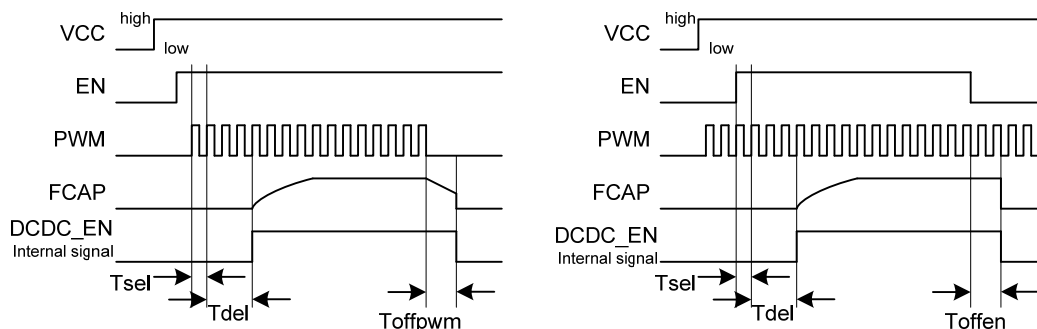


Fig6. Start up and shutdown diagram (**PWM MODE**)

LEDO1 or LEDO2 UNUSED

If only one channel is used, a user can be made to OFF by connecting to ground the unused channel. If LEDO1 pin and LEDO2 pin are connected to ground, dc/dc will not start up.

Over Voltage Protection (SW OVP)

SW pin over-voltage protection is set at 37.5V. This IC monitors the Voltage at SW pin. When the voltage exceed OVP threshold, the switching converter stops switching.

If SW terminal voltage exceeds a threshold Vovp (37.5V typ) for 8 cycles, boost converter enters shutdown mode. In order to restart the IC, SWIRE signal is required again.

Over Voltage Protection (LEDO OVP)

LED pin over-voltage protection is set at 4.5V(rise) 3.5V(fall). This IC monitors the Voltage at LEDO1 pin and LEDO2 pin. When the voltage exceed LEDO OVP threshold, the switching converter stops switching. LED current sink keep.

Open LED Protection

< When one LED string becomes open.>

If one LED string is open, open channel voltage is about ground, the boost output voltage is increased and other LEDO channel voltage is increased. When SW pin voltage is reached the SW OVP threshold the LV52207AXA's switching converter stops switching. When other LEDO pin voltage is reached the LEDO OVP threshold, the LV52207AXA's switching converter stops switching.

< When both LED strings become open.>

If both LED strings are open, LEDO1 pin voltage and LEDO2 pin voltage is about ground, and the boost output voltage is increased

When SW pin voltage is reached the SW OVP threshold the LV52207AXA's switching converter stops switching.

Over Current Protection

Current limit value for built-in power MOS is around 1.5A. The power MOS is turned off for each switching cycle when peak current through it exceeds the limit value.

Under Voltage Lock Out (UVLO)

UVLO operation works when VIN terminal voltage is below 2.2V.

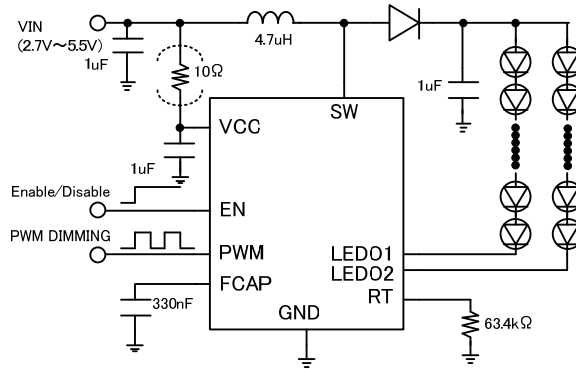
Thermal Shutdown

When chip temperature is too high, boost converter is stopped.

Application Circuit Diagram

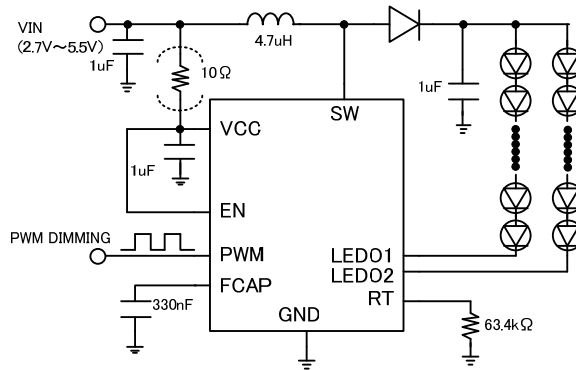
PWM dimming mode

EN pin can be used to enable or disable



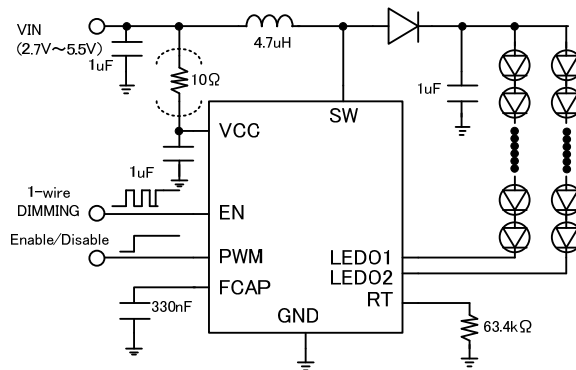
PWM dimming mode

PWM pin can be used to enable or disable



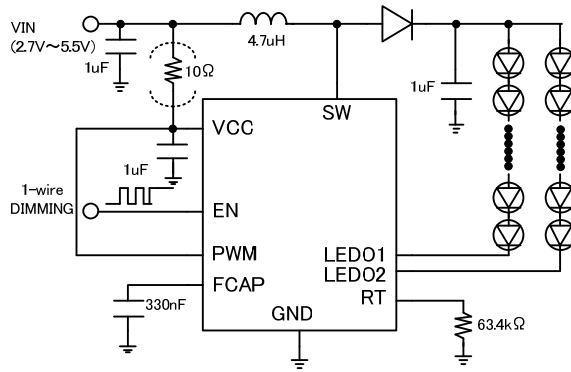
1-wire dimming mode

PWM pin can be used to enable or disable

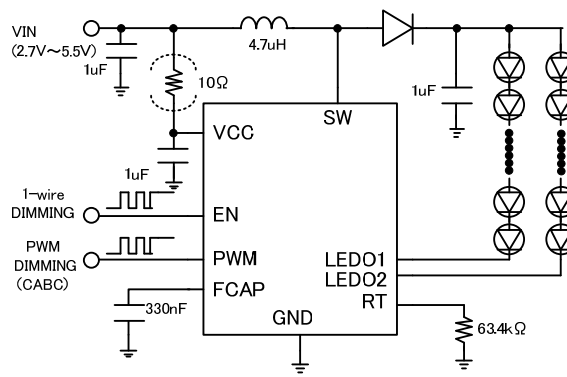


1-wire dimming mode

EN pin can be used to enable or disable



1-wire dimming mode and PWM dimming mode (CABC)



Notes start-up sequences

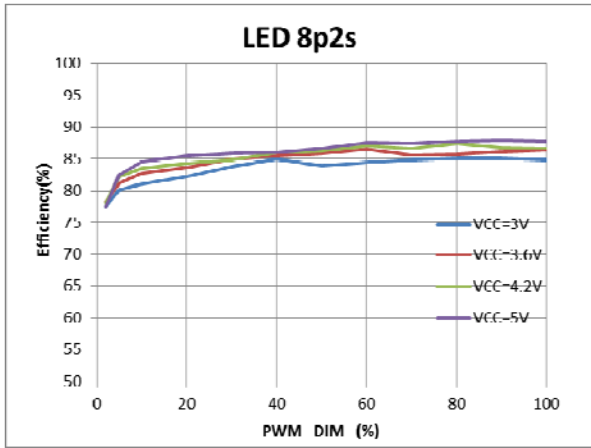
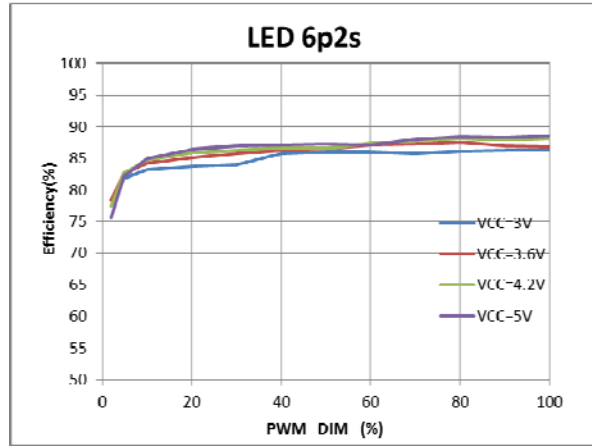
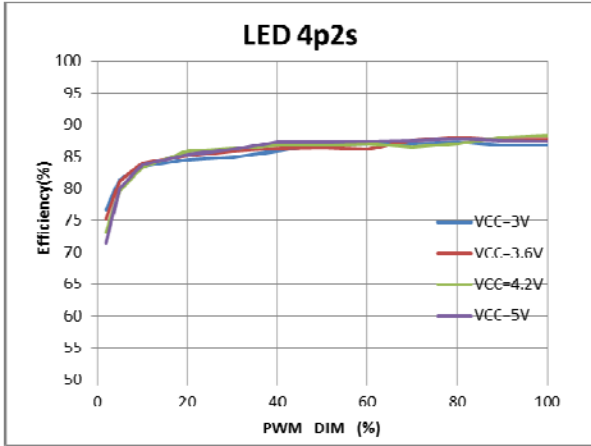
During Tw0 period of 1-wire, it is necessary to make PWM "High".

Fig7. Various application circuit diagram

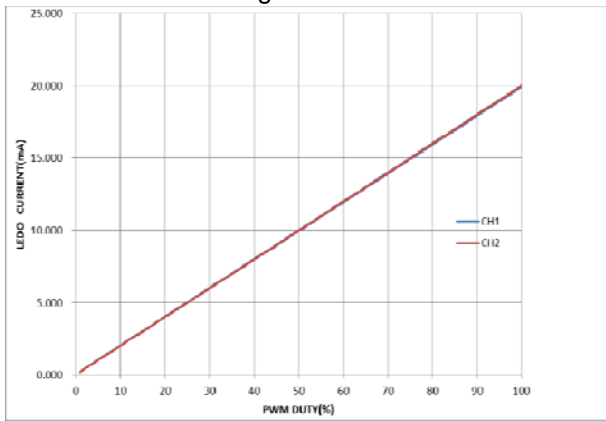
LV52207AXA

Typical Characteristics (VIN=3.6V, L=10uH, T=25degC, unless otherwise specified)

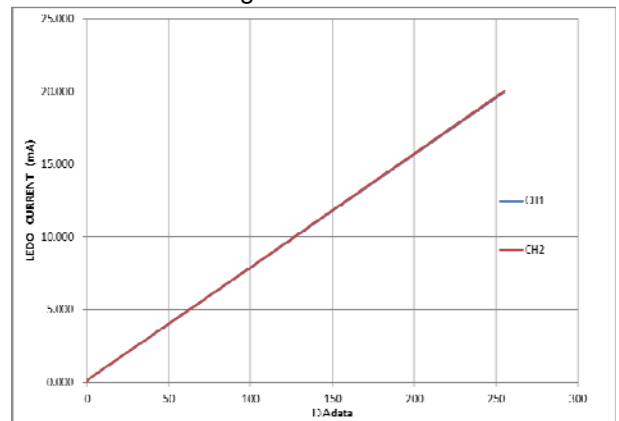
Efficiency vs PWM DIMMING (20mA/string) Fig8



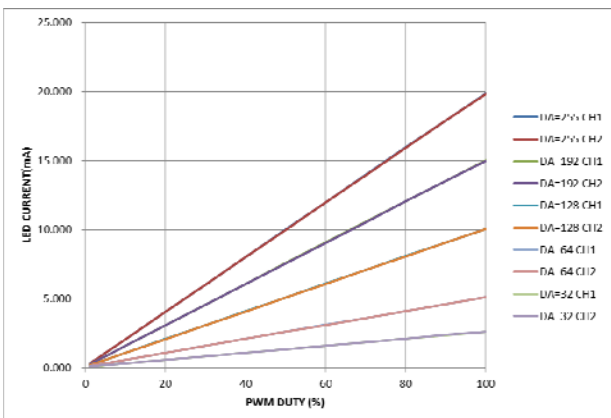
PWM DIMMING Fig9



1-wire DIMMING Fig10

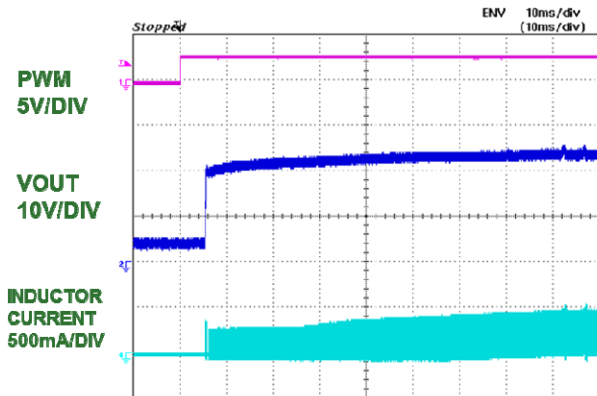


CABC DIMMING Fig11

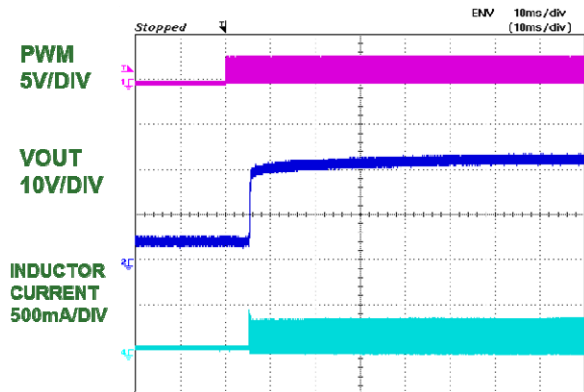


START UP WAVEFORM Fig12

PWM DUTY=100%
LED 7s2p

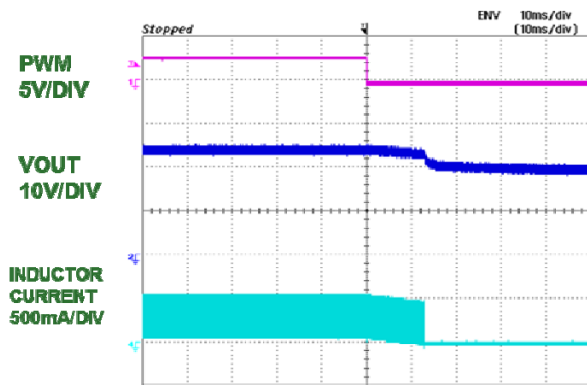


PWM DUTY=50%
LED 7s2p

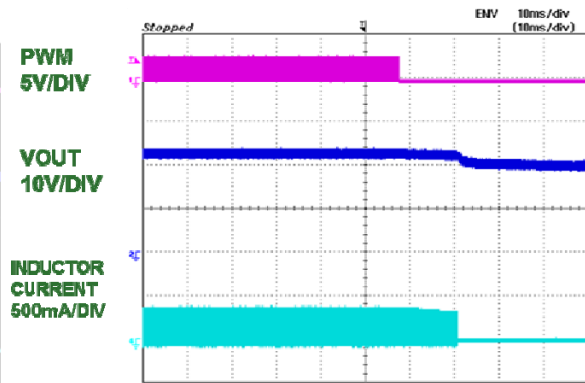


SHUTDOWN WAVEFORM Fig13

PWM DUTY=100%
LED 7s2p

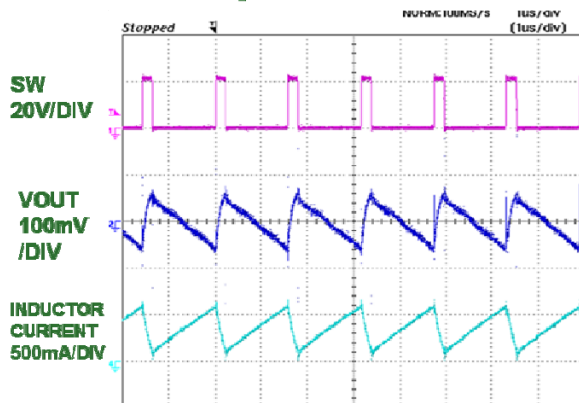


PWM DUTY=50%
LED 7s2p

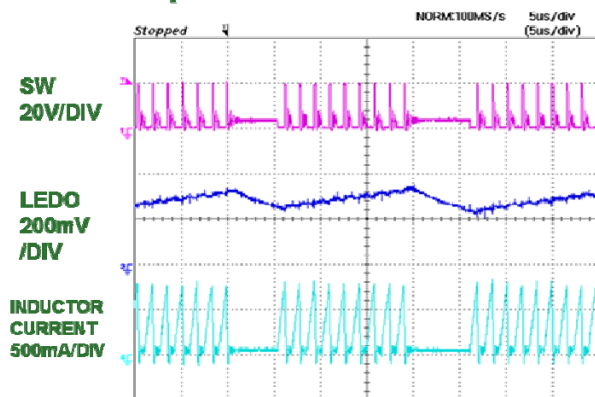


SWITCHING WAVEFORM Fig14

PWM DUTY=100%
LED 7s2p



PWM DUTY=20%
LED 7s2p

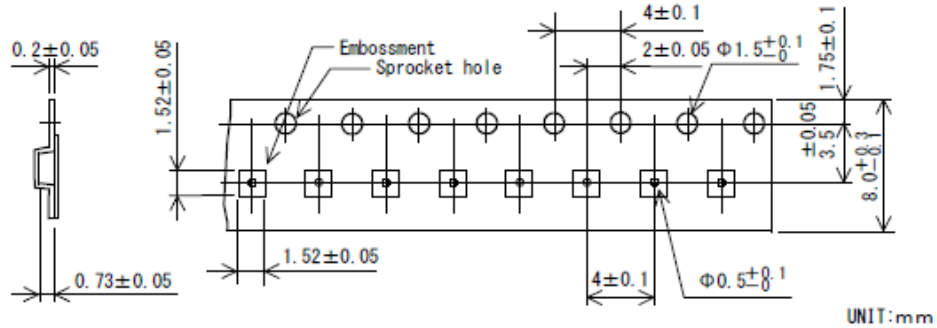


Packing Specification of Embossed Carrier Taping

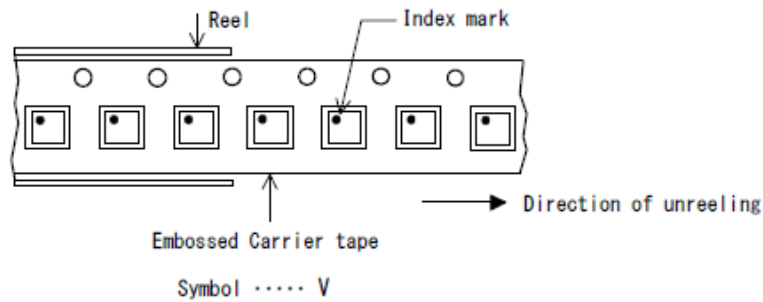
WLP9 (1.31X1.31)

1. EMOSS CARRIER TAPING

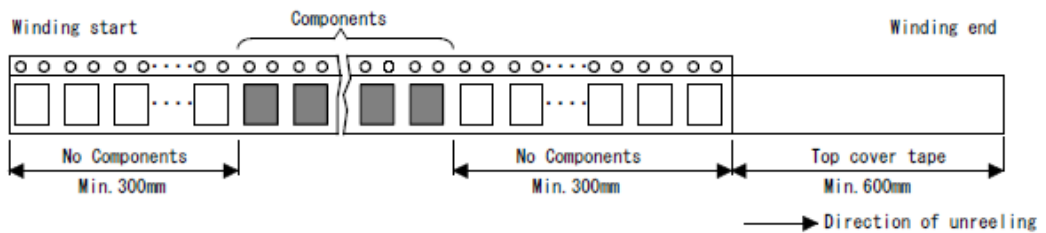
1-1. Emboss carrier tape dimensions



1-2. Tape mounting direction



1-3. Reel winding start and reel winding end



2. TAPE STRENGTH

2-1. Tensile strength of the carrier tape : Min.10N

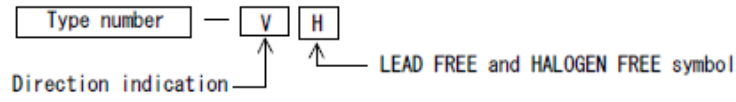
2-2. Peel strength of the top cover tape

- (a) Peel angle : 165° to 180° relative to the tape adhesive surface
- (b) Peel rate : 300mm / minute
- (c) Peel of strength : 0.1N to 1.0N

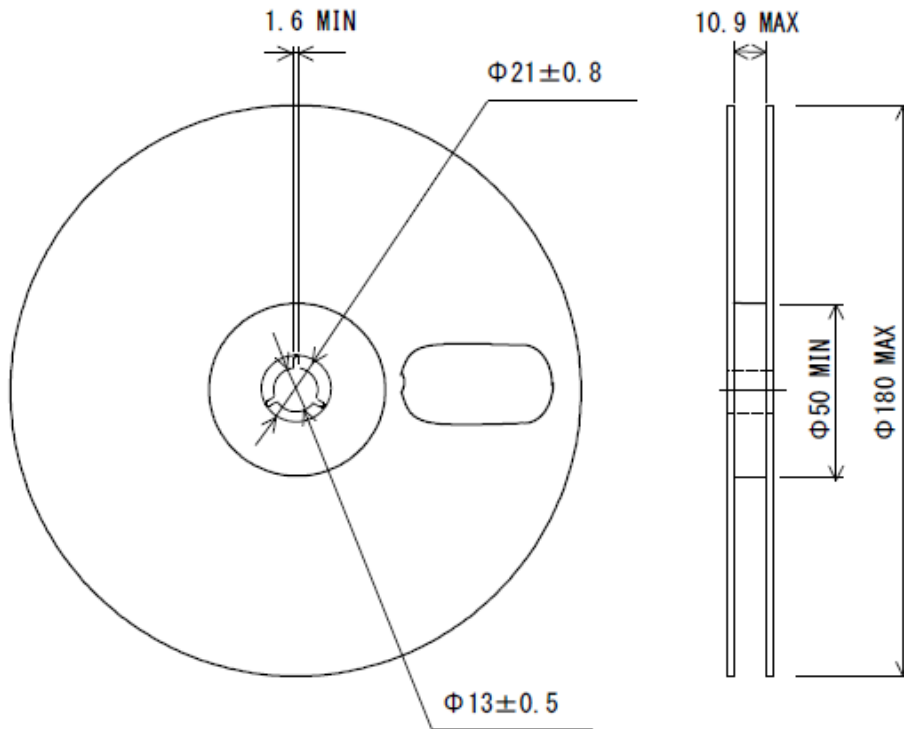
Packing Specification of Embossed Carrier Taping

WLP9 (1.31X1.31)

3. PARTS No. ON BAR CODE LABEL



4. REEL DIMENSIONS



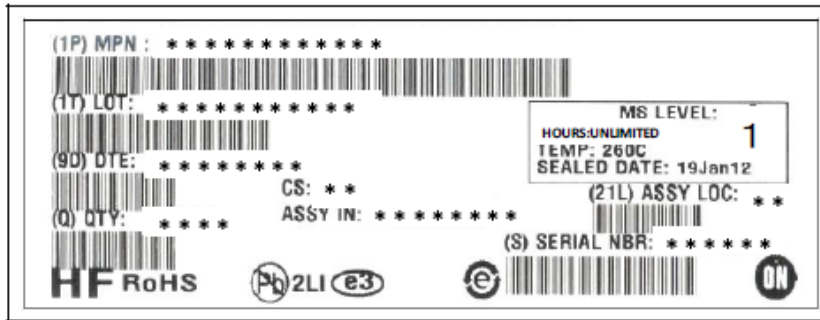
MODEL : RRM-08B
UNIT : mm

Packing Specification of Embossed Carrier Taping

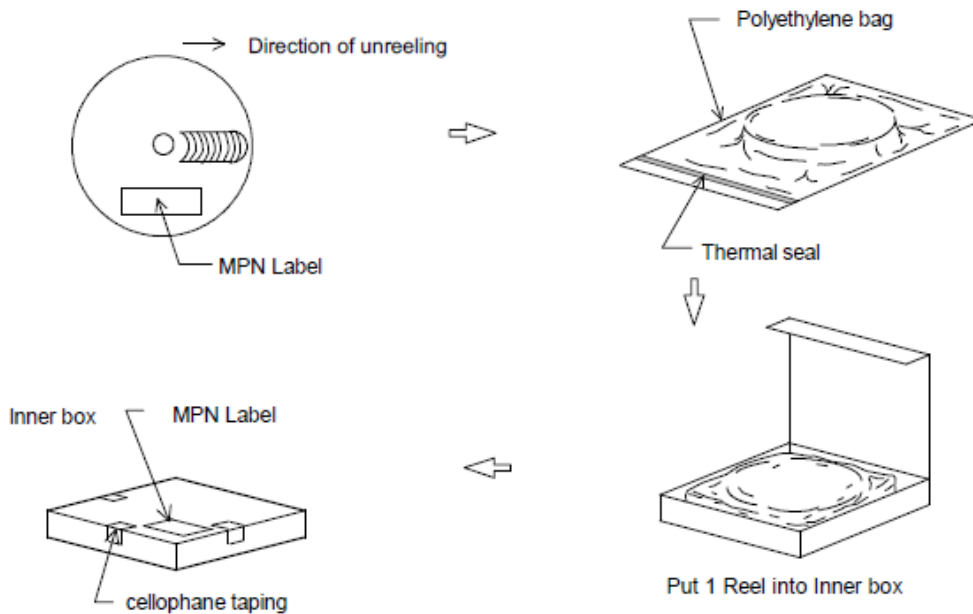
WLP9 (1.31X1.31)

| Carrier tape type number | Package code | Maximum number of ICs contained (pcs.) | | Packing form |
|--------------------------|------------------|--|-----------|--|
| | | Reel | Inner box | Inner box. BOX (TE-1208) |
| CARR (BD0145X0145) | WLP9 (1.31X1.31) | 5,000 | 5,000 | 1 Reels contained Dimensions:mm 190×37×190 |

MPN Label



Packing Method



ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---------------|--|--------------------------|
| LV52207AXA-VH | WLP9 (1.31x1.31) (Pb-Free / Halogen Free) | 5000 / Tape & Reel |

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.