

# LV52207NXB

## LED Boost Driver, Dual Channel, PWM, 1-Wire Dimming

### Overview

The LV52207NXB is a high voltage boost driver for LED drive with 2 channels adjustable constant current sources.

### Features

- Operating Voltage from 2.7 V to 5.5 V
- Integrated 40 V MOSFET
- 1-wire 255 level digital and PWM dimming
- Supports CABC
- 600 kHz Switching Frequency
- 37.5 V Overvoltage Protection (OVP) Threshold
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- LED Display Backlight Control

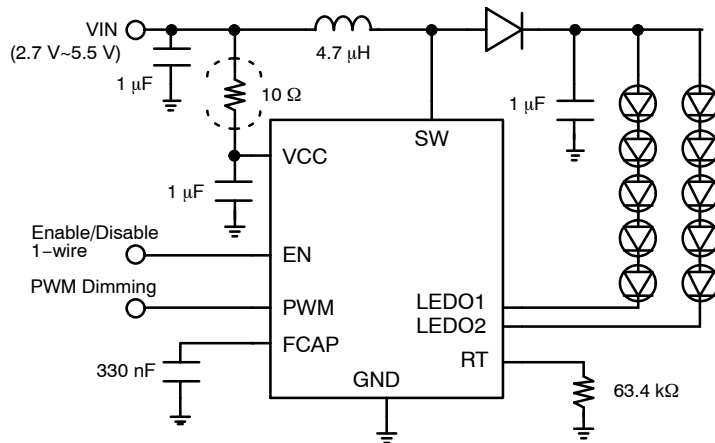


Figure 1. 5 x 2 LED Application



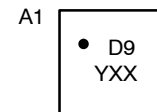
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WLCSP9, 1.31x1.31  
CASE 567HX

### MARKING DIAGRAM

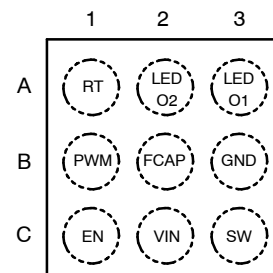


(Top View)

D9 = Specific Device Code  
YXX = Assembly Lot Code

OPTION: BACKSIDE COATING

### PIN CONNECTION



(Top View)

### ORDERING INFORMATION

Device	Package	Shipping
LV52207NXB-VH	WLCSP9 (Pb-Free/ Halogen Free)	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://BRD8011/D).

SPECIFICATIONS

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply Voltage	V <sub>CC</sub> max	V <sub>CC</sub>	6	V
Maximum Pin Voltage1	V1 max	SW	40	V
Maximum Pin Voltage2	V2 max	Other pin	5.5	V
Allowable Power Dissipation	Pd max	Ta = 25°C (Note 1)	1.05	W
Operating Temperature	Topr		-40 to +85	°C
Storage Temperature	Tstg		-55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on the following board: 70 mm × 70 mm × 1.6 mm (4 layer glass epoxy)
2. Absolute maximum ratings represent the values which cannot be exceeded for any length of time.
3. When the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be decrease. Please contact ON Semiconductor for the further details.

**RECOMMENDED OPERATING CONDITIONS** (Ta = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage Range1	V <sub>CC</sub> op	V <sub>CC</sub>	2.7 to 5.5	V
PWM Frequency	F <sub>PWM</sub>	PWM pin input signal	300 to 100k	Hz
Min. Duty% on PWM Pin	D <sub>MIN</sub> PWM	PWM pin input signal	0.5	%

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

\*Recommended MIN duty % on PWM pin is a design assurance

**ELECTRICAL CHARACTERISTICS ANALOG BLOCK** (Ta = 25°C, V<sub>CC</sub> = 3.6 V, RT resistor = 63.4 kΩ unless otherwise specified)

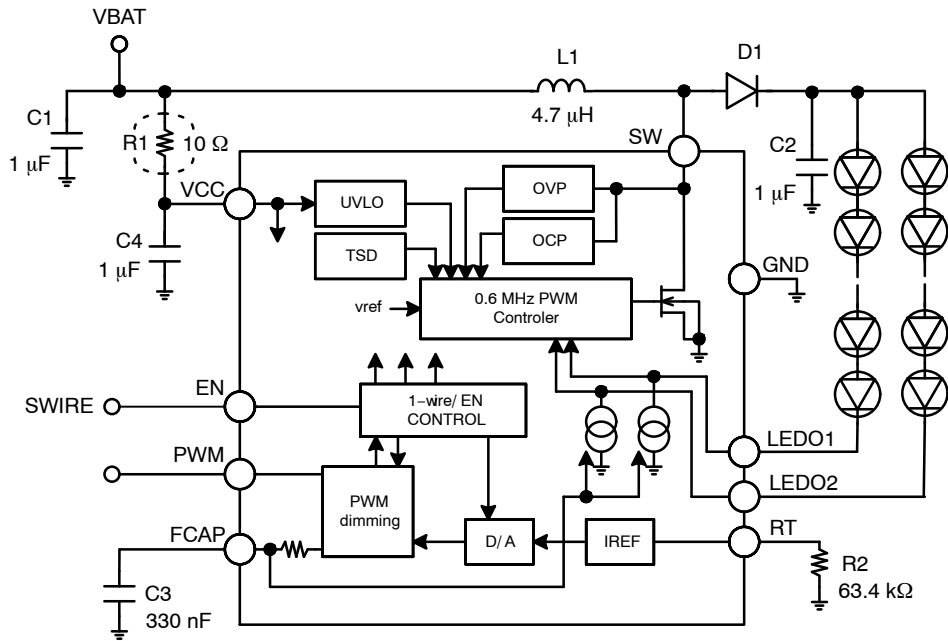
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Standby Current Dissipation	I <sub>CC1</sub>	EN = PWM = L		0	2.0	μA
DC/DC Current Dissipation1	I <sub>CC2</sub>	Device enable, switching 0.6 MHz and no load		0.7	1.2	mA
Feedback Voltage	V <sub>FB</sub>	LEDO1, 2 = 20 mA		0.2		V
Output Current1	I <sub>O1</sub>	LEDO1, LEDO2, LEDISET = 20 mA Duty = 100%	19.6	20	20.4	mA
Output Current Matching1	I <sub>OM1</sub>	LEDO1, LEDO2, LEDISET = 20 mA Duty = 100% (I <sub>MAX</sub> - I <sub>AVG</sub> ) / I <sub>AVG</sub>		0.3	2.0	%
LEDO1, 2 Max Current	I <sub>MAX</sub>	LEDO1 LEDO2	40			mA
LEDO1, 2 Leak Current	I <sub>LEAK</sub>	LEDO1 LEDO2			1.0	μA
OVP Voltage	V <sub>OVP</sub>	SW_pin over voltage threshold	36	37.5	39	V
LEDO_OVP Voltage	V <sub>OVP,LED</sub>	LEDO_pin over voltage threshold LEDO_DC rising	4.2	4.5	5.0	V
SW <sub>OUT</sub> ON Resistance	R <sub>ON</sub>	I <sub>L</sub> = 100 mA		300		mΩ
NMOS Switch Current Limit	I <sub>LIM</sub>		1.0	1.5		A
OSC Frequency	F <sub>OSC</sub>		500	600	750	kHz
High Level Input Voltage	V <sub>INH</sub>	EN PWM	1.2		V <sub>CC</sub>	V
Low Level Input Voltage	V <sub>INL</sub>	EN PWM	0		0.4	V
Under Voltage Lockout	V <sub>UVLO</sub>	VIN falling		2.2		V
EN Pin Output Voltage for Acknowledge	V <sub>ACK</sub>	R <sub>PULL-UP</sub> = 15 kΩ			0.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**RECOMMENDED EN PWM TIMING** (Ta = 25°C, VCC = 3.6 V unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Dimming Mode Selectable Time	T <sub>SEL</sub>		1.0		2.2	ms
Delay Time to Start Digital Mode Detection	T <sub>w0</sub>		100			μs
Low Time to Switch to Digital Mode	T <sub>w1</sub>		260			μs
EN Pin Low Time to Shutdown	T <sub>OFF, EN</sub>		2.5			ms
PWM Pin Low Time to Shutdown	T <sub>OFF, PWM</sub>		20			ms
1-wire Start Time for Digital Mode Programming	T <sub>START</sub>		2.0			μs
1-wire End Time for Digital Mode Programming	T <sub>END</sub>		2.0		360	μs
1-wire High Time of Bit 0	T <sub>H0</sub>	Bit detection = 0	2.0		180	μs
1-wire Low Time of Bit 0	T <sub>L0</sub>	Bit detection = 0	T <sub>H0</sub> × 2		360	μs
1-wire High Time of Bit 1	T <sub>H1</sub>	Bit detection = 1	T <sub>L1</sub> × 2		360	μs
1-wire Low Time of Bit 1	T <sub>L1</sub>	Bit detection = 1	2.0		180	μs
DCDC Startup Delay	T <sub>DEL</sub>			5		ms
Delay time of Acknowledge	T <sub>ACKD</sub>				2	μs
Duration of Acknowledge	T <sub>ACK</sub>				512	μs

**BLOCK DIAGRAM**



L1: VLS3012E-4R7M (TDK), VLF504015-4R7 (TDK) VLS3012E-100M (TDK), VLF504015-100M (TDK)  
 D1: MBR0540T1 (ON Semiconductor), NSR05F40 (ON Semiconductor)  
 C2: GRM21BR71H105K (Murata), C1608X5R1H105K (TDK)

**Figure 2. Block Diagram**

PIN CONNECTION

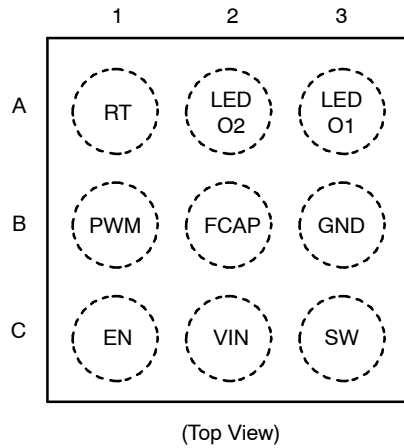


Figure 3. Pin Connection

PIN FUNCTION

Pin No.	Pin Name	Description
A1	RT	Connecting a resistor terminal for Full scale LED current setting
A2	LEDO2	Constant Current Output_pin2
A3	LEDO1	Constant Current Output_pin1
B1	PWM	PWM dimming input (active High)
B2	FCAP	Filtering capacitor terminal for PWM mode
B3	GND	Ground
C1	EN	1-wire control and Enable control input (active High)
C2	VIN	Supply voltage
C3	SW	Switch pin. Drain of the internal power FET

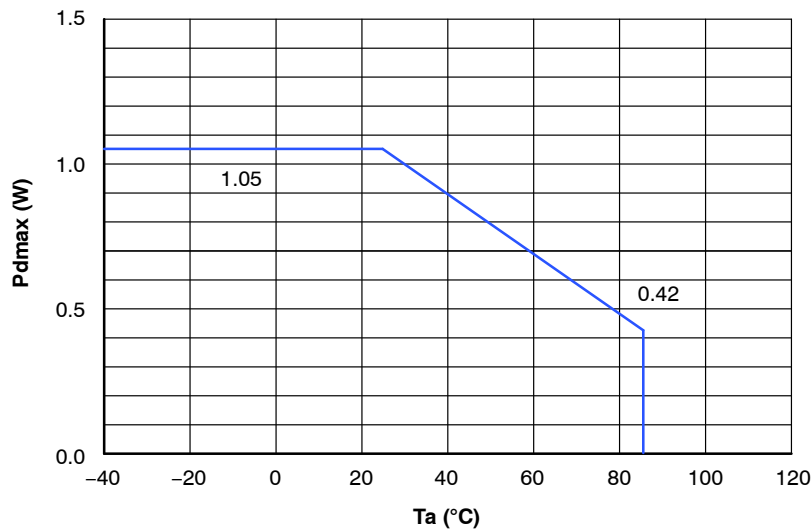


Figure 4. Pd-Max – Mounted on the Following Board: 70 mm × 70 mm × 1.6 mm (4 Layer Glass Epoxy)

**LED CURRENT SETTING (MAX SINK CURRENT)**

LED\_full current is set by an external resistor connected between the RT pin and ground.

$$I_{LED\_Full} = 2113 \times \frac{V_{RT}}{R_{RT}} \quad (\text{eq. 1})$$

$V_{RT}$  – RT pin DC Voltage; typically 0.6 V

$R_{RT}$  – RT pin resistor to ground

Eg:  $R_{T\_res} = 63.4 \text{ k}\Omega$  at typical  $V_{RT}$

$$I_{LED\_Full} = 2113 \times \frac{V_{RT}}{R_{RT}} = 2113 \times \frac{0.6 \text{ V}}{63.4 \text{ k}\Omega} = 19.99 \text{ mA} \approx 20 \text{ mA} \quad (\text{eq. 2})$$

**PWM DIMMING CONTROL**

To avoid LED light off, 75  $\mu\text{A}$  offset per channel for PWL duty was designed.

$$I_{LED} = I_{LED\_Full} \times 0.00375 + (I_{LED\_Full} - I_{LED\_Full} \times 0.00375) \times \text{PWMDUTY} \quad (\text{eq. 3})$$

PWMDUTY: PWM pin DUTY

$$I_{LED\_Full} \times 0.00375 \approx 75 \mu\text{A} \quad (\text{eq. 4})$$

\*This formula is applicable at PWM = 10 kHz. When used the higher frequency, a gap gradually occurs.

**BRIGHTNESS CONTROL**

The LV52207NXB controls the DC current of the dual channels. The DC current control is normally referred to as analog dimming mode.

The LV52207NXB can receive digital commands at the EN pin (1-wire digital interface, known as *Digital Mode*) and the PWM signals at the PWM pin (PWM interface, known as *PWM Mode*) for brightness dimming.

**Dimming Mode Selection**

Dimming Mode is selected by a specific pattern of the EN pin within  $T_{SEL}$  of 1.0 ms from the startup of the device every time.

**DIGITAL MODE**

To enter Digital Mode, EN pin should be taken high for more than  $T_{W0} = 100 \mu\text{s}$  from the first rising edge and keep low state for  $T_{W1} = 260 \mu\text{s}$  before  $T_{SEL} = 1 \text{ ms}$ . It is required sending the device address byte and the data byte to select LEDI. The bit detection is determined by the ratio of  $T_H$  and  $T_L$  (See Figure 7). The start condition for the bit transmission required EN pin high for at least  $T_{start}$ . The end condition is required EN pin low for at least  $T_{end}$ . When data is not being transferred, EN pin is set in the “H” state. These registers are initialized with shutdown.

**Start Up and Shutdown**

The device becomes enabled when EN pin is initially taken high. The dimming mode is determined within  $T_{SEL}$  and the boost converter start up after  $T_{DEL}$ . To place the device into shutdown mode, the SWIRE must be held low for  $T_{OFF}$ . For specific timings please refer to the Recommended EN PWMIN Timing Table on page 3 or the below figures.

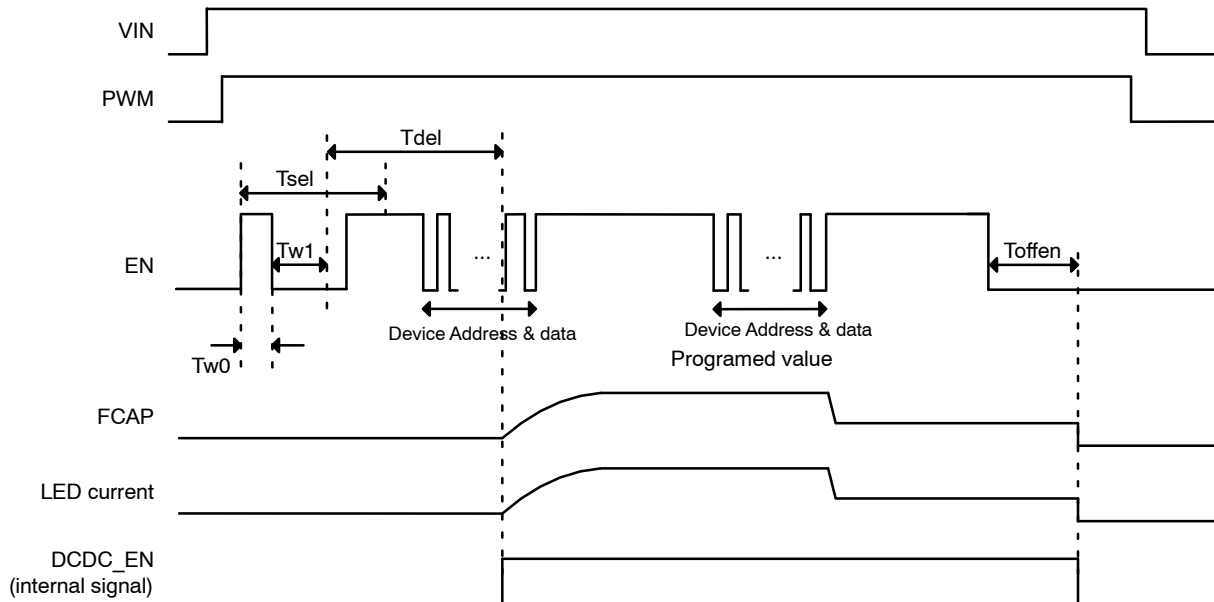


Figure 5. Start Up and Shutdown Diagram (Digital Mode)

1-wire Programming

Figure 6 and Table 2 give an overview of the protocol used by LV52207NXB. A command consists of 24 bits, including an 8-bit device address byte and a 16-bit data byte. All of the 24 bits should be transmitted together each time, and the LSB bit should be transmitted first. In the LV52207NXB, the device address (DA7(MSB) to

DA0(LSB)) is specified as “10001111”. AKct is setting for the acknowledge response. If the device address and the data byte are transferred on Akct = 1, the ACK signal is sent from the receive side to the send side. The acknowledge signal is issued when EN pin on the send side is released and EN pin on the receive side is set to low state.

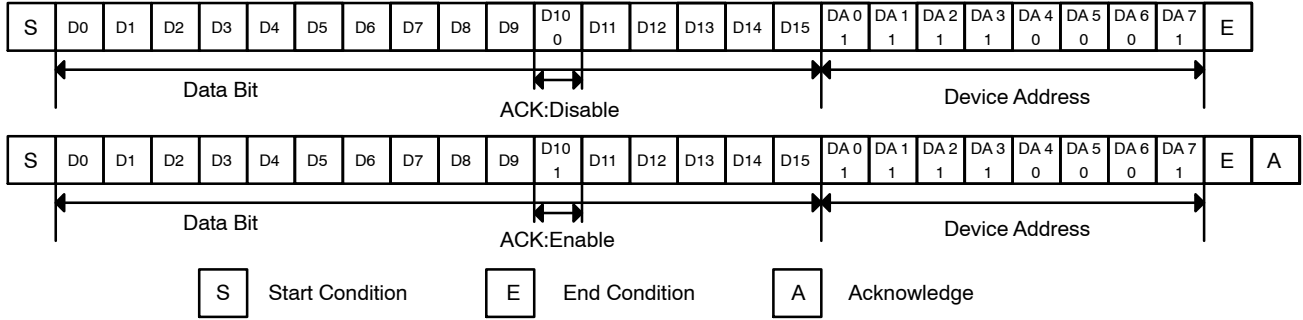


Figure 6. Example of Writing Data

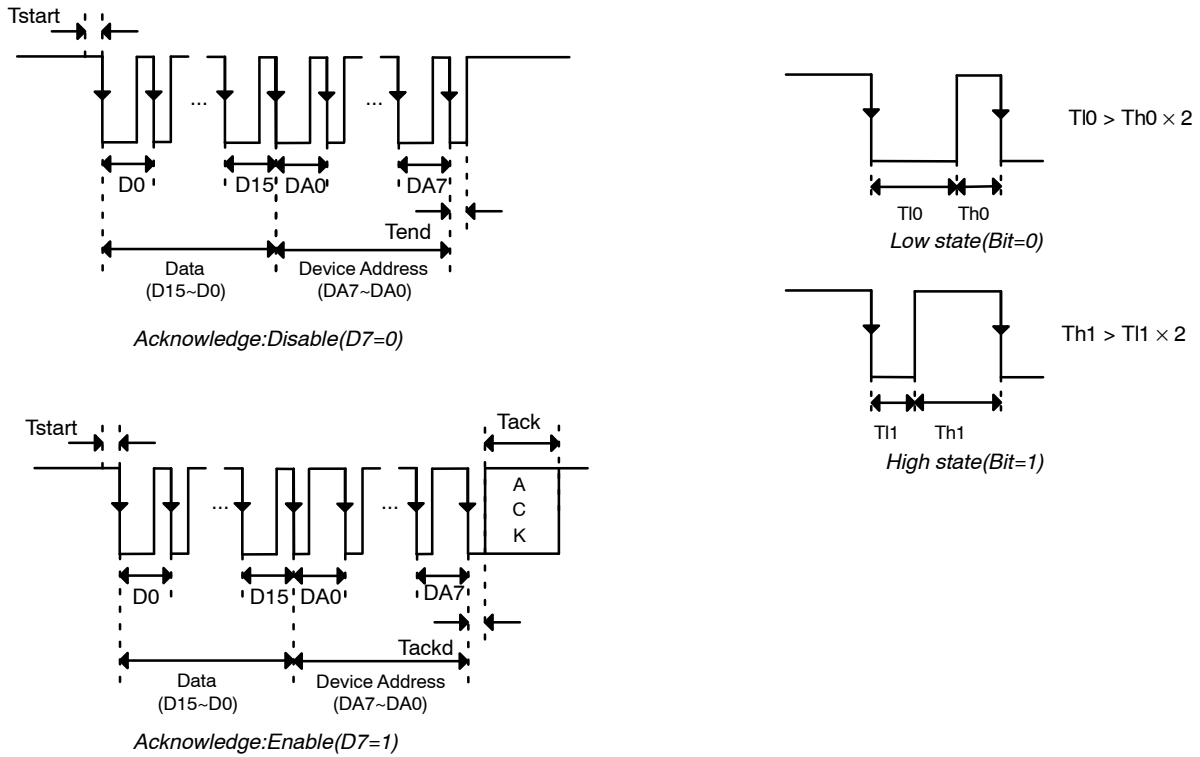


Figure 7. Bit Detection Diagram

Table 1. BIT DESCRIPTION

BITE	Register	BIT	Description
Device Address (0x8F)	DA7	23 (MSB)	1
	DA6	22	0
	DA5	21	0
	DA4	20	0
	DA3	19	1
	DA2	18	1
	DA1	17	1
	DA0	16	1
Data	D15	15	Data bit 15 No information. Write 0 to this bit
	D14	14	Data bit 14 No information. Write 0 to this bit
	D13	13	Data bit 13 No information. Write 0 to this bit
	D12	12	Data bit 12 No information. Write 0 to this bit
	D11	11	Data bit 11 No information. Write 0 to this bit
	Akct (D10)	10	0 = Acknowledge disabled 1 = Acknowledge enabled
	D9	9	Data bit 9
	D8	8	Data bit 8
	D7	7	Data bit 7
	D6	6	Data bit 6
	D5	5	Data bit 5
	D4	4	Data bit 4
	D3	3	Data bit 3
	D2	2	Data bit 2
	D1	1	Data bit 1 LSB of brightness code
	D0	0 (LSB)	Data bit 0 No information

LED Current setting: RT resistor = 63.4 kΩ (for I<sub>LED Full</sub> = 20 mA)

NOTE: If you change the RT resistor, the LED Currents will all change.

$$I_{LED} = I_{LED\_Full} \times \frac{\text{code \#}}{255}$$

Where I<sub>LED\_FULL</sub> is the current calculated above.

$$I_{LED} = I_{LEDO1} = I_{LEDO2}$$

Table 2. DATA REGISTER VS. LED CURRENT SINK

Code	D8	D7	D6	D5	D4	D3	D2	D1	LED Current (mA)
0	0	0	0	0	0	0	0	0	0 Unavailable
1	0	0	0	0	0	0	0	1	0.22
2	0	0	0	0	0	0	1	0	0.30
3	0	0	0	0	0	0	1	1	0.38
4	0	0	0	0	0	1	0	0	0.47
5	0	0	0	0	0	1	0	1	0.55
6	0	0	0	0	0	1	1	0	0.63
7	0	0	0	0	0	1	1	1	0.70
8	0	0	0	0	1	0	0	0	0.78
9	0	0	0	0	1	0	0	1	0.86
10	0	0	0	0	1	0	1	0	0.94
.	:								.
.	:								.
.	:								.
246	1	1	1	1	0	1	1	0	19.30
247	1	1	1	1	0	1	1	1	19.38
248	1	1	1	1	1	0	0	0	19.46
249	1	1	1	1	1	0	0	1	19.54
250	1	1	1	1	1	0	1	0	19.61
251	1	1	1	1	1	0	1	1	19.69
252	1	1	1	1	1	1	0	0	19.77
253	1	1	1	1	1	1	0	1	19.84
254	1	1	1	1	1	1	1	0	19.93
255	1	1	1	1	1	1	1	1	20 *Default



## PWM MODE

The dimming mode is set to PWM mode when it is not recognized as a digital mode within  $T_{sel}$ . The LV52207NXB can receive the PWM signals at the PWM pin (PWM interface, also known as *PWM Mode*) for brightness dimming. When using PWM interface, the EN pin should be

kept high. If EN pin is High, PWM pin alone is used to enable and disable the IC. When EN pin is High and PWM pin is High, this IC is enabled. When EN pin is Low for more than 2.5 ms or when PWM pin is Low for more than 20 ms, the IC is disabled.

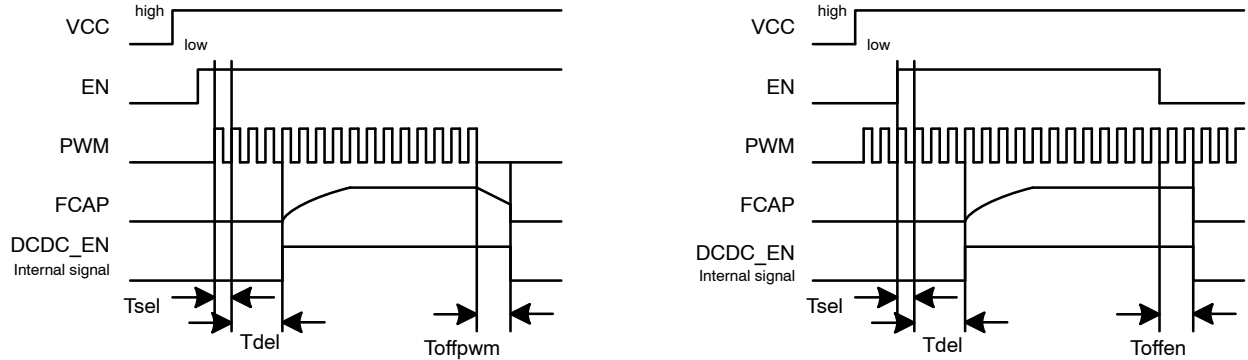


Figure 8. Start Up and Shutdown Diagram (PWM Mode)

### LEDO1 or LEDO2 UNUSED

If only one channel is used, a user can turn OFF a branch current by connecting the unused channel to ground.

If both LEDO1 pin and LEDO2 pin are connected to ground, boost converter will not start up.

### Over Voltage Protection (SW OVP)

SW pin over-voltage protection is set at 37.5 V. *This IC monitors the Voltage at SW pin.* When the voltage exceeds OVP threshold the switching converter stops switching.

If SW terminal voltage exceeds a threshold  $V_{OVP} = 37.5$  V typ. for 8 cycles, boost converter enters shutdown mode. In order to restart the IC, SWIRE signal must be used again.

### Over Voltage Protection (LEDO OVP)

LED pin over-voltage protection is set at 4.5 V (rising) and 3.5 V (falling). *This IC monitors the Voltage at LEDO1 pin and LEDO2 pin.* When the voltage exceeds LEDO OVP threshold the switching converter stops switching, LED current sink keep.

### Open LED Protection

- When one LED string becomes open:  
If one LED string is open, open channel voltage is approximately ground, the boost output voltage is

increased and other LEDO channel voltage is increased. When SW pin voltage is reached the SW OVP threshold the LV52207NXB's switching converter stops switching. When the other LEDO pin voltage reaches the LEDO OVP threshold the LV52207NXB's switching converter stops switching.

- When both LED strings become open:  
If both LED strings are open, LEDO1 pin voltage and LEDO2 pin voltage are approximately ground and the boost output voltage is increased.  
When SW pin voltage is reached the SW OVP threshold the LV52207NXB's switching converter stops switching.

### Over Current Protection

Current limit value for built-in power MOS is around 1.5 A. The power MOS is turned off for each switching cycle when peak drain current exceeds the limit value.

### Under Voltage Lock Out (UVLO)

UVLO operation works when VIN terminal voltage is below 2.2 V.

### Thermal Shutdown

When chip temperature is too high, boost converter is stopped.

APPLICATION CIRCUIT DIAGRAMS

PWM Dimming Mode – EN pin can be used to enable or disable

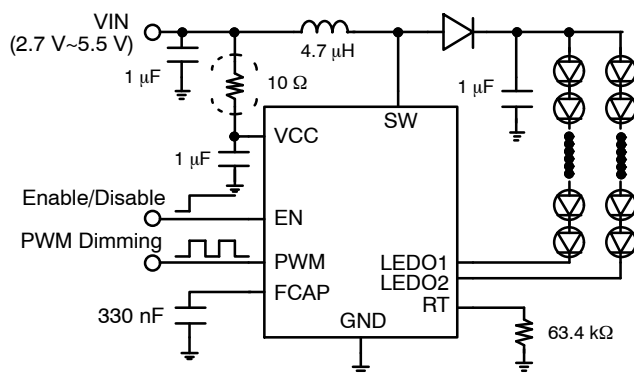


Figure 9.

PWM Dimming Mode – PWM pin can be used to enable or disable

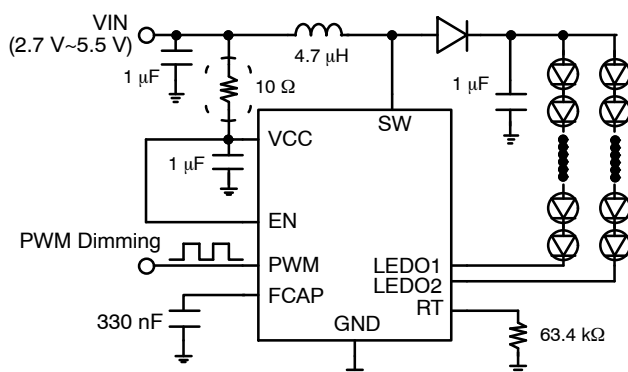


Figure 10.

1-wire Dimming Mode – PWM pin can be used to enable or disable

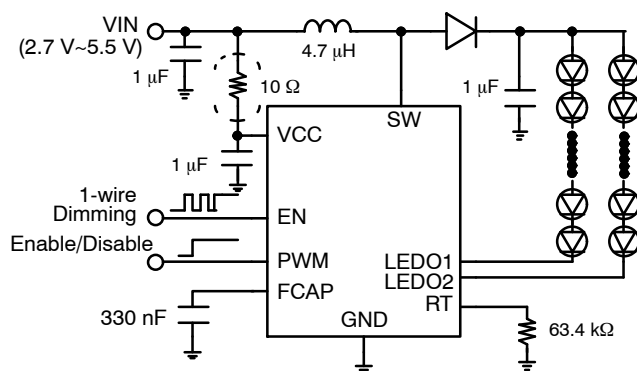


Figure 11.

APPLICATION CIRCUIT DIAGRAMS (Continued)

1-wire Dimming Mode – EN pin can be used to enable or disable

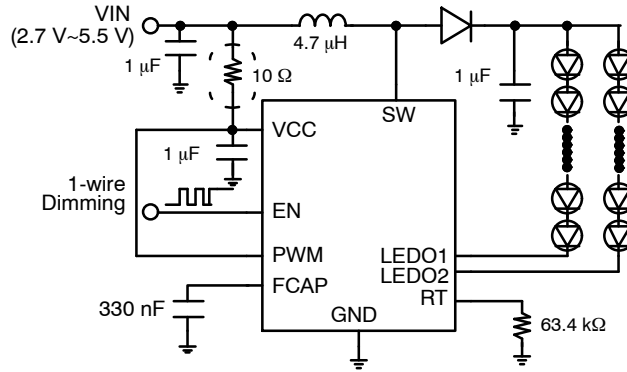


Figure 12.

1-wire Dimming Mode and PWM Dimming Mode (CABC)

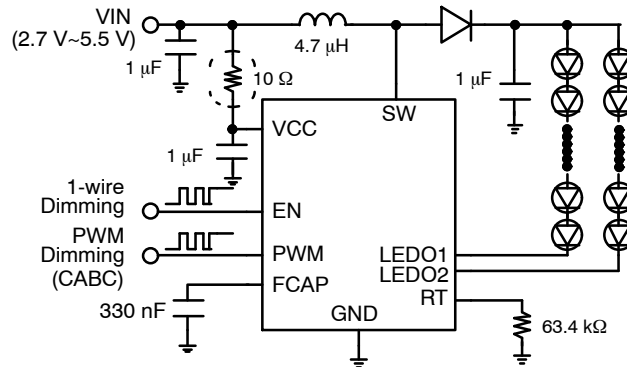


Figure 13.

**Note: Start-up Sequence**

During Tw0 period of 1-wire, it is necessary to hold PWM “High”.

TYPICAL CHARACTERISTICS

( $V_{IN} = 3.6\text{ V}$ ,  $L = 10\ \mu\text{H}$ ,  $T = 25^\circ\text{C}$ , unless otherwise specified. Note: "4s2p" means 2 strings of 4 series LEDs per string)

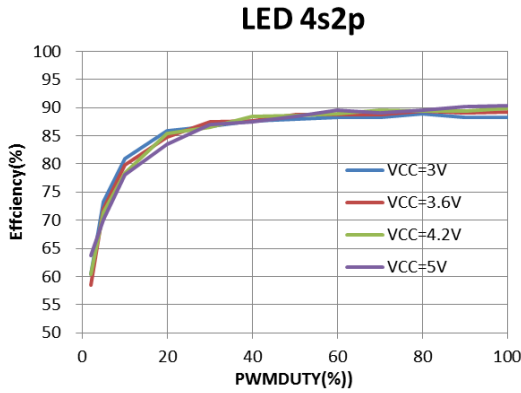


Figure 14. Efficiency vs. PWM Dimming (20 mA/String) – 4s2p

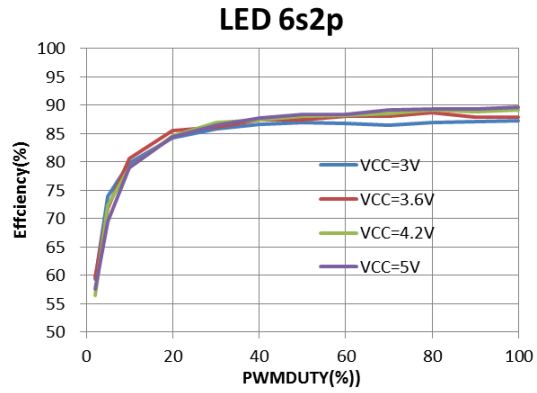


Figure 15. Efficiency vs. PWM Dimming (20 mA/String) – 6s2p

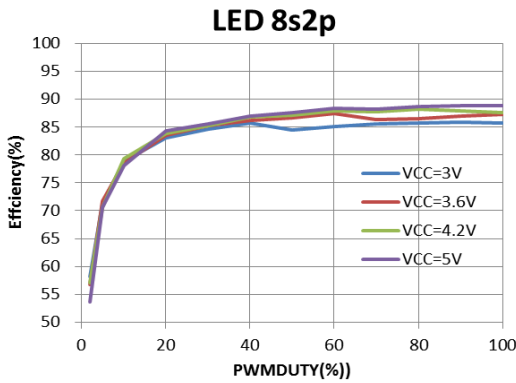


Figure 16. Efficiency vs. PWM Dimming (20 mA/String) – 8s2p

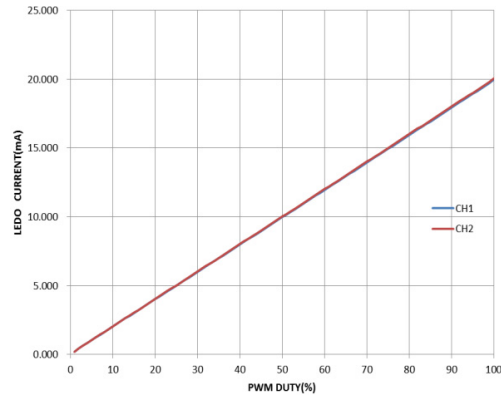


Figure 17. PWM Dimming

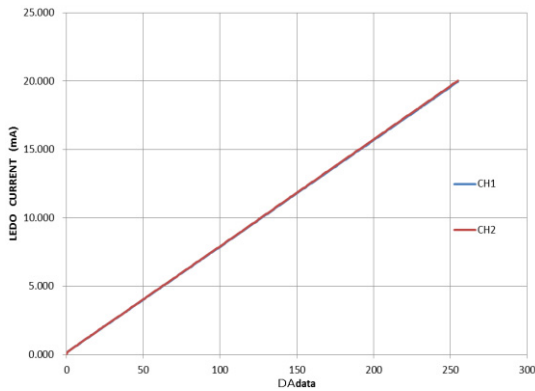


Figure 18. 1-wire Dimming

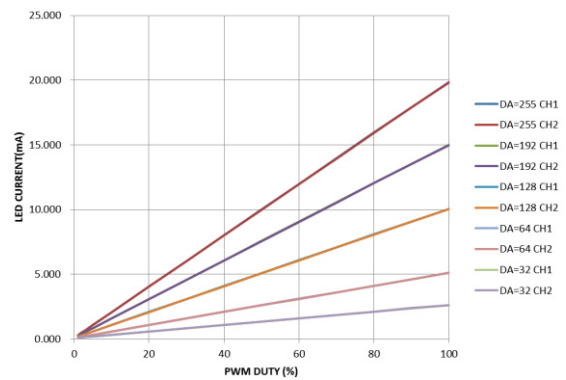


Figure 19. CABC Dimming

START UP WAVEFORMS

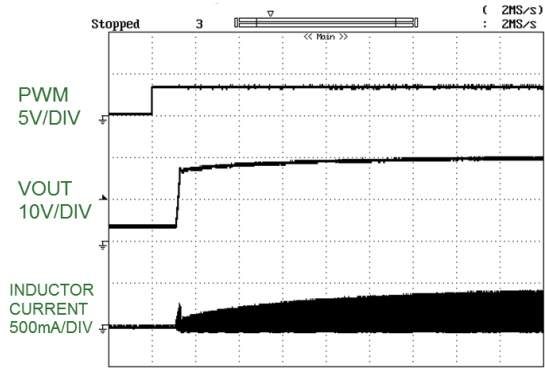


Figure 20. PWM Duty = 100%, LED 6s2p

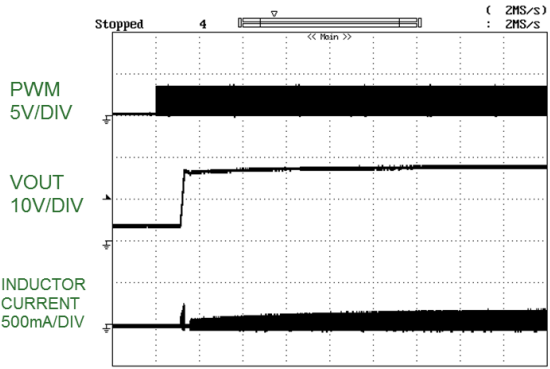


Figure 21. PWM Duty = 20%, LED 6s2p

SHUTDOWN WAVEFORMS

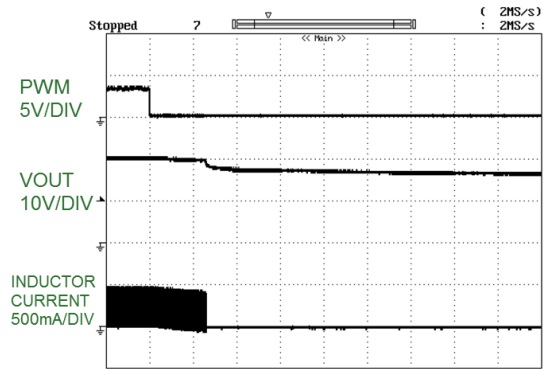


Figure 22. PWM Duty = 100%, LED 6s2p

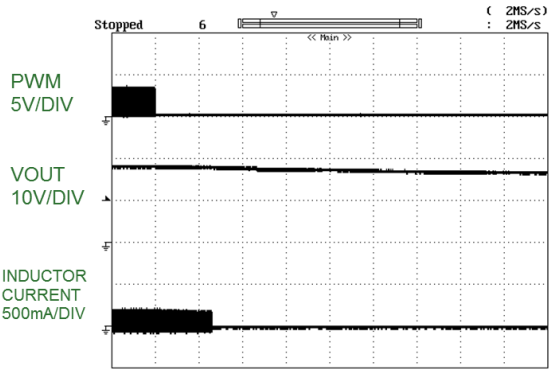


Figure 23. PWM Duty = 20%, LED 6s2p

SWITCHING WAVEFORMS

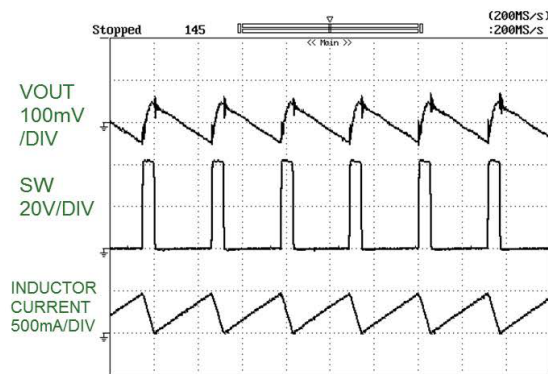


Figure 24. PWM Duty = 100%, LED 6s2p

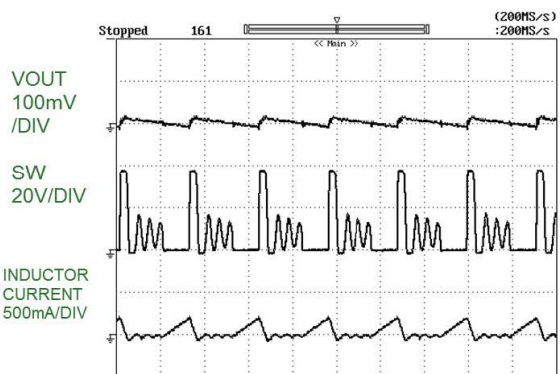


Figure 25. PWM Duty = 20%, LED 6s2p

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

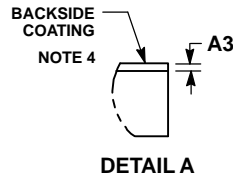
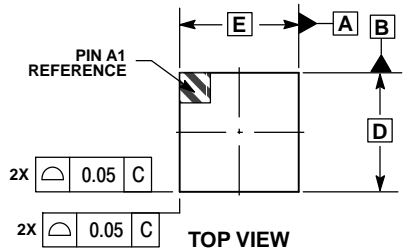
ON Semiconductor®



SCALE 4:1

WLCSP9, 1.31x1.31  
CASE 567HX  
ISSUE C

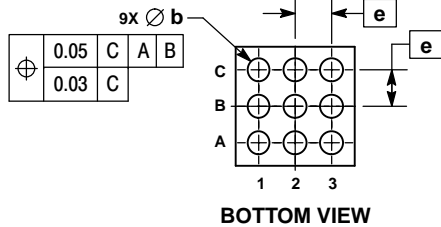
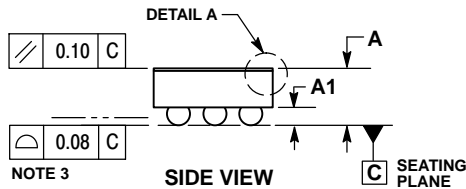
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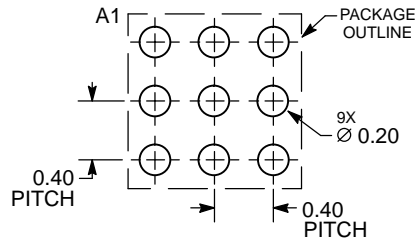
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. BACKSIDE COATING IS OPTIONAL.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.65
A1	0.16	0.26
A3	0.025 REF	
b	0.21	0.31
D	1.31 BSC	
E	1.31 BSC	
e	0.40 BSC	



**RECOMMENDED SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>NEW STANDARD:</b>		
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