Ordering number : ENA1512

SANYO Semiconductors
DATA SHEET

LV5652T — Bi-CMOS LSI 3-channel Switching Regulator Controller

Overview

The LV5652T is a 3-channel switching regulator controller.

Features

- Low-voltage (3V) operation
- Reference voltage precision : ±1%
- Independent standby functions for each of three channels.
- Is capable of driving MOS transistors.
- switching regulator controller : 3-channel
  ch1 : Supports synchronous rectification
  ch2 : Supports inverting step-up operation
  ch3 : Supports step-up operation

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CC} max	V_{CC} pin	-0.3 to 16	V
Maximum supply voltage 2	VBIAS max	VBIAS pin	-0.3 to 18	V
Maximum clock input voltage	VCLKIN max	CLKIN pin	5.5	V
Allowable power dissipation	Pd max	Mounted on a specified board*	1	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

* Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC}	V_{CC} pin	3 to 15	V
Supply voltage 2	VBIAS	VBIAS pin	3 to 15	V
Clock input voltage	VCLKIN	CLKIN pin	5	V
Timing resistor	RT		7 to 30	kΩ
Timing capacitor	CT		100 to 1000	pF
Triangle wave frequency	f_{OSC}		0.1 to 1.3	MHz

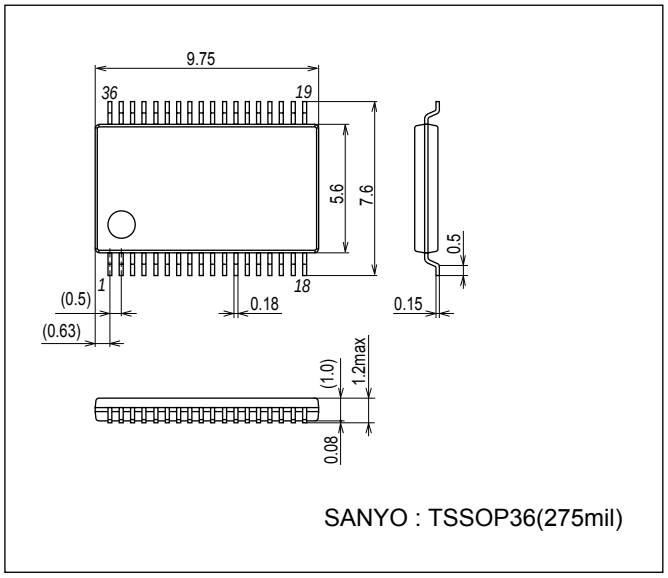
Electrical Characteristics at Ta = 25°C, V_{CC} = VBIAS = 3.6V, SCP = 0V

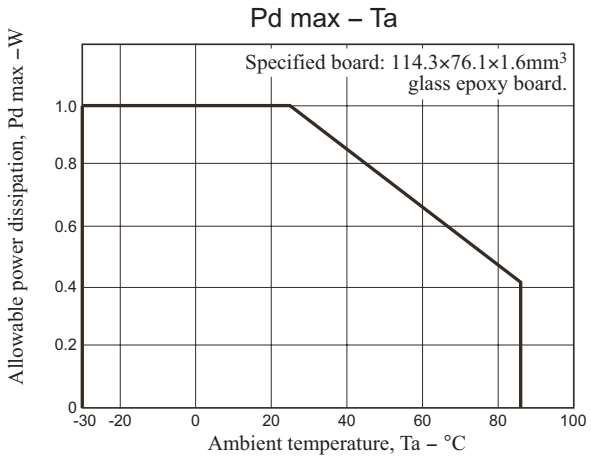
Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Error amplifier 1							
IN^+ pin internal bias voltage		VB	Value added to the error amplifier offset at the error amplifier + side voltage	0.504	0.51	0.516	V
Output low voltage	ch1 to ch3	V_{Low} FB	IN^- = 2.0V, IFB = 20μA			0.2	V
Output high voltage	ch1 to ch3	V_{Hi} FB	IN^- = 0V, IFB1 = -20μA	2.0			V
Error amplifier 2							
IN2⁻RE pin offset voltage		VOFF2		-6		6	V
Output low voltage		V_{Low} FB2RE	$IN2^-RE$ = 2.0V, IFB = 20μA			0.2	V
Output high voltage		V_{Hi} FB2RE	$IN2^-RE$ = -10V, IFB1 = -500μA	2.0			V
Protection circuit							
Threshold voltage		V_{SCP}		1.1	1.25	1.4	V
SCP pin current		I_{SCP}			4		μA
Short circuit detection signal pin		VSCPOUT	Open collector, ISCPOUT = 100μA			0.2	V
Software start block							
Soft start current	ch1 to ch3	I_{SF}	CSOFT = 0V	3.2	4	4.8	μA
Soft start resistance	ch1 to ch3	R_{SF}		160	200	240	kΩ
Fixed duty							
Maximum on duty 1	ch1	Duty MAX 1	Out monitor , IN^- = 0V	100			%
Maximum on duty 2	ch2	Duty MAX 2	Out monitor , IN^- = 0V	80	85	90	%
Maximum on duty 3	ch3	Duty MAX 3	Out monitor , IN^- = 0V	80	85	90	%
Output block							
OUT pin high side on resistance		R_{OUT} SOUR	I_O = 10mA		28	50	Ω
OUT pin low side on resistance		R_{OUT} SINK	I_O = 10mA		18	35	Ω
Triangle wave oscillator block							
Current setting pin voltage		VT RT	RT = 10kΩ		0.57		V
Output current		IOH CT			190		μA
Output current ratio		ΔIO CT	CT pin, rise/fall	2	2.5	3	-
Oscillation frequency		f_{OSC}	RT = 10kΩ , CT = 270pF	390	510	620	kHz
Reference voltage block							
Reference voltage		VREF			1.240		V
Line regulation		V_{LN} REF	V_{CC} = 3V to 15V			10	mV
Control circuit							
On state voltage		V_{ON} CTL		2.0			V
OFF state voltage		V_{OFF} CTL				0.6	V
Pin input current		I_{IN} CTL				60	μA
Standby circuit							
On voltage		V_{ON} STBY		2.0			V
OFF voltage		V_{OFF} STBY				0.6	V
Pin input current		I_{IN} STBY				60	μA
All circuits							
V_{CC} current consumption		I_{CC}	$IN1^-$ to $IN3^-$ = 1V		4	5	mA
Standby mode current consumption		I_{OFF}	VSTBY = VCTL = 0V, $I_{OFF} = I_{CC} + I_{BIAS}$			1	μA

Package Dimensions

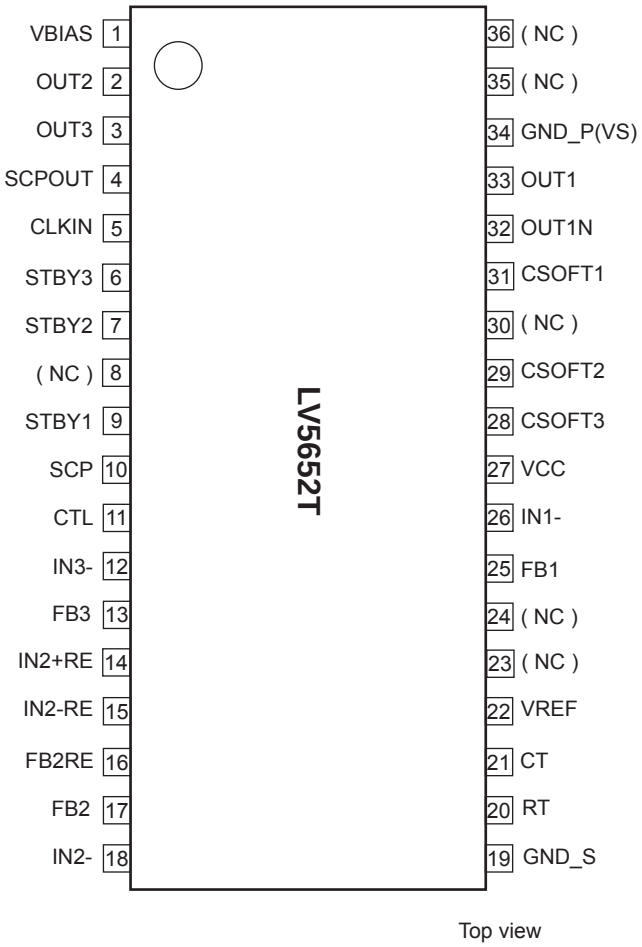
unit : mm (typ)

3253B



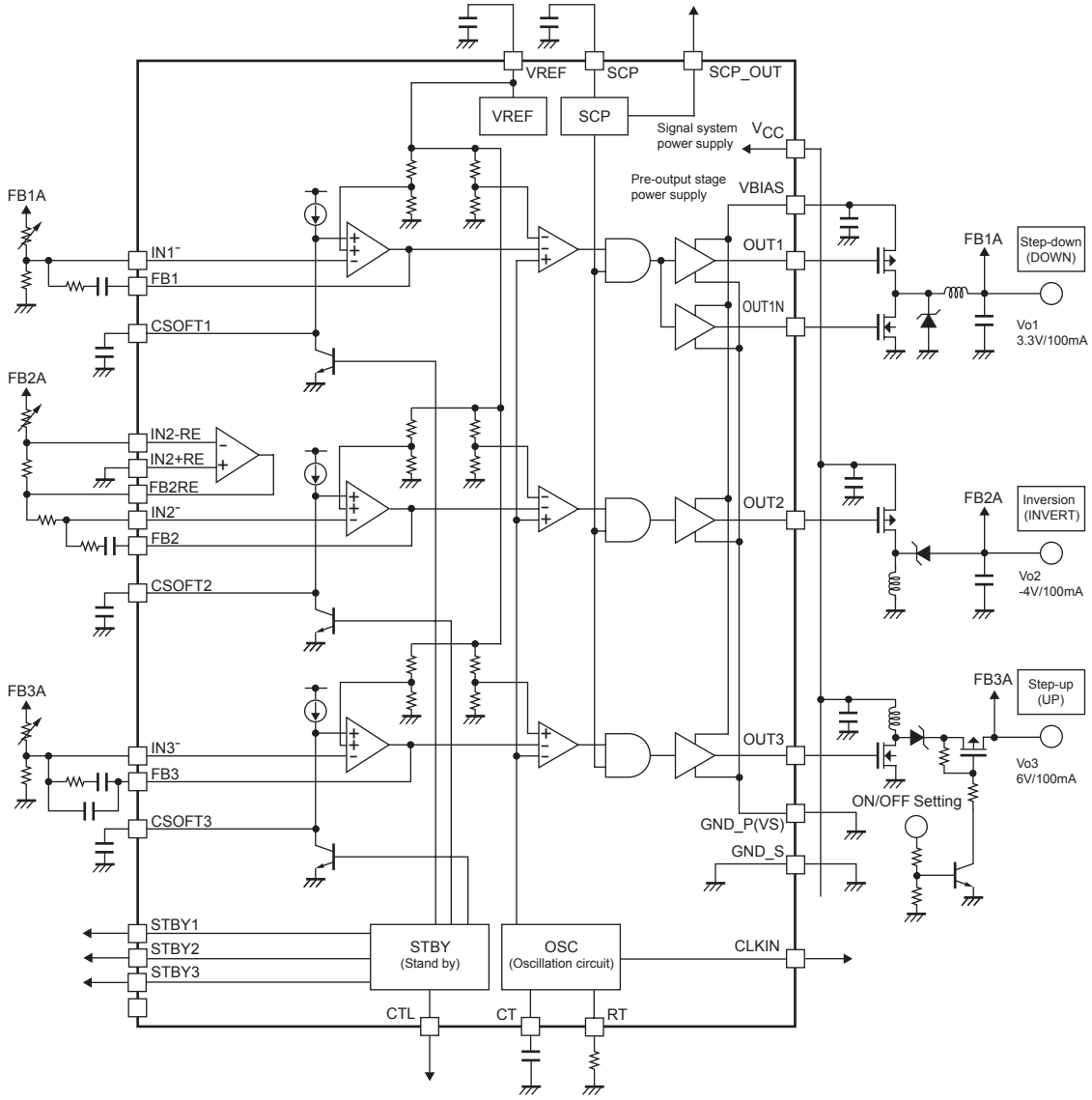


Pin Assignment



Top view

Block Diagram and Sample Application Circuit

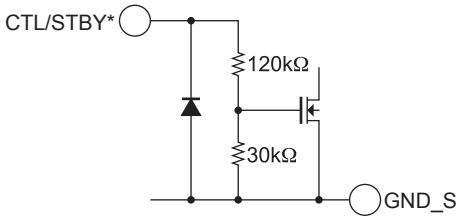
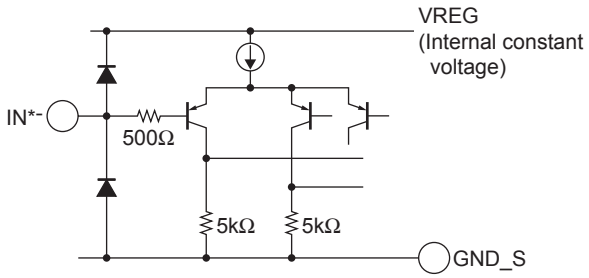
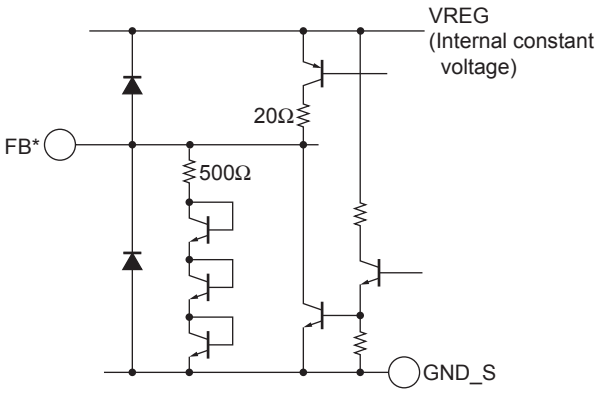
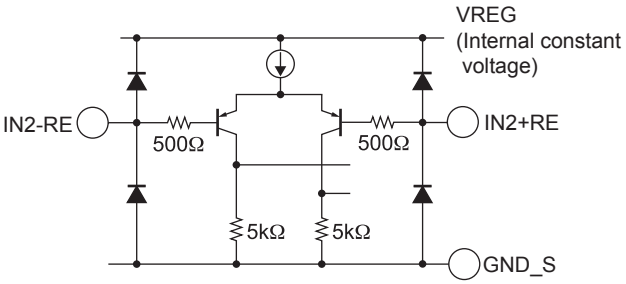
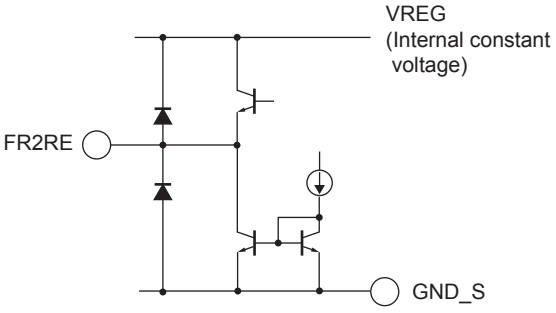


The CLKIN pin must be connected to GND,when the external clock synchronization (CLKIN) is not used.

Pin Function

Block	Pin No.	Pin Name	Functions
ch1 (Step-down)	9	STBY1	Standby input. H/ch1 ; ON, L/ch1 ; OFF.
	26	$IN1^-$	Error amplifier Inverting input.
	25	FB1	Error amplifier output.
	31	CSOFT1	Soft start setting capacitor connection. Connect to GND through a capacitor.
	33	OUT1	Output. External transistor P-channel gate connection.
	32	OUT1N	Output. External transistor N-channel gate connection.
ch2 (Inversion)	7	STBY2	Standby input. H/ch2 ; ON, L/ch2 ; OFF.
	14	$IN2^+RE$	Inversion amplifier, +(noninverting) input.
	15	$IN2^-RE$	Inversion amplifier, -(Inverting) input.
	16	FB2RE	Inversion amplifier output.
	18	$IN2^-$	Error amplifier, - (Inverting) input.
	17	FB2	Error amplifier output.
	29	CSOFT2	Soft start setting capacitor connection. Connect to GND through a capacitor.
	2	OUT2	Output. External transistor P-channel gate connect.
ch3 (Step-up)	6	STBY3	Standby input. H/ch3 ; ON, L/ch3 ; OFF.
	12	$IN3^-$	Error amplifier, - (Inverting) input.
	13	FB3	Error amplifier output.
	28	CSOFT3	Soft start setting capacitor connection. Connect to GND through a capacitor.
	3	OUT3	Output. External transistor N-channel gate connect.
POWER	27	V_{CC}	Power supply input (signal system).
	1	VBIAS	Power supply input (pre-output stage).
	19	GND_S	Ground (signal system).
	34	GND_P (VS)	Ground (pre-output stage).
	22	VREF	Reference voltage output.
CONTROL	11	CTL	Output control.
	10	SCP	Connection pin for the delay time setting capacitor of short circuit detection circuit.
	4	SCPOUT	SCP_OUT pin (SCP output).
OSC	21	CT	Triangle wave oscillation frequency setting capacitor connection.
	20	RT	Triangle wave oscillation frequency setting resistor connection.
	5	CLKIN	External clock input.
OTHER	8	(NC)	Not use.
	23	(NC)	Not use.
	24	(NC)	Not use.
	30	(NC)	Not use.
	35	(NC)	Not use.
	36	(NC)	Not use.

Equivalent Circuits

Pin No.	Pin Name	Description	Equivalent Circuit
11 9 7 6	CTL STBY1 STBY2 STBY3	CTL : Controls operation of all circuits. STBY* : Independently controls operation of the corresponding channel. Operation is high active. High : ON Low : OFF	
26 18 12	$IN1^-$ $IN2^-$ $IN3^-$	Error amplifier inverting input. The regulator output is divided by a resistor and connected to $IN*^-$	
25 17 13	FB1 FB2 FB3	Error amplifier output. These pins, in combination with $IN*^-$, configure the error amplifier filters	
14 15	$IN2^+RE$ $IN2^-RE$	Inversion step-up (Channel2) error amplifier input. These pins, in combination with FB2RE,configure the operational amplifier (independent)	
16	FB2RE	Inversion step-up (Channel2) error amplifier output. This pin, in combination with $IN2^+RE$ and $IN2^-RE$, configures the operational amplifier (independent)	

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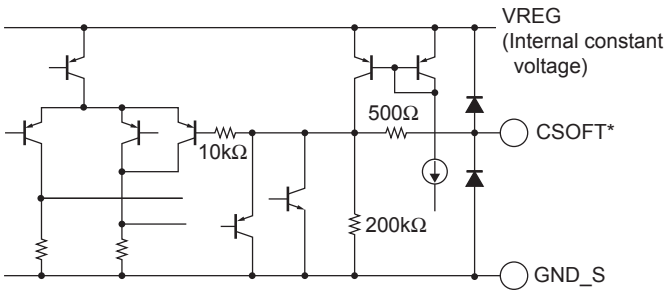
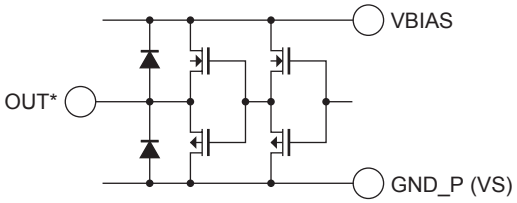
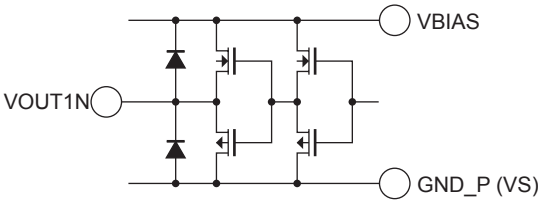
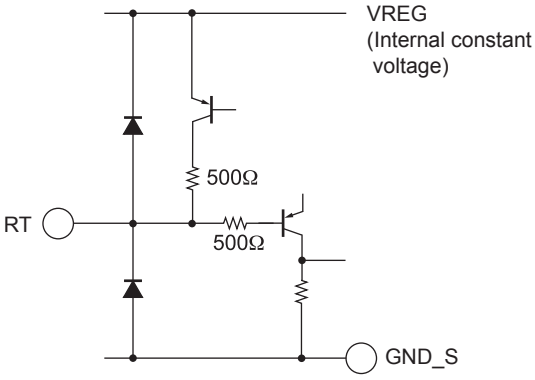
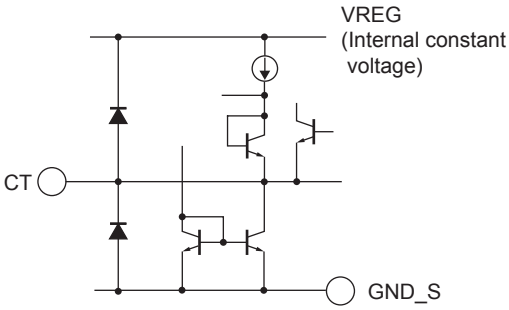
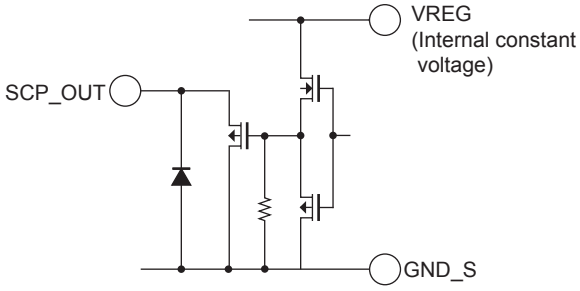
Pin No.	Pin Name	Description	Equivalent Circuit
31 29 28	CSOFT1 CSOFT2 CSOFT3	Soft start. Connect to GND via a capacitor to set the soft start time.	
33 2 3	OUT1 OUT2 OUT3	Output. Connect external PchFET.	
32	OUT1N	Output. Connect external NchFET.	
20	RT	Connect to GND through a resistor. This pin, together eith CT, sets the oscillation frequency.	
21	CT	Connect to GND through a capacitor. This pin, together eith RT, sets the oscillation frequency.	
4	SCP_OUT	Short circuit detection circuit output. When SCP exceeds the threshold voltage, the open collector goes OFF and this pin goes High.	

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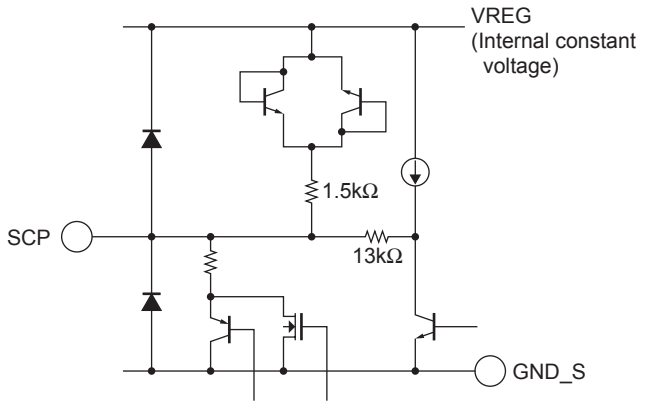
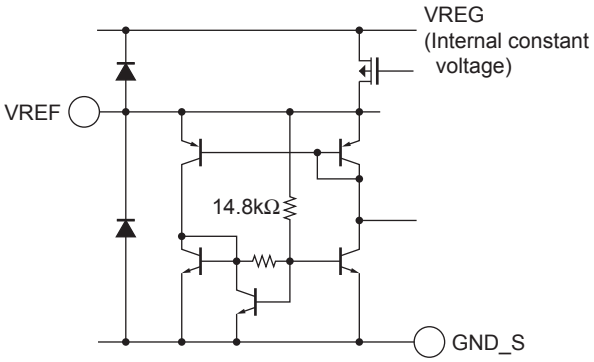
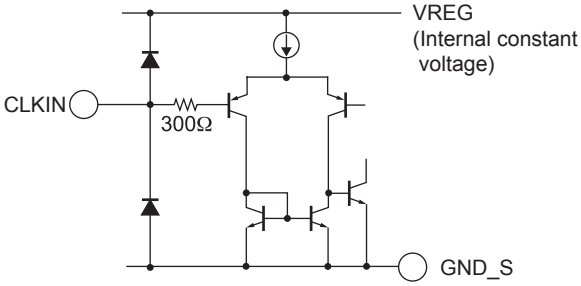
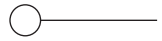
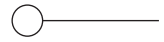
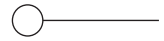
Pin No.	Pin Name	Description	Equivalent Circuit
10	SCP	Connect to GND via a capacitor to set the short circuit detection circuit delay time.	
22	VREF	Internal constant voltage circuit output. Connect a stabilizing capacitor.	
5	CLKIN	External clock input. Apply an external clock of the internal oscillation frequency or higher.	
27	V_{CC}	Signal system power supply	
1	VBIAS	Power system power supply (Output stage)	
19	GND_S	Signal system GND	
34	GND_P (VS1)	Output stage GND (pre-stage)	
8 23 24 30 35 36	(NC) (NC) (NC) (NC) (NC) (NC)	Use prohibited. (Not connect pins.)	

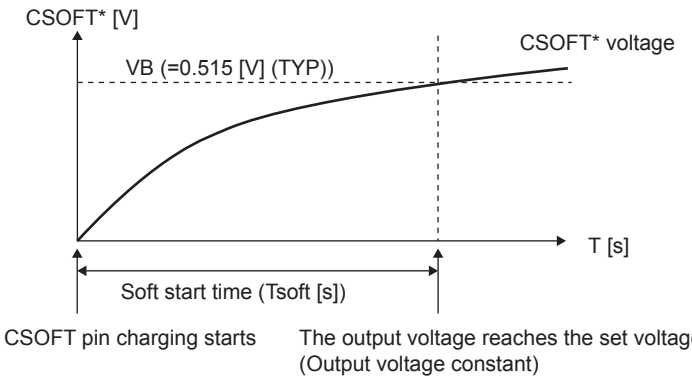
Notes

(1) Soft start time setting method

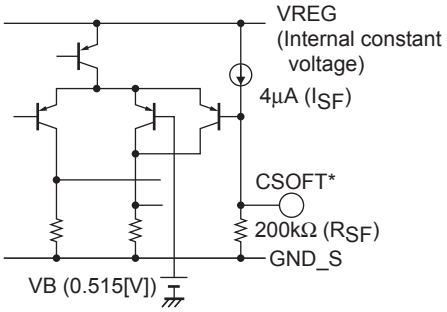
The soft start time is set with the capacitor connected between CSOFT* and GND_S.

This IC has an independent soft start function for each channel, so a capacitor must be connected for each CSOFT to set the soft start time.

(Description of soft start operation)



(Outline of soft start pin)



$$T_{SOFT} = C_{SOFT} \times R_{SF} \ln\left(\frac{VB}{R_{SF} \times I_{SF}}\right)$$

$$= 0.206 \times 10^{6} \times C_{SOFT}\ [s]$$

(2) Setting the oscillation frequency

The internal oscillation frequency is set by the resistor connected to the RT pin and the capacitor connected to the CT pin. The waveform generated on CT is a triangular wave with the charging/discharging waveform determined by RT and CT.

$$f_{OSC} = 1.32 \times \frac{1}{CT \times RT}\ [Hz]$$

The actual internal oscillation frequency deviates from the calculated value due to overshoot, undershoot and other factors, so the frequency should be confirmed in an actual set.

(3) External input CLK function (CLK_IN)

Switching operation can be synchronized with external clock input (CLK_IN) by using the CLK_IN pin.

- External clock (CLK_IN) frequency and input level

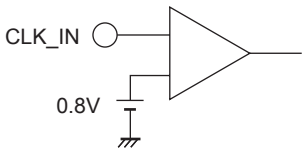
  When using external clock (CLK_IN) input, input a frequency equal to the internal oscillation frequency +20% or more to CLK_IN. In addition, the CLK_IN configuration is shown in the figure “CLK_IN (input) equivalent circuit (outline)” below.

  The 0.8V reference voltage and CLK_IN are compared to determine the edges, so input a signal of 0.8V or more (V_{CC} voltage or less) as the external clock (CLK_IN).
- External/internal clock switching

  Set the CTL pin Low before switching between the external clock and the internal clock. Switching clocks when running may give rise to output voltage fluctuations.
- Maximum ON duty

  The maximum ON duty (Duty_MAX*) of channel 2 to channel 3 is the 85% (typ.) setting. When using the external clock (CLK_IN), the maximum ON duty (Duty_MAX*) becomes smaller, so care must be taken for the set output voltage.

(CLK_IN (input) equivalent circuit (outline))



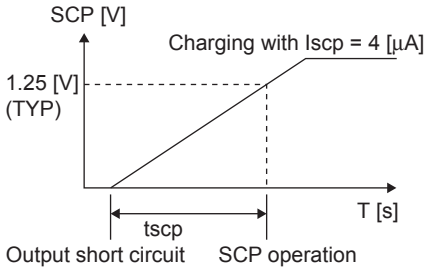
(4) SCP (short circuit protection) function

• Description of operation

When any one of FB1 to FB4 goes High due to the load being shorted or other reason, charging to the SCP pin starts. If output does not recover during the set time Tscp and SCP pin voltage exceeds the threshold voltage, the protective circuit (SCP) operates and all channel outputs are turned OFF. All outputs are latched off by the protection circuit (SCP). This latched state (output OFF) is canceled by setting the CTL pin Low or by turning the power supply OFF. When not using the protection function (SCP), the SCP pin must be shorted to GND_S with a line that is as short as possible.

The SCP operation time is set by the capacitor connected to the SCP pin.

(SCP charging operation)



(SCP function)