LV5680P

Multi Voltage Regulator IC Application Note

ON Semiconductor®

Overview

The LV5680P is a multiple voltage regulator for car audio system. This IC has 4 voltage regulators and 2 high-side switches.

The following protection circuits are integrated: over current limiter, overvoltage protection and Thermal Shut Down. This IC is most suitable Car Audio.

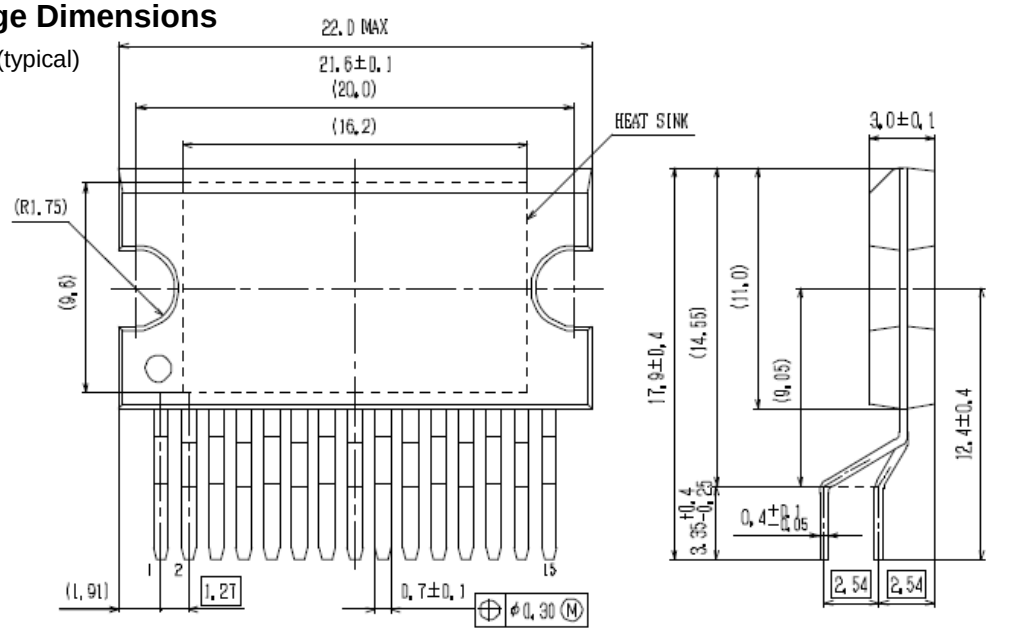
Features

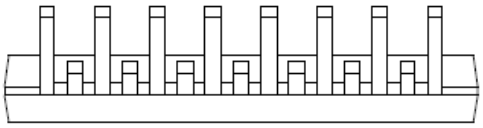
- 4 LDO regulators
  - For VDD: Vout is 5.0V, Iomax is 200mA
  - For CD: Vout is 8.0V, Iomax is 1300mA
  - For Illumination: Vout is 8V to 12V(Adjustable external resistors), Iomax is 300mA
  - For Audio: Vout is 8V to 9V(Adjustable external resistors), Iomax is 300mA
- 2 High-side Switches
  EXT：Voltage difference between input and output is 0.5V, Iomax is 350mA
  ANT：Voltage difference between input and output is 0.5V, Iomax is 300mA
- 2 Switches connected to “VDD”
  SW5V：Voltage difference between “VDD” and output is 0.2V, Iomax is 200mA
  ACC(Accessory Voltage Detector output)：Voltage difference between “VDD” and output is 0.2V, Iomax is 100mA
- Over Current Limiting
- Overvoltage Protection (Without VDD-OUT) *Detection voltage is 21V(typical)
- Thermal Shut Down *175℃(typical)
- ACC voltage detector
- Maximum surge peak Voltage is 50V
- Low thermal resistance package “HZIP15J”(θ jc=2℃/W)

(Warning) The protector functions only improve the IC’s tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under overcurrent protection range or thermal shutdown state may degrade the IC’s reliability and eventually damage the IC.

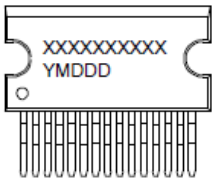
Package Dimensions

unit : mm(typical)





GENERIC MARKING DIAGRAM*



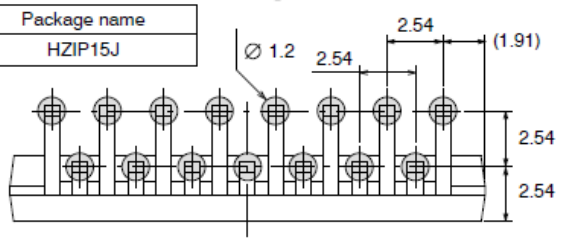
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

SOLDERING FOOTPRINT*

(Unit: mm) Through Hole Area

Package name
HZIP15J



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Fig1. Package Dimensions of HZIP15J

• Allowable power dissipation derating curve

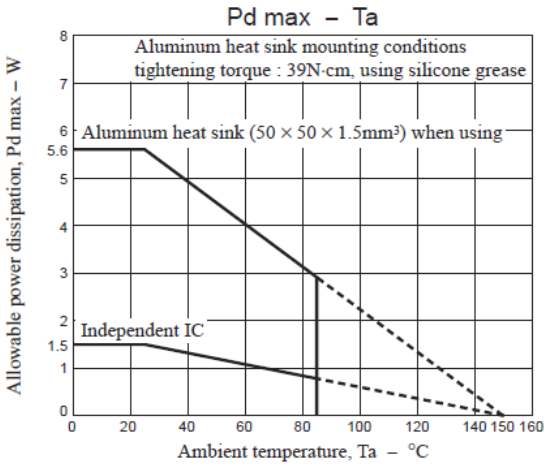


Fig2. Allowable Power Dissipation Derating Curve

Pin Assignment

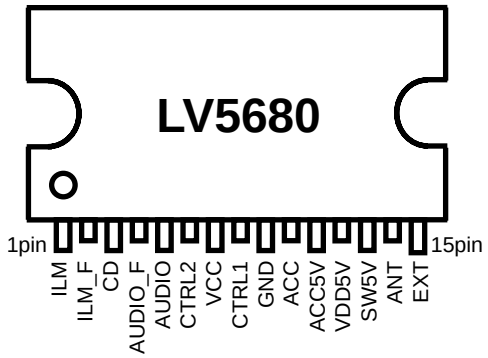


Fig3. Pin Assignment

Block Diagram

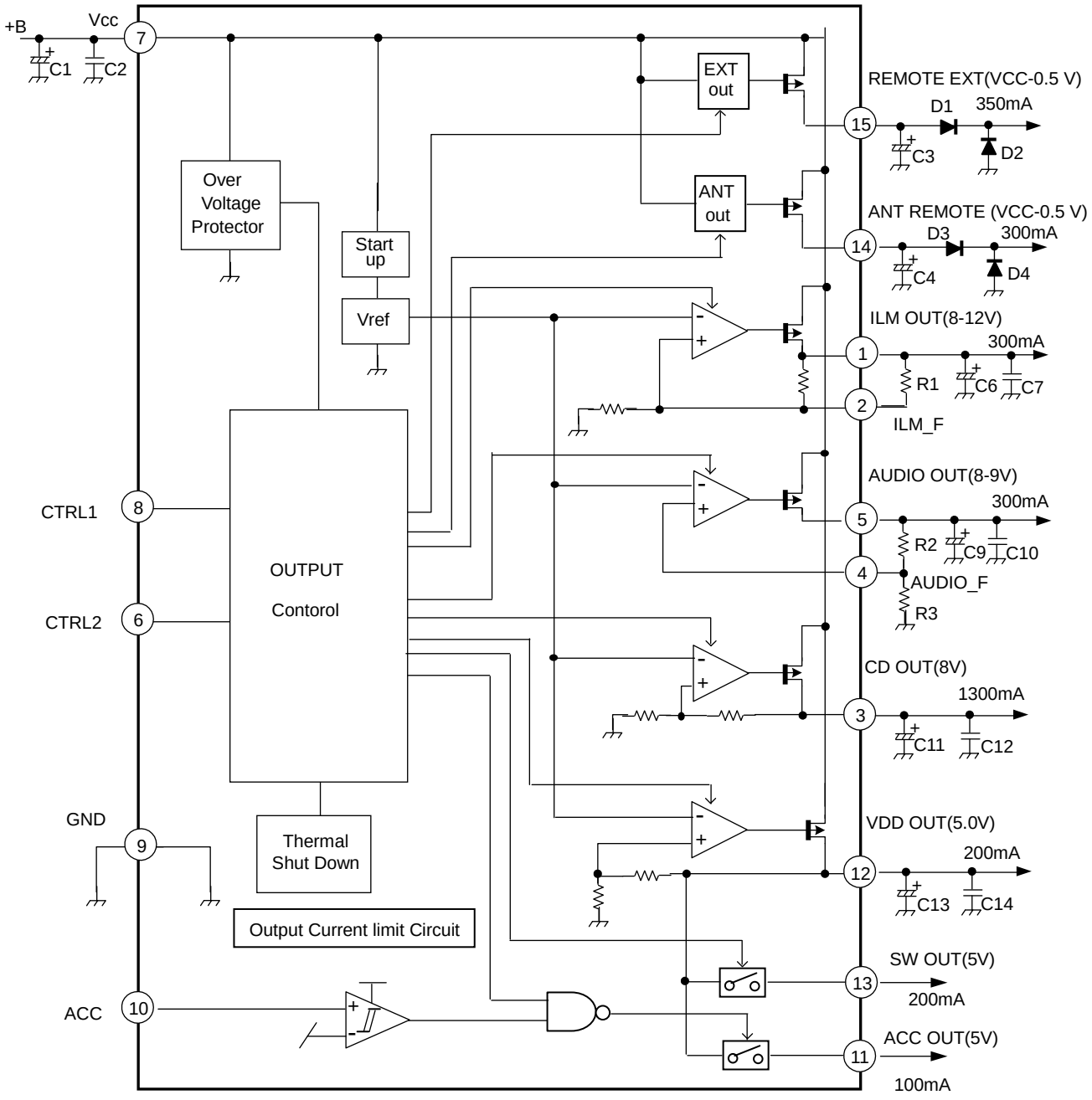


Fig4. Block Diagram of LV5680P

Specifications

Absolute Maximum Ratings at Ta=25 °C

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	Vcc max			36	V
Power dissipation	Pd max	Without heat sink	Ta≦25 °C	1.5	W
		At using Al heat sink(*1)		5.6	
		At heat sink of infinite area		32.5	
Peak voltage	Vcc peak	Regarding Bias wave, refer to below the pulse.		50	V
Operating temperature	Topr			-40 to +85	℃
Storage temperature	Tstg			-55 to +150	℃
Junction temperature	Tjmax			150	℃

*1：When the Aluminum heat sink(50mm×50mm×1.5mm) is used

・Peak Voltage testing pulse wave

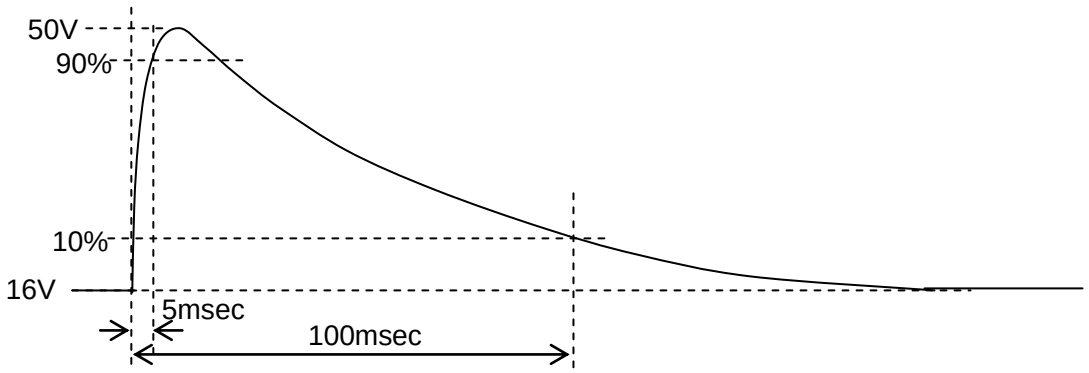


Fig5. Peak Voltage testing pulse wave

Allowable Operating Range at Ta=25 °C

Parameter	Conditions	Range	Unit
Power supply voltage range1	VDD output, SW output, ACC output	7.5 to 16	V
Power supply voltage range2	ILM output at 10V	12 to 16	V
	ILM output at 8V	10 to 16	V
Power supply voltage range3	AUDIO output at 9V	10 to 16	V
Power supply voltage range4	CD output(CD output current =1.3A)	10.5 to 16	V
	CD output(CD output current ≦1A)	10 to 16	V

Electrical Characteristics at Ta=25 °C, Vcc=14.4V (*2)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Current	Icc	VDD No Load,CTRL1/2=「L/L」,ACC=0V		400	800	μA
CTRL1 Input						
“L” Input voltage	$V_{IL}1$		0		0.5	V
“M1” Input voltage	$V_{IM1}1$		0.8	1.1	1.4	V
“M2” Input voltage	$V_{IM2}1$		1.9	2.2	2.5	V
“H” Input voltage	$V_{IH}1$		2.9	3.3	5.5	V
Input impedance	$R_{IN}1$		350	500	650	kΩ
CTRL2 Input						
“L” Input voltage	$V_{IL}2$		0		0.5	V
“M” Input voltage	$V_{IM}2$		1.1	1.65	2.1	V
“H” Input voltage	$V_{IH}2$		2.5	3.3	5.5	V
Input impedance	$R_{IN}2$		350	500	650	kΩ
VDD5V output (*3)				**VDD5V supplies a current to SW5V and ACC5V**		
Output voltage1	Vo1	Io1= 200 mA, Io7,Io8=0A	4.75	5.0	5.25	V
Output voltage2	Vo1’	Io1=200mA, Io7=200mA, Io8=100mA	4.75	5.0	5.25	V
Output total current	Ito1	Vo1≧4.75V, Ito1=Io1+Io7+Io8	500			mA
Line regulation	$\Delta Vo_{LN}1$	7.5V<Vcc<16 V, Io1= 200 mA(*4)		30	90	mV
Load regulation	$\Delta Vo_{LD}1$	1 mA<Io1<200 mA(*4)		70	150	mV
Dropout voltage 1	$V_{DROP}1$	Io1= 200 mA(*4)		1.0	1.5	V
Dropout voltage 2	$V_{DROP}1$’	Io1= 100 mA(*4)		0.7	1.05	V
Dropout voltage 3	$V_{DROP}1$’’	Io1+Io7+Io8= 500 mA		2.5	3.75	V
Ripple rejection	$R_{REJ}1$	f=120Hz, Io1= 200 mA(*4)	40	50		dB
CD-ON；**CTRL2=“H”**						
Output voltage	Vo2	Io2= 1000 mA	7.6	8.0	8.4	V
Output current capacity	Io2	Vo2≧7.6V	1300			mA
Line regulation	$\Delta Vo_{LN}2$	10.5V<Vcc<16V, Io2=1000mA		50	100	mV
Load regulation	$\Delta Vo_{LD}2$	10 mA<Io2<1000 mA		100	200	mV
Dropout voltage1	$V_{DROP}2$	Io2= 1000 mA		1.0	1.5	V
Dropout voltage2	$V_{DROP}2$’	Io2= 500 mA		0.5	0.75	V
Ripple rejection	$R_{REJ}2$	f=120Hz ,Io2= 1000 mA	40	50		dB
AUDIO (8-9V) -ON；**CTRL2=“M”&“H”**						
AUDIO_F voltage	V_i3		1.222	1.260	1.298	V
AUDIO_F current	$I_{IN}3$		-1		1	μA
AUDIO output voltage1	Vo3	Io3= 200 mA, R2=30kΩ,R3=5.6kΩ (*5)	7.65	8.0	8.35	V
AUDIO output voltage2	Vo3’	Io3= 200 mA, R2=27kΩ,R3=4.7kΩ (*5)	8.13	8.5	8.87	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AUDIO (8-9V) -ON ; CTRL2="M"&"H"						
AUDIO output voltage3	Vo3' '	Io3= 200 mA, R2=24kΩ,R3=3.9kΩ(*5)	8.6	9.0	9.4	V
Output current capacity	Io3		300			mA
Line regulation	$\Delta Vo_{LN}3$	10V<Vcc<16 V, Io3= 200 mA		30	90	mV
Load regulation	$\Delta Vo_{LD}3$	1 mA<Io3<200 mA		70	150	mV
Dropout voltage1	$V_{DROP}3$	Io3= 200 mA		0.3	0.45	V
Dropout voltage2	$V_{DROP}3'$	Io3= 100 mA		0.15	0.23	V
Ripple rejection	$R_{REJ}3$	f=120Hz, Io3= 200 mA	40	50		dB
ILM (8-12V) -ON ; CTRL1="M1","M2"&"H"						
ILM_F voltage	V_I4		1.222	1.260	1.298	V
ILM output voltage1	Vo4	Io4= 200 mA	11.4	12.0	12.6	V
ILM output voltage2	Vo4'	Io4= 200 mA、R1=270kΩ(*6)	8.5	10.0	11.5	V
ILM output voltage3	Vo4' '	Io4= 200 mA、R1=100kΩ(*6)	6.8	8.0	9.2	V
Output current capacity	Io4	R1 =270kΩ	300			mA
Line regulation	$\Delta Vo_{LN}4$	12V<Vcc<16V, Io4=200mA,R1=270kΩ		30	90	mV
Load regulation	$\Delta Vo_{LD}4$	1 mA<Vo4<200,mA		70	150	mV
Dropout voltage1	$V_{DROP}4$	Io4= 200 mA		0.7	1.05	V
Dropout voltage2	$V_{DROP}4'$	Io4= 100 mA		0.35	0.53	V
Ripple rejection	$R_{REJ}4$	f=120Hz ,Io4= 200 mA	40	50		dB
REMOTE(EXT)-ON ; CTRL1="M2"&"H"						
Output voltage	Vo5	Io5= 350 mA	Vcc-1.0	Vcc-0.5		V
Output current capacity	Io5	Vo5≧Vcc-1.0	350			mA
ANT Remote-ON ; CTRL1="H"						
Output voltage	Vo6	Io6= 300 mA	Vcc-1.0	Vcc-0.5		V
Output current capacity	Io6	Vo6≧Vcc-1.0	300			mA
SW5V output ; CTRL2="M"&"H"						
Output voltage1	Vo7	Io7= 1 mA, Io1,Io8= 0A(*7)	Vo1-0.25	Vo1		V
Output voltage2	Vo7'	Io7= 200 mA, Io1,Io8= 0A(*7)	Vo1-0.45	Vo1-0.2		V
Output current capacity	Io7	Vo7≧4.55	200			mA
ACC Detector ; Vout=5V coupled ACC						
ACC detection voltage	$V_{TH}8$		2.8	3.0	3.2	V
Hysteresis	$V_{HIS}8$		0.2	0.3	0.4	V
Input impedance	ZI8	Included Pull-down resistor	42	60	78	kΩ
ACC Vout1	Vo8	Io8= 0.5 mA, Io1,Io7= 0A(*7)	Vo1-0.25	Vo1		V
ACC Vout2	Vo8'	Io8= 100 mA, Io1,Io7= 0A(*7)	Vo1-0.45	Vo1-0.2		V
Output current capacity	Io8	Vo8≧4.55	100			mA

*2：The entire specification has been defined based on the tests performed under the conditions where Tj and Ta(=25℃) are almost equal. There tests were performed with pulse load to minimize the increase of junction temperature (Tj).

*3：The VDD5V output supplies the output currents of SW5V and ACC5V. Therefore, the current supply capability of the VDD5V output and its other electrical characteristics are affected by the output statuses of SW5V and ACC5V.

*4：SW5V and ACC5V outputs have no load.

*5：When a resistor tolerance ±1% is used.

<Reference> When a resistor tolerance ±0.5% is used, Vo3’ ’ is 8.67V≦9.0V≦9.33V.

*6：When a resistor tolerance ±1% is used. The absolute accuracy of the internal resistance is ±15%.

*7：Since the "SW5V" and "ACC5V" are output from "VDD5V" through the switch, each output voltage drops by an amount equivalent to the ON resistance of the switch.

True Table of CTRL

CTRL1	ANT	EXT	ILM
L	OFF	OFF	OFF
M1	OFF	OFF	ON
M2	OFF	ON	ON
H	ON	ON	ON

CTRL2	CD	AUDIO	SW5
L	OFF	OFF	OFF
M	OFF	ON	ON
H	ON	ON	ON

Timing Chart

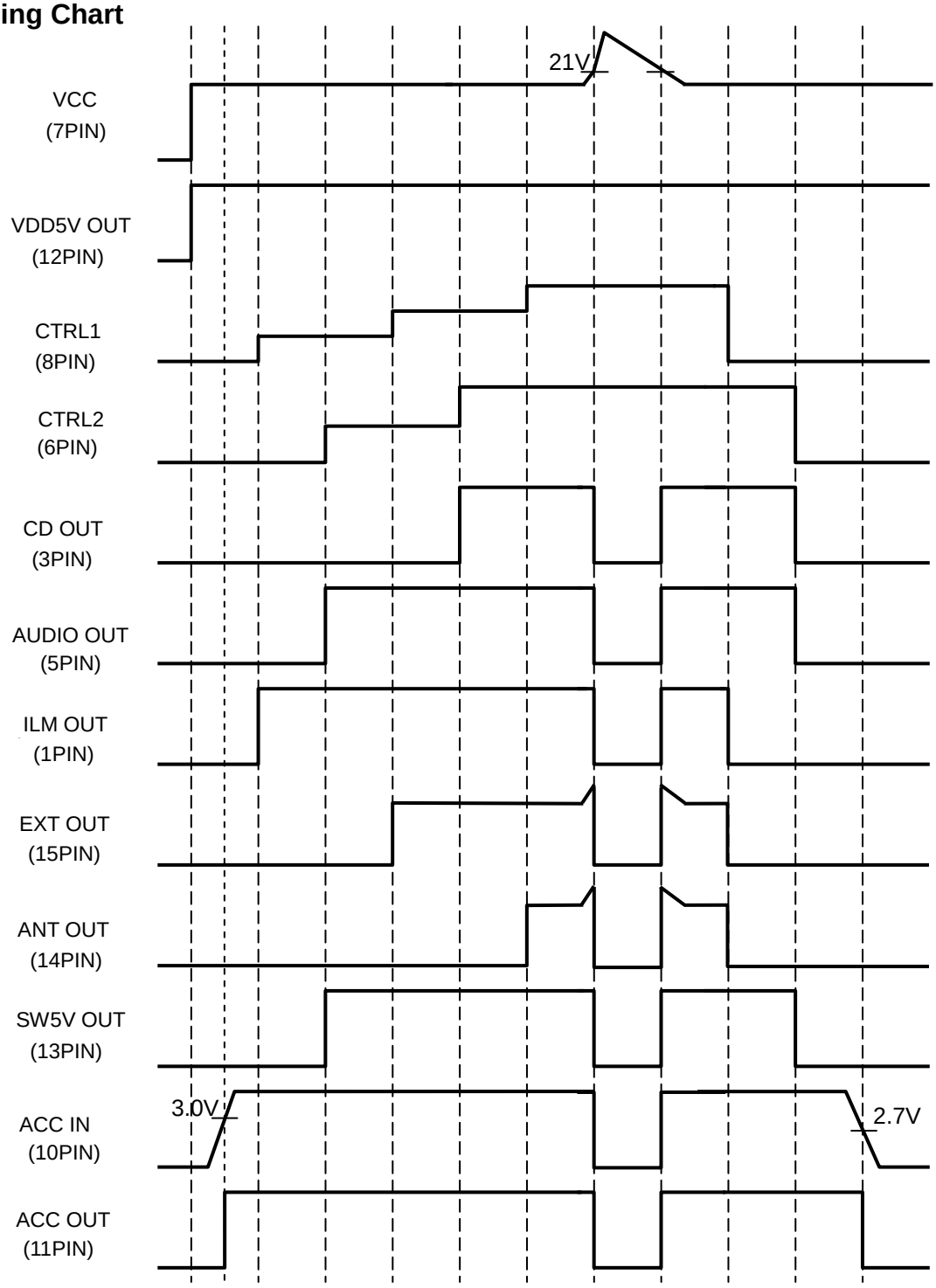


Fig6. Timing Chart

Main Characteristics

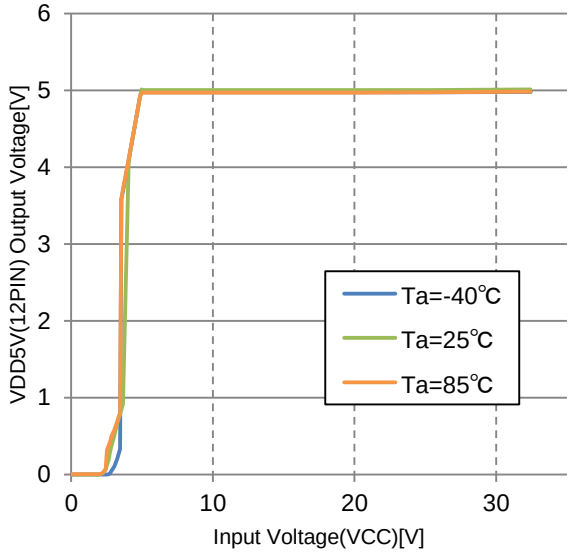


Fig7. [VDD] Vo vs. Input Voltage

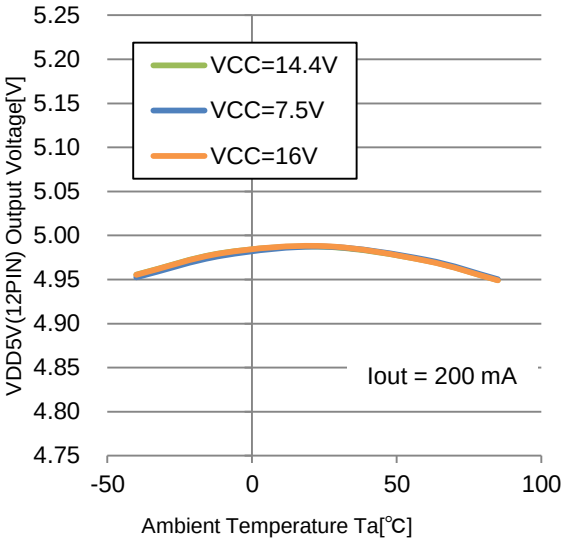


Fig8. [VDD] Vo vs. Ta

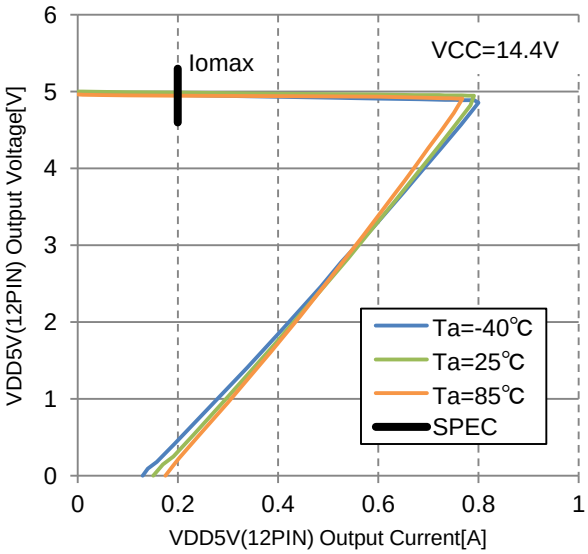


Fig9. [VDD] Vo vs. Io@VCC=14.4V

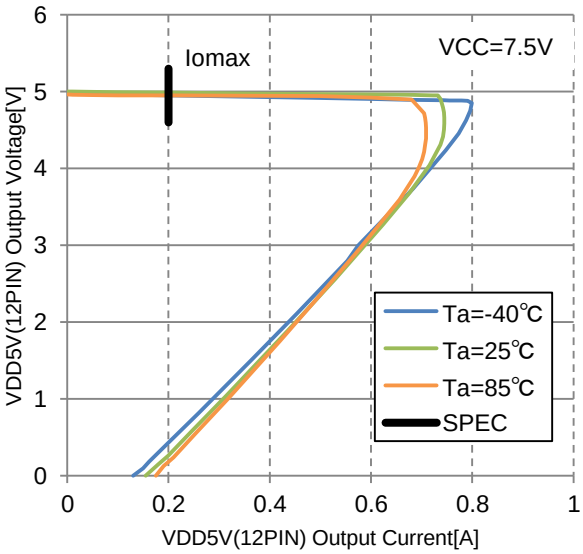


Fig10. [VDD] Vo vs. Io@VCC=7.5V

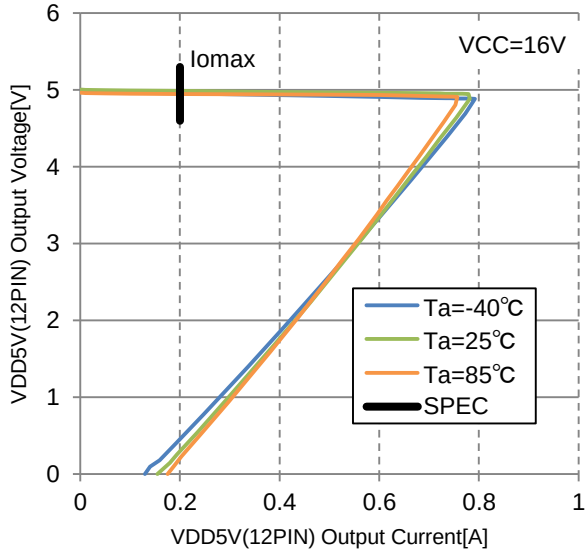


Fig11. [VDD] Vo vs. Io@VCC=16V

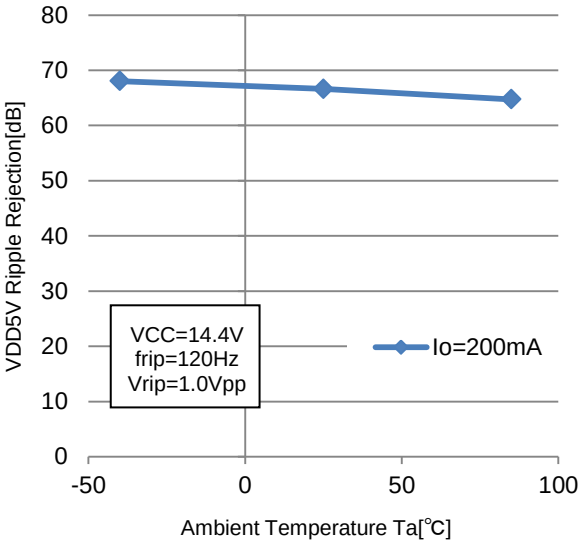


Fig12. [VDD] Ripple Rejection vs. Ta

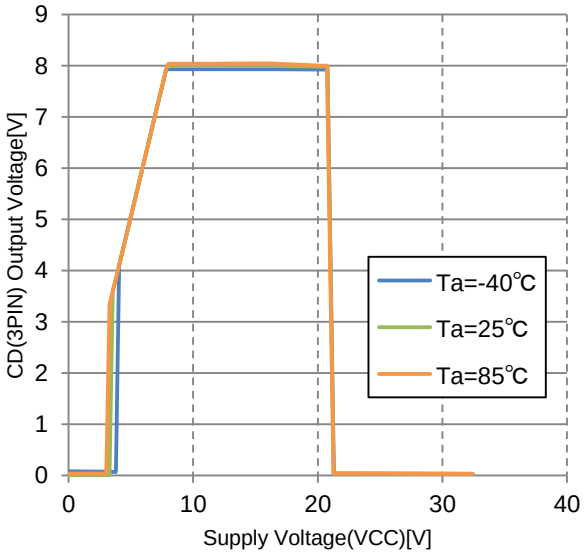


Fig13. [CD] Vo vs. Input Voltage

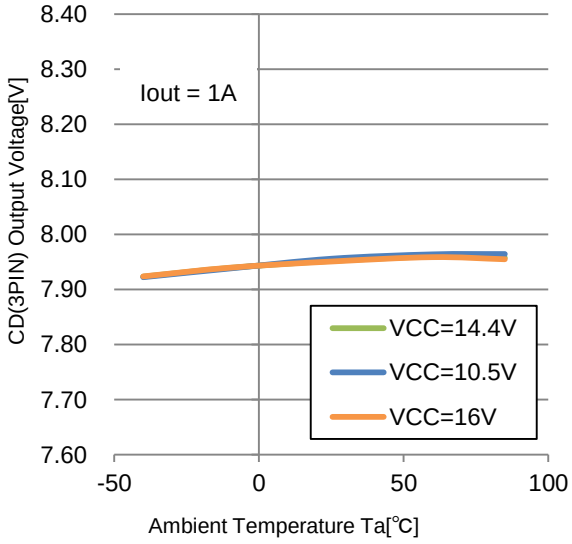


Fig14. [CD] Vo vs. Ta

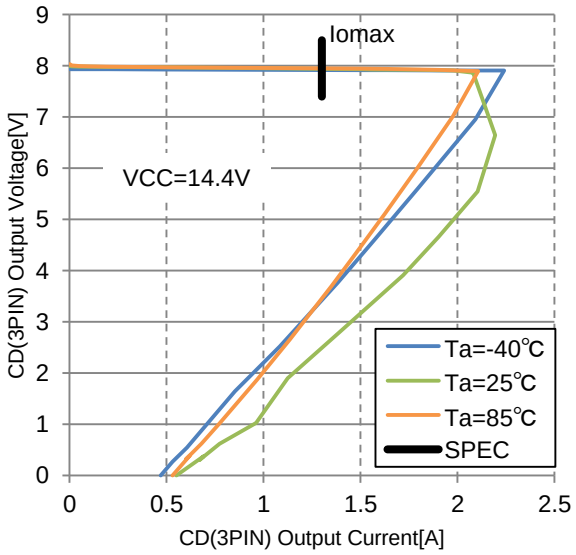


Fig15. [CD] Vo vs. Io@VCC=14.4V

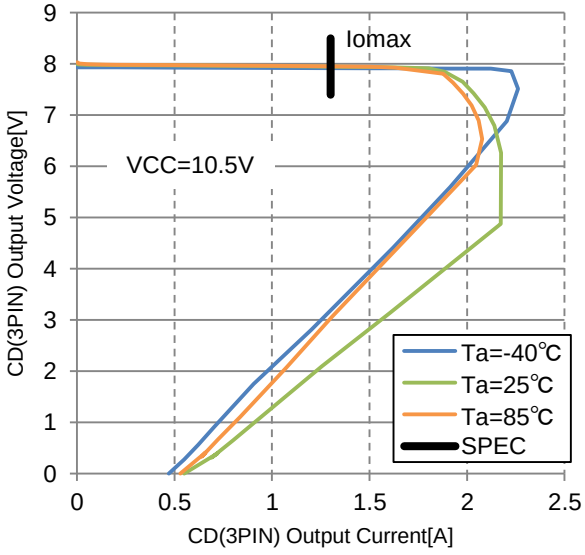


Fig16. [CD] Vo vs. Io@VCC=10.5V

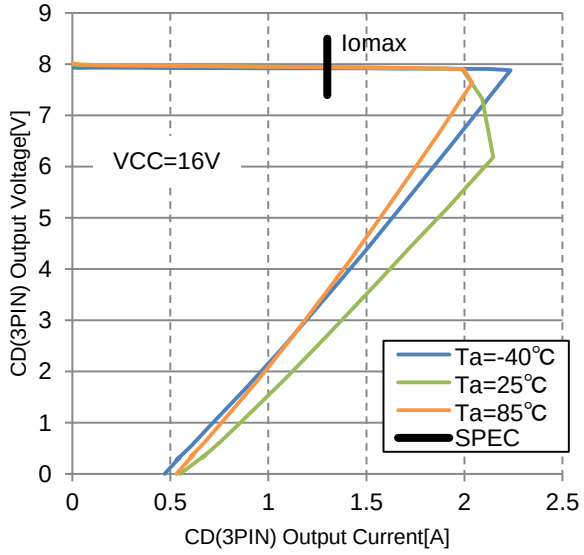


Fig17. [CD] Vo vs. Io@VCC=16V

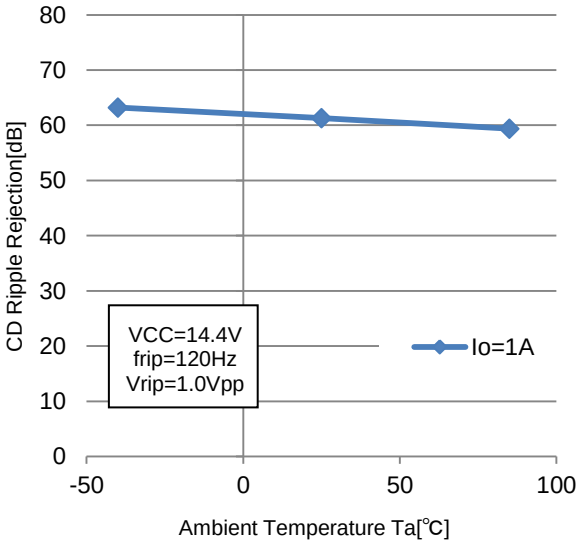


Fig18. [CD] Ripple Rejection vs. Ta

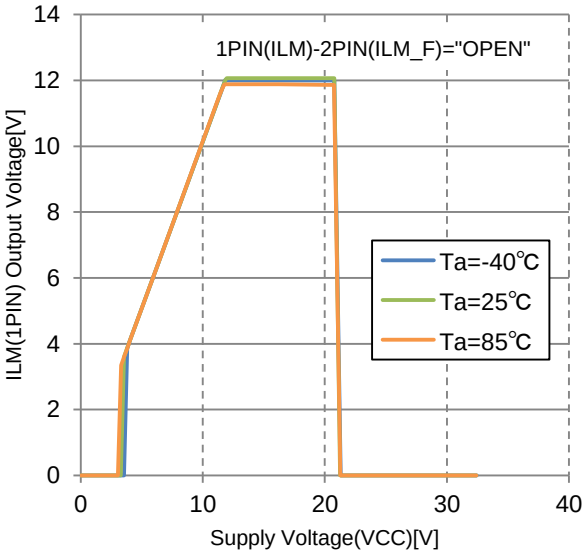


Fig19. [ILM(12V)] Vo vs. Input Voltage

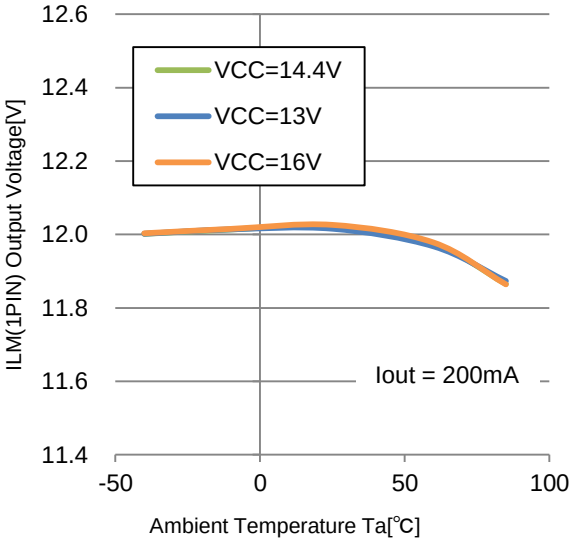


Fig20. [ILM(12V)] Vo vs. Ta

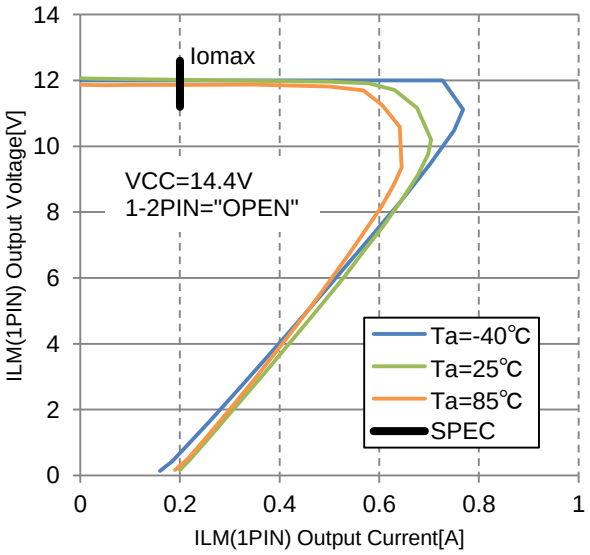


Fig21. [ILM(12V)] Vo vs. Io@VCC=14.4V

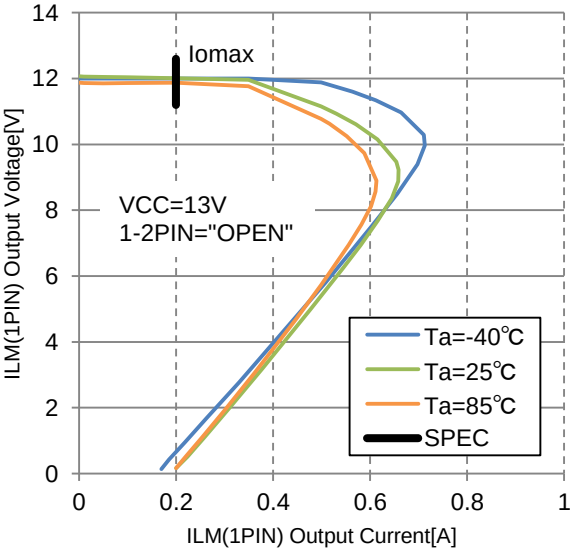


Fig22. [ILM(12V)] Vo vs. Io@VCC=13V

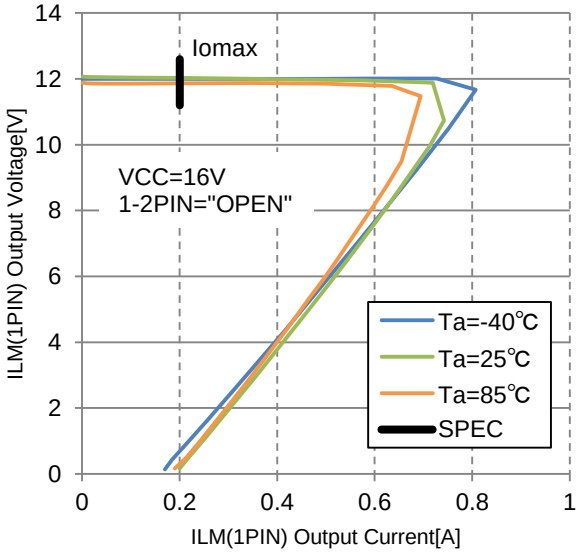


Fig23. [ILM(12V)] Vo vs. Io@VCC=16V

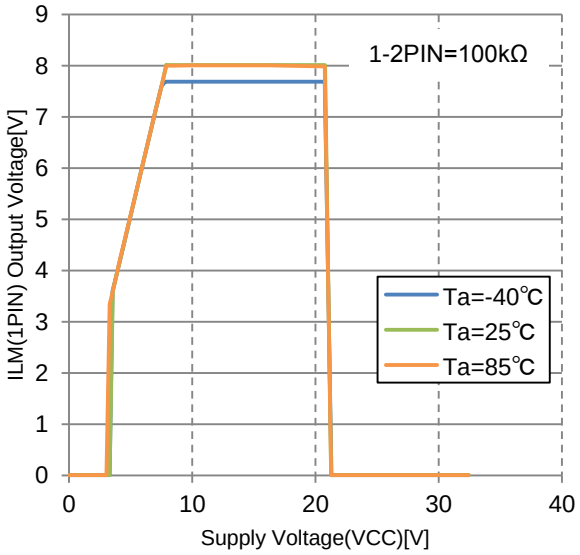


Fig24. [ILM(8V)] Vo vs. Input Voltage

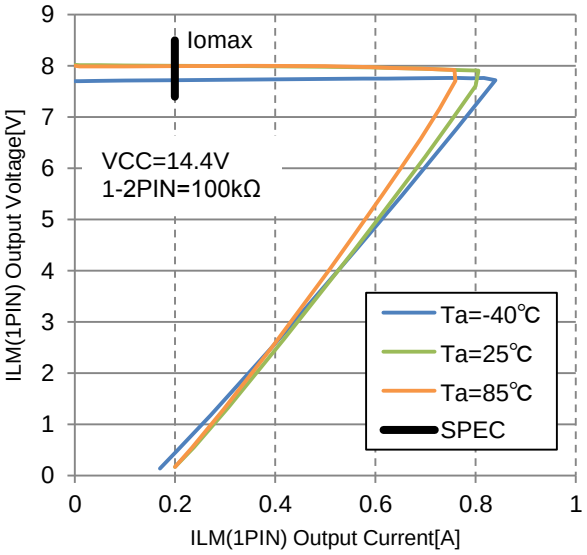


Fig25. [ILM(8V)] Vo vs. Io@VCC=14.4V

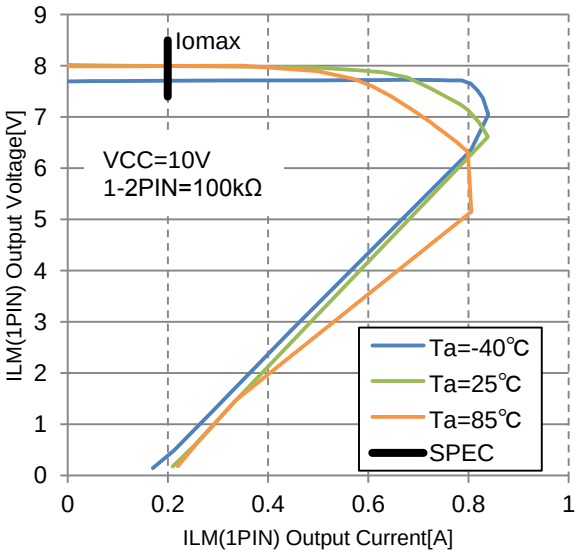


Fig26. [ILM(8V)] Vo vs. Io@VCC=10V

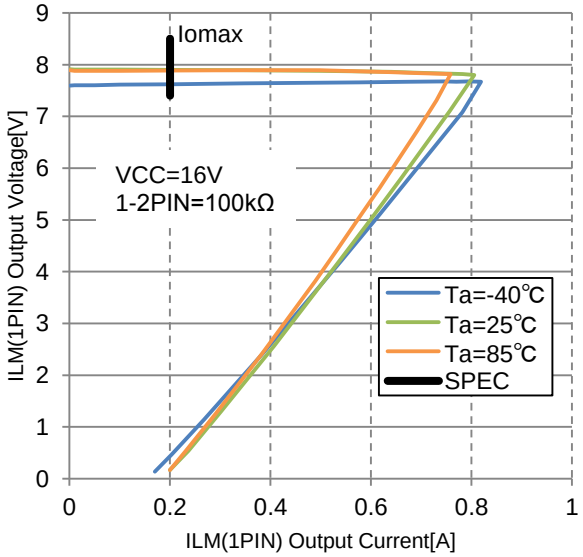


Fig27. [ILM(8V)] Vo vs. Io@VCC=16V

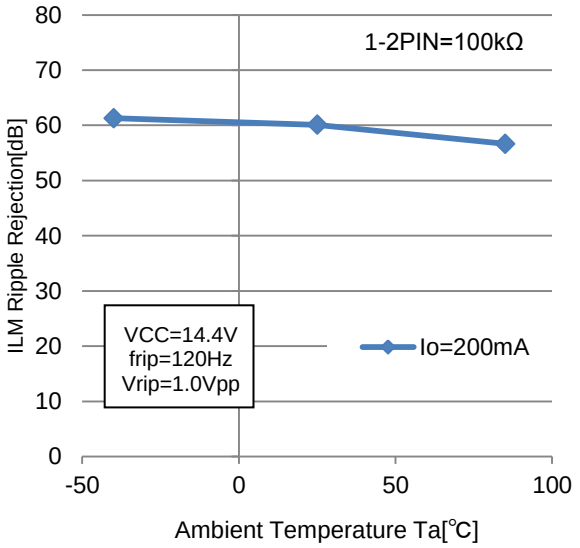


Fig28. [ILM(8V)] Ripple Rejection vs. Ta

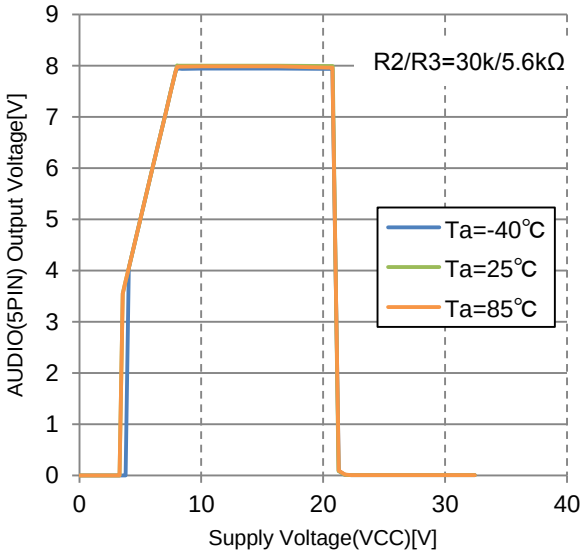


Fig29. [AUDIO(8V)] Vo vs. Input Voltage

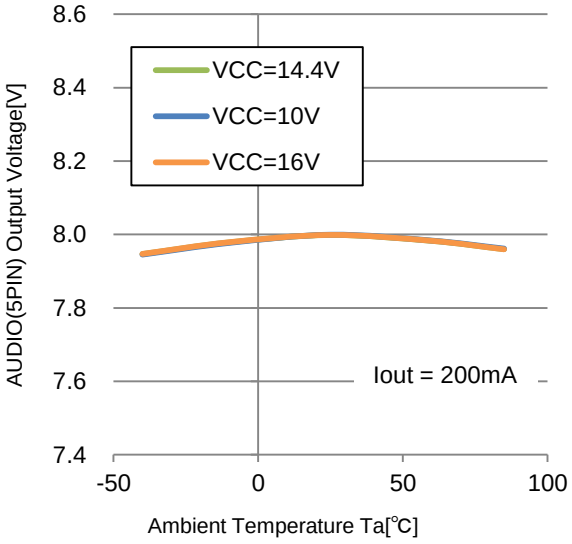


Fig30. [AUDIO(8V)] Vo vs. Ta

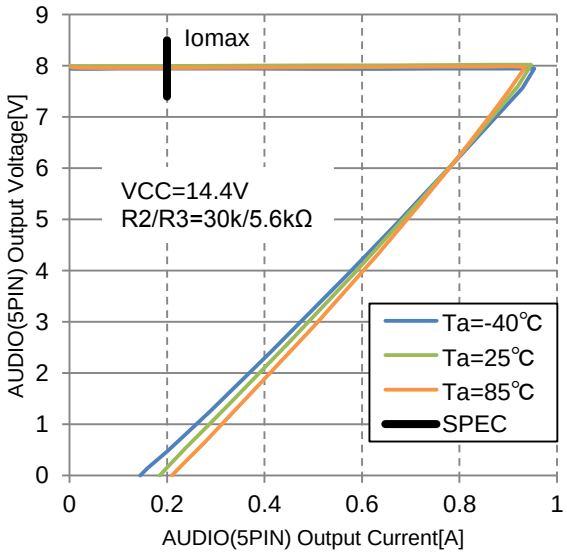


Fig31. [AUDIO(8V)] Vo vs. Io@VCC=14.4V

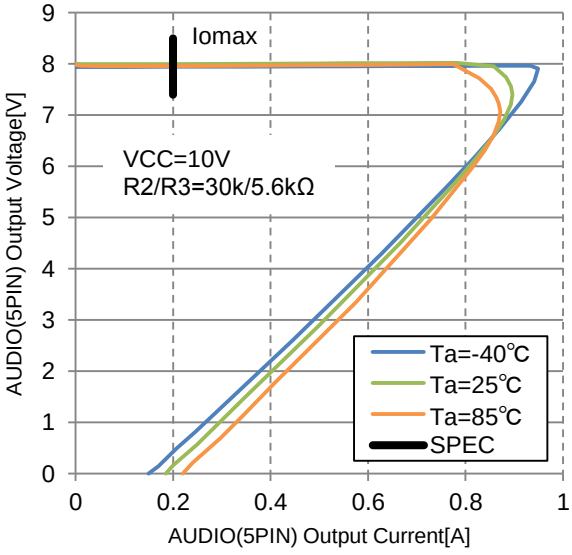


Fig32. [AUDIO(8V)] Vo vs. Io@VCC=10V

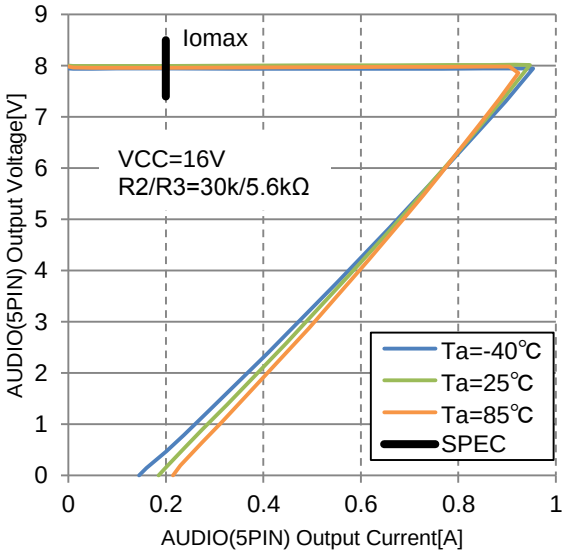


Fig33. [AUDIO(8V)] Vo vs. Io@VCC=16V

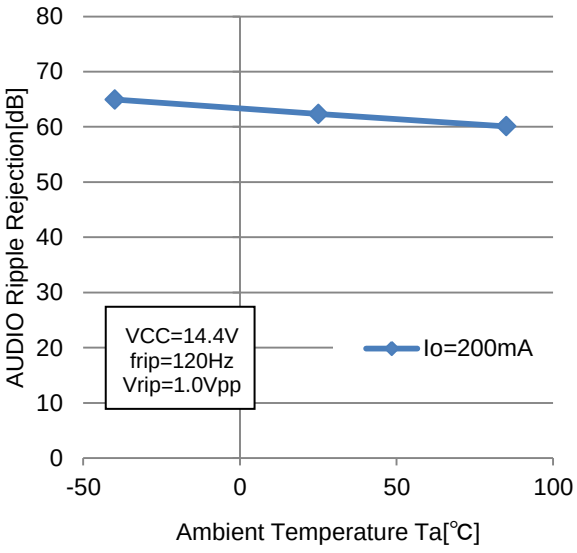


Fig34. [AUDIO(8V)] Ripple Rejection vs. Ta

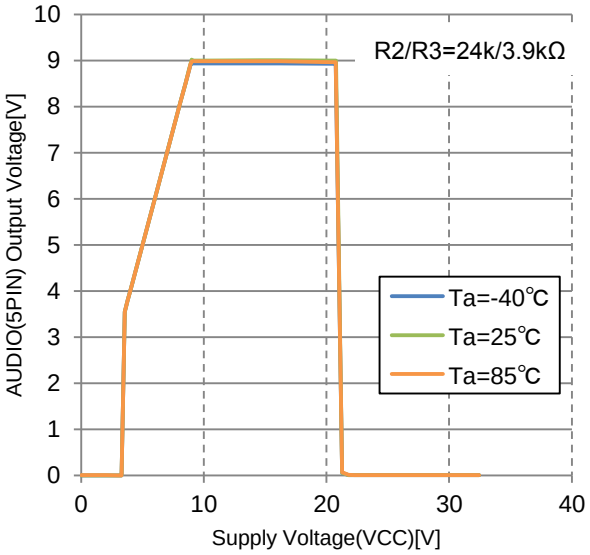


Fig35. [AUDIO(9V)] Vo vs. Input Voltage

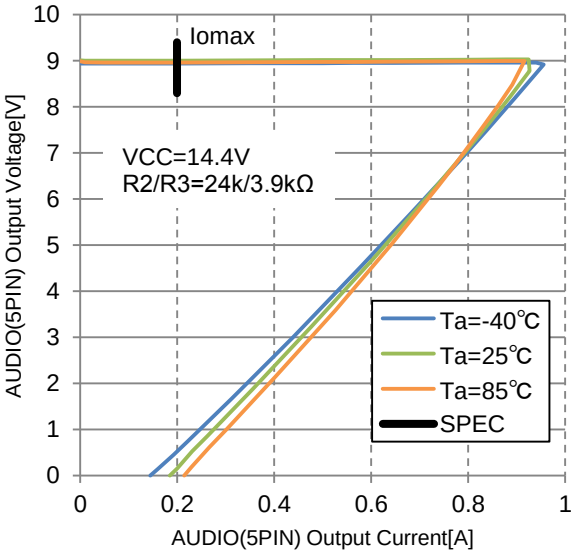


Fig36. [AUDIO(9V)] Vo vs. Io@VCC=14.4V

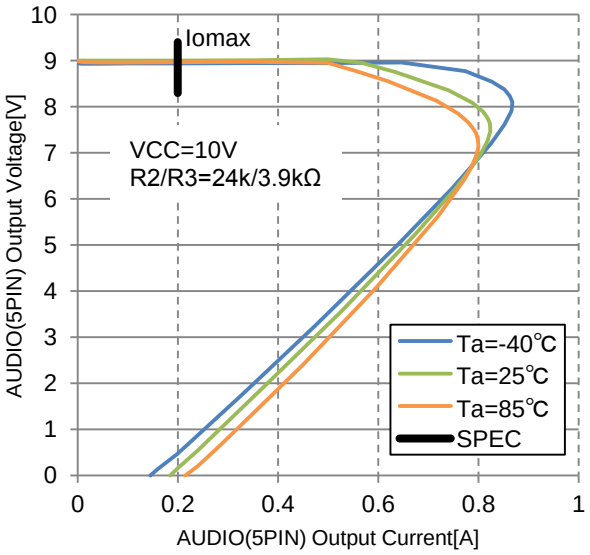


Fig37. [AUDIO(9V)] Vo vs. Io@VCC=10V

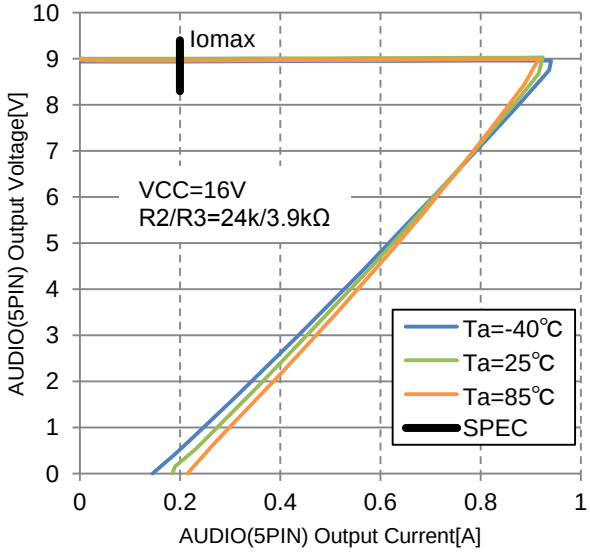


Fig38. [AUDIO(9V)] Vo vs. Io@VCC=16V

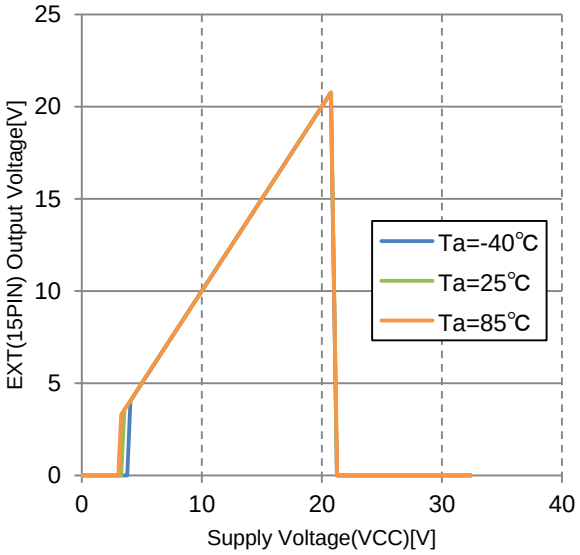


Fig39. [EXT] Vo vs. Input Voltage

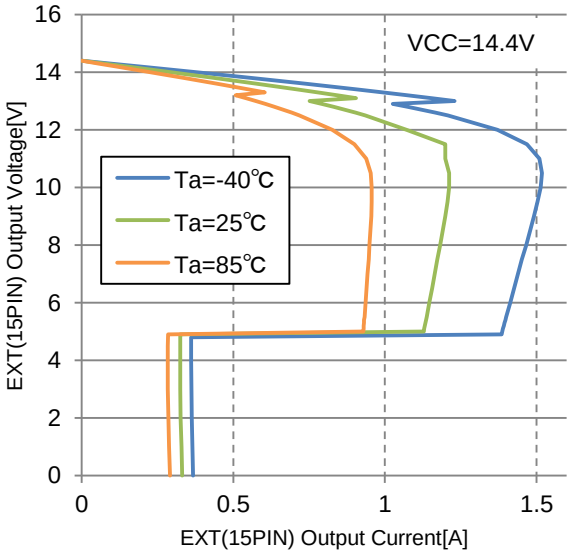


Fig40. [EXT] Vo vs. Io@VCC=14.4V

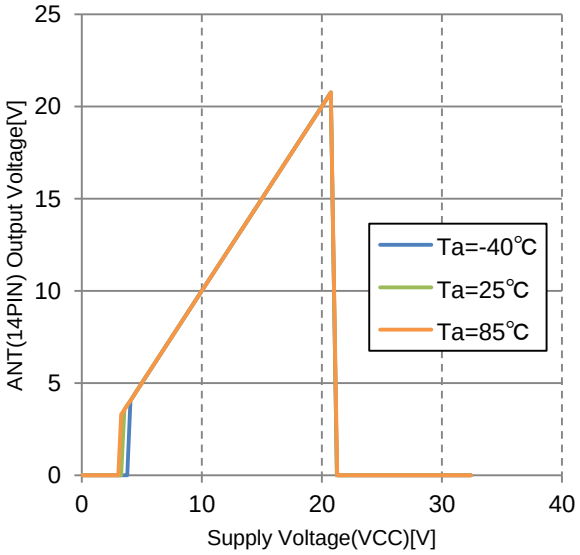


Fig41. [ANT] Vo vs. Input Voltage

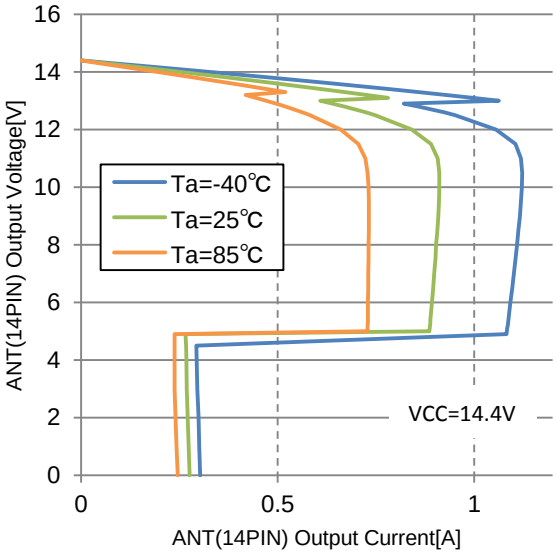


Fig42. [ANT] Vo vs. Io@VCC=14.4V

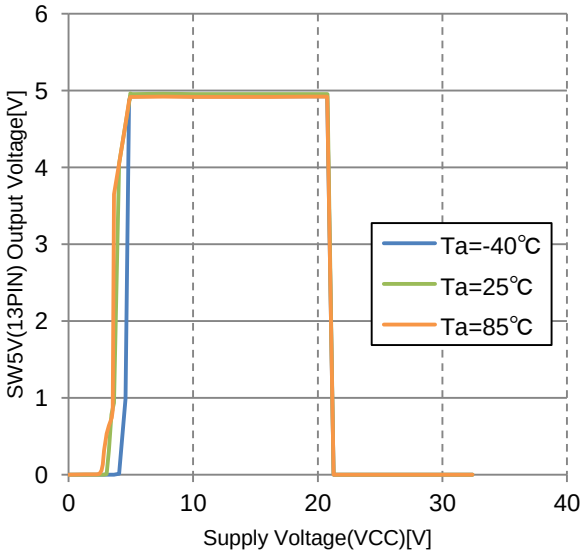


Fig43. [SW5V] Vo vs. Input Voltage

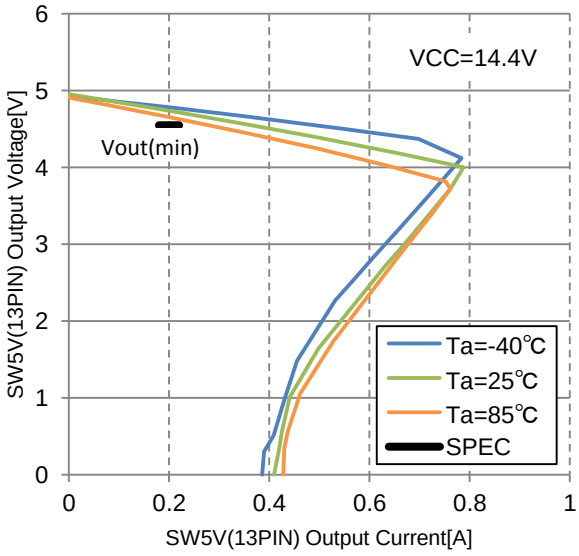


Fig44. [SW5V] Vo vs. Io@VCC=14.4V

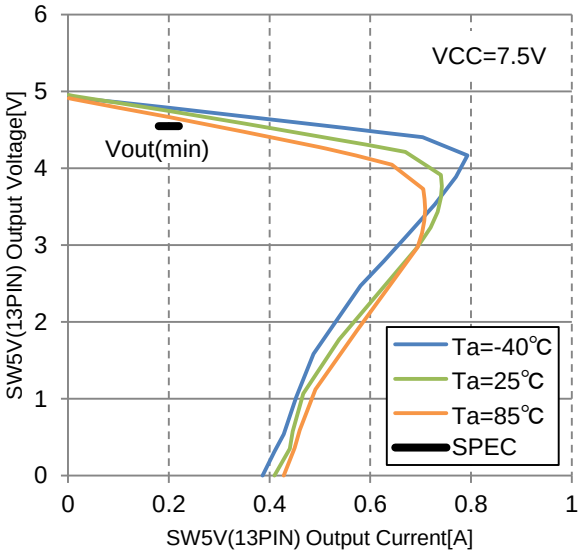


Fig45. [SW5V] Vo vs. Io@VCC=7.5V

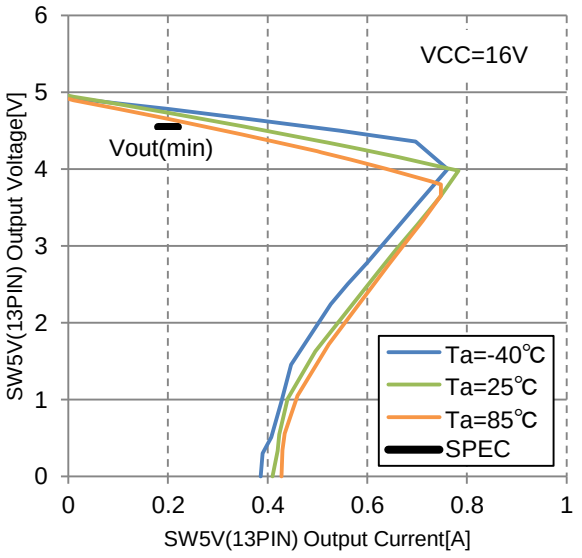


Fig46. [SW5V] Vo vs. Io@VCC=16V

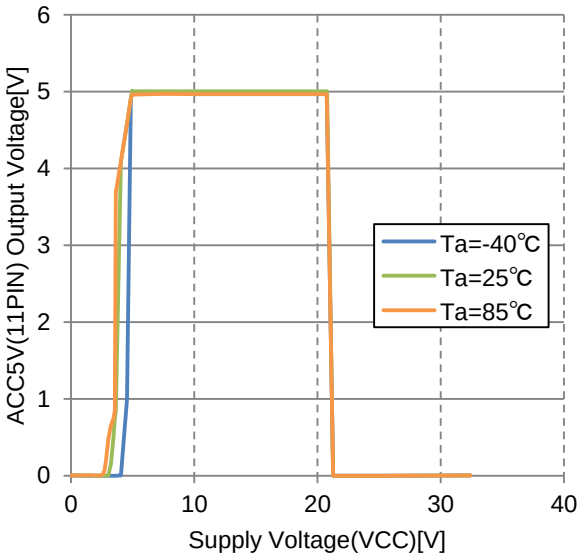


Fig47. [ACC5V] Vo vs. Input Voltage

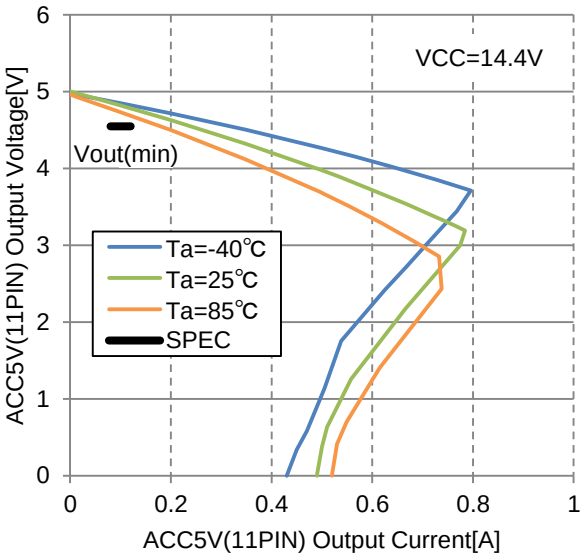


Fig48. [ACC5V] Vo vs. Io@VCC=14.4V

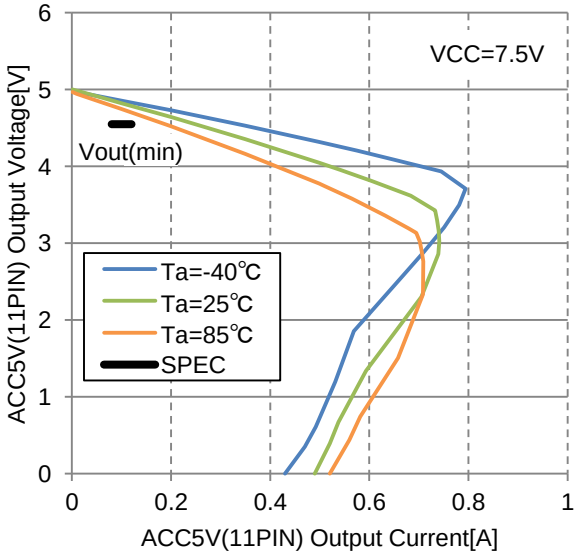


Fig49. [ACC5V] Vo vs. Io@VCC=7.5V

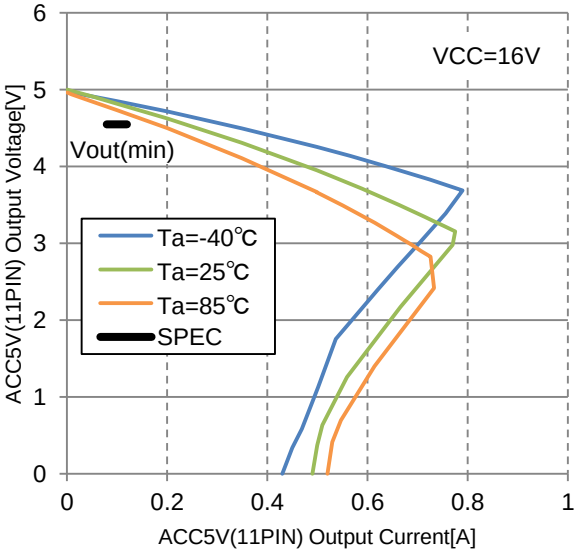
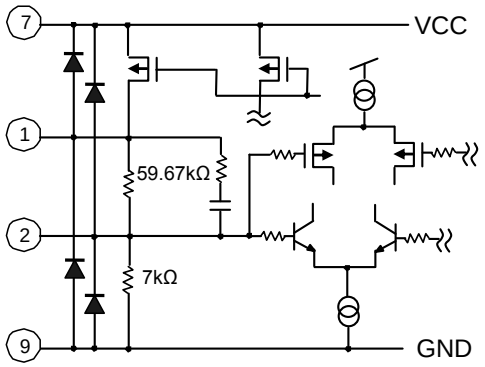
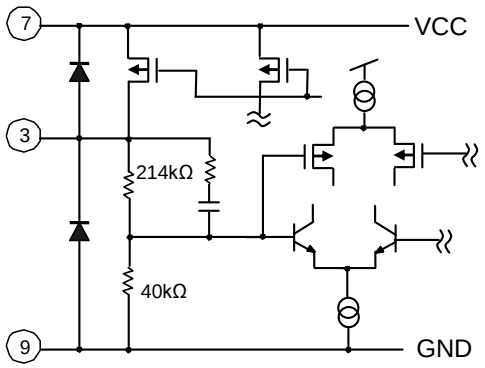
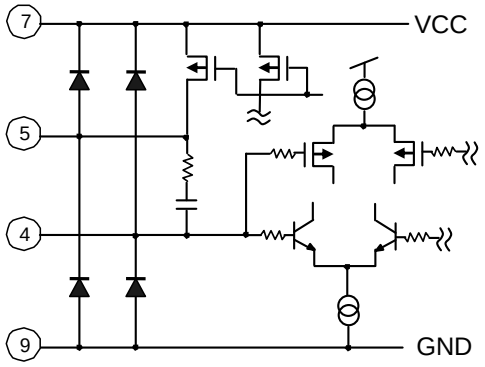
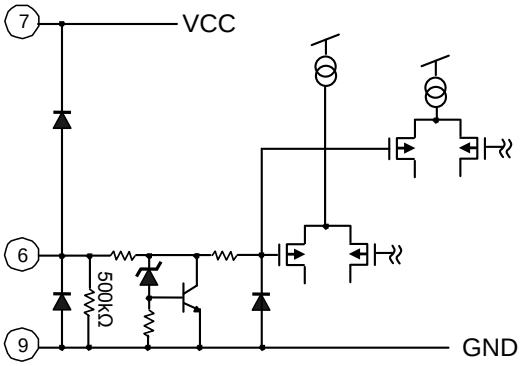
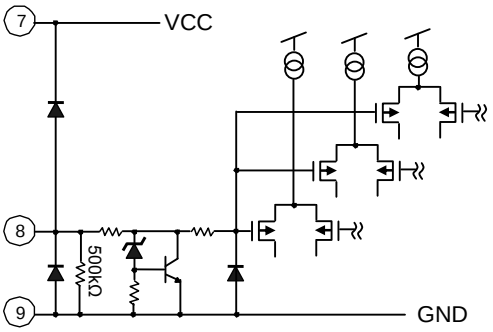
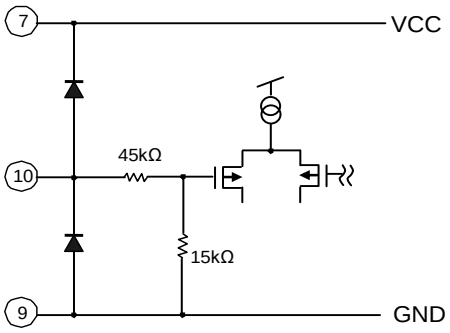
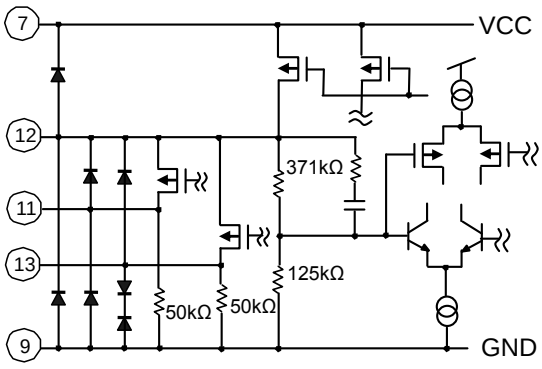
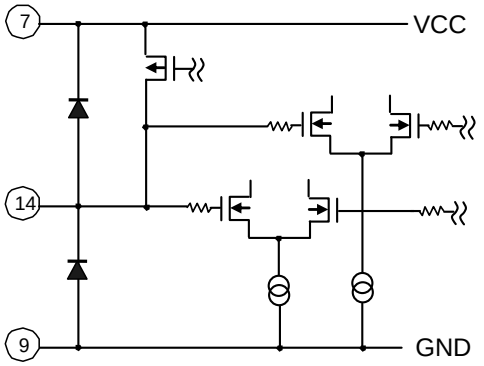
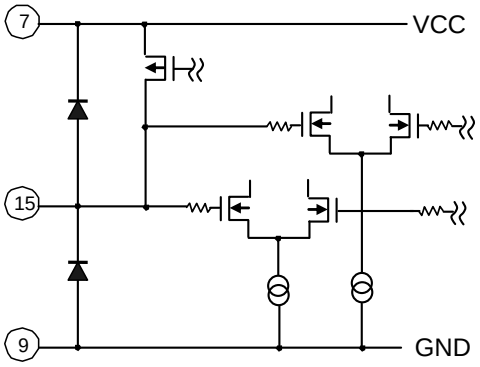


Fig50. [ACC5V] Vo vs. Io@VCC=16V

Terminal outline

Pin No.	Terminal	Function	Equivalent circuit
1	ILM	ILM OUT at CTRL1=M1,M2,H, OUT=ON 12.0V/300mA	
2	ILM_F	ILM Feed back	
3	CD	CD OUT at CTRL2=M,H, OUT=ON 8.0V/1.3A	
4	AUDIO_F	AUIDO Feed back	
5	AUDIO	AUDIO OUT at CTRL2=M,H, OUT=ON	
6	CTRL2	CTRL2(Input) 3 input values	

Pin No.	Terminal	Function	Equivalent circuit
7	VCC	Power	
8	CTRL1	CTRL1(Input) 4 input values	
9	GND	GND	
10	ACC	Accessory Voltage detector(input)	
11	ACC5V	Accessory OUT At ACC > 3V, OUT=ON	
12	VDD5V	VDD5V OUT 5.0V/200mA	
13	SW5V	SW5V OUT at CTRL2=M,H, OUT=ON	
14	ANT	ANT OUT at CTRL1=H, OUT=ON VCC-0.5V/300mA	

Pin No.	Terminal	Function	Equivalent circuit
15	EXT	EXT OUT at CTRL1=M2,H, OUT=ON VCC-0.5V/350mA	

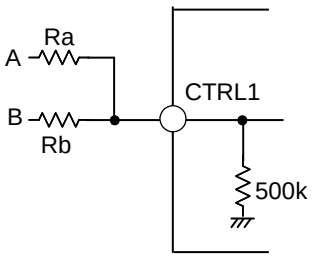


Fig51. CTRL1 Application Circuit

Input 3.3V：Ra=4.7kΩ,Rb=10kΩ

A	B	CTRL1
0V	0V	0V
0V	3.3V	1.05V
3.3V	0V	2.23V
3.3V	3.3V	3.20V

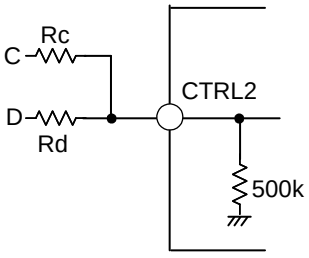


Fig52. CTRL2 Application Circuit

Input 3.3V：Rc=Rd=4.7kΩ

C	D	CTRL2
0V	0V	0V
0V	3.3V	1.61V
3.3V	0V	1.61V
3.3V	3.3V	3.29V

Board Layout

・Layer 1(Top)

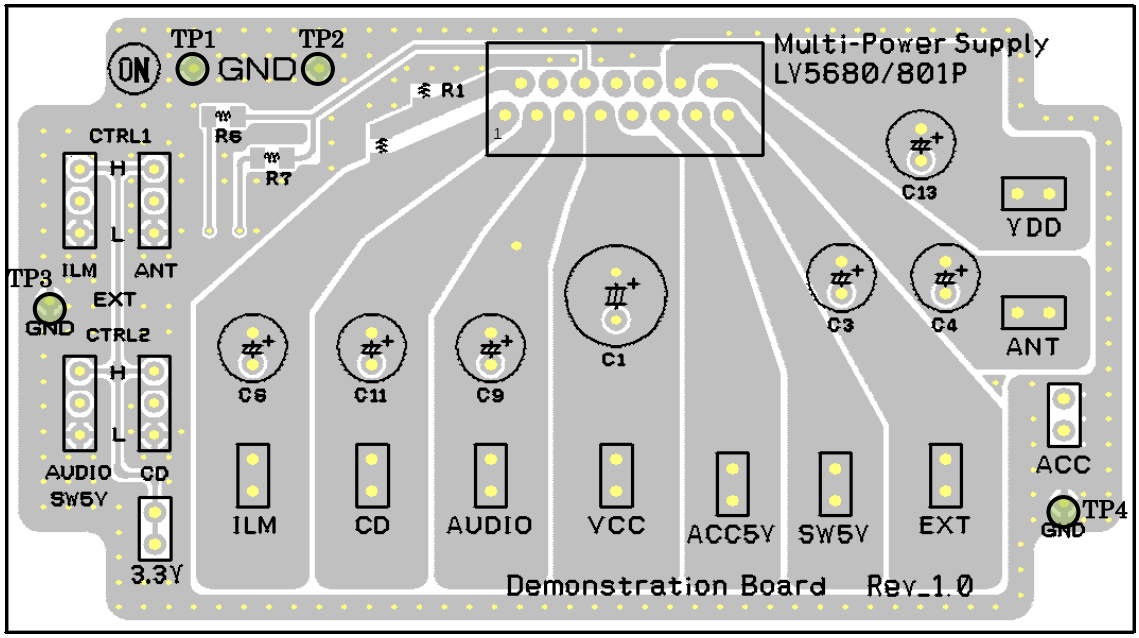


Fig53. Top Layer

・Layer 2(Bottom)

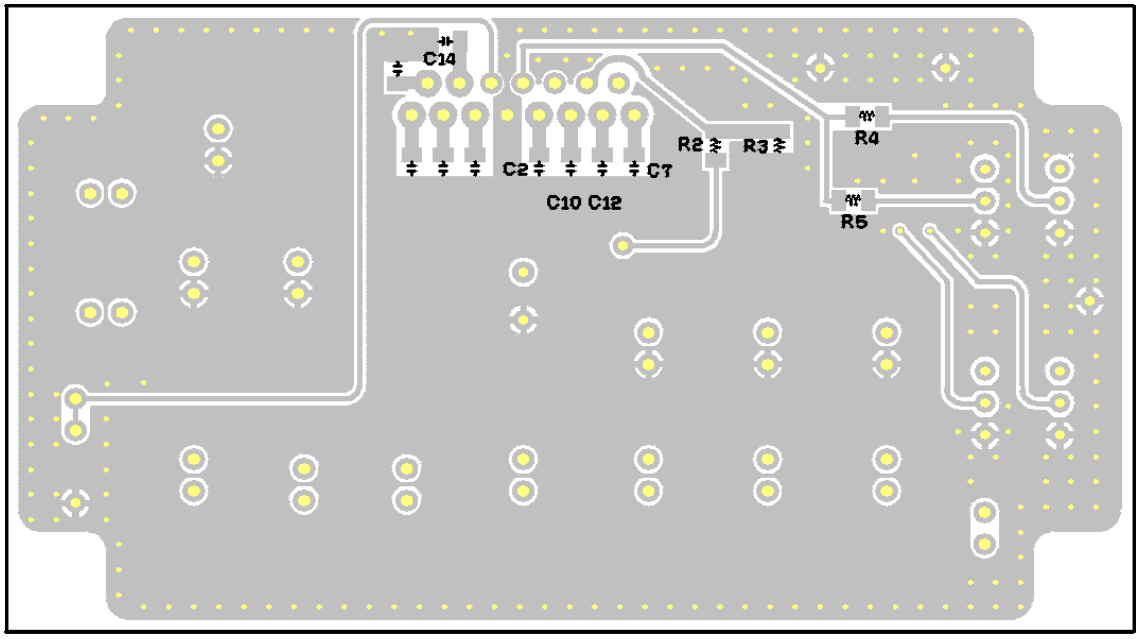


Fig54. Bottom Layer

Application Circuit Example

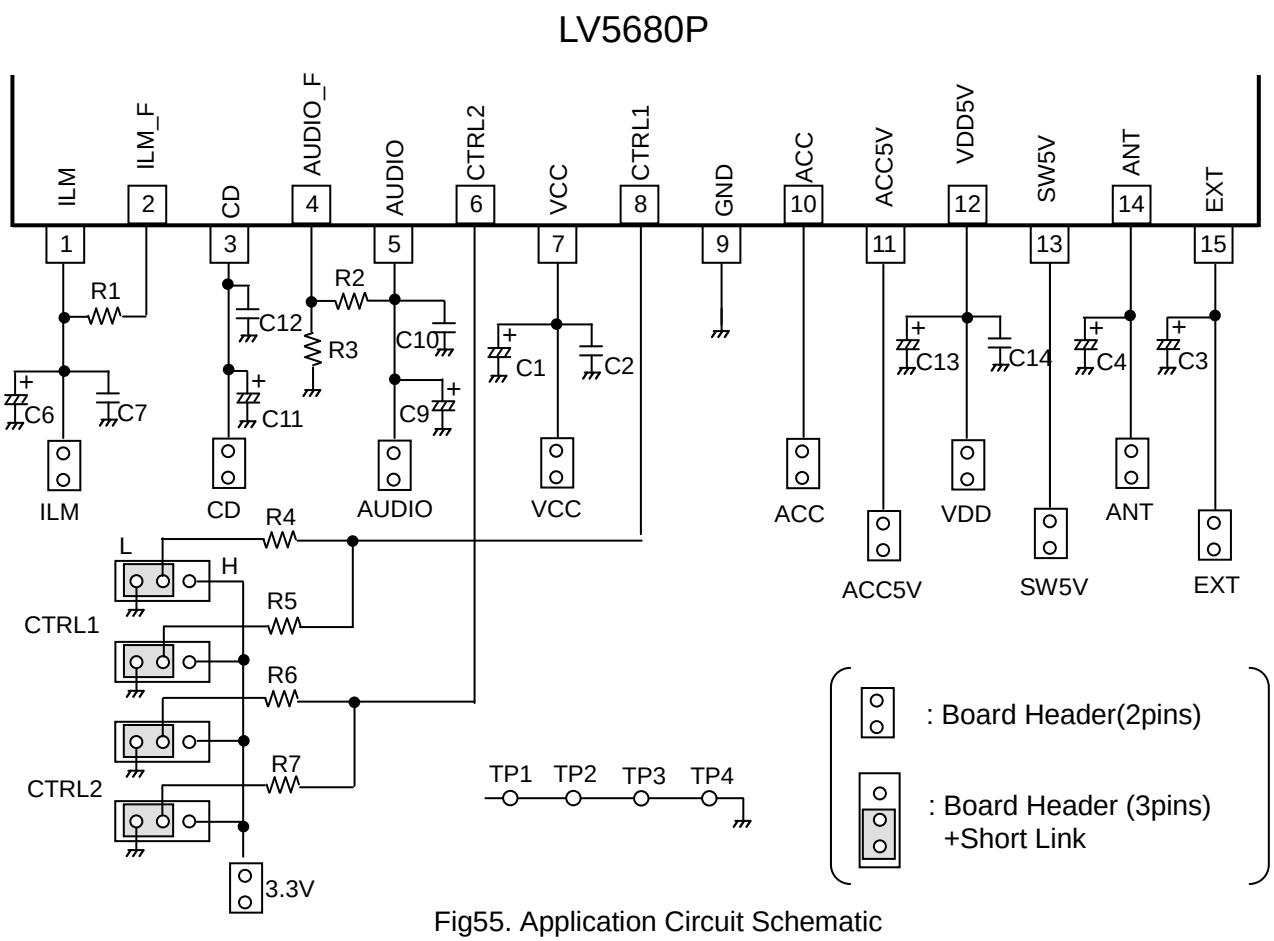
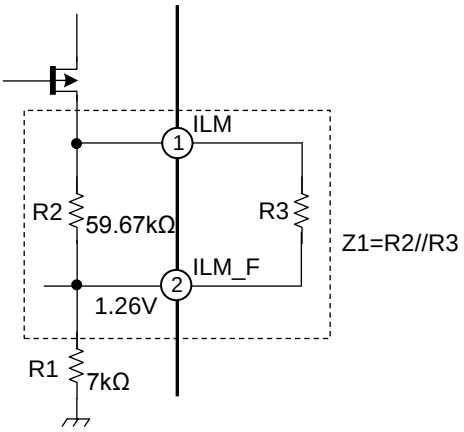


Fig55. Application Circuit Schematic

Bill of Materials

Reference	Value	Part	Vendor	Comments
C1	100μF/50V	UVR1H101MPD	nichicon	Capacitor, Aluminum Electrolytic
C2,C7,C10, C12,C14	0.22μF/50V	GRM21BR71H224KA01L	Murata	Capacitor, Ceramic
C3,C4	2.2μF/50V	UVK1H2R2MDD	nichicon	Capacitor, Aluminum Electrolytic
C6,C9, C11,C13	10μF/25V	UMA1E100MDD/ ECEA1FKS100	nichicon/ Panasonic	Capacitor, Aluminum Electrolytic
R1	270kΩ/0.125W	CRG0805F270K	Tyco Electronics	Resistor, Thick Film
R2	27kΩ/0.125W	CRG0805F27K	Tyco Electronics	Resistor, Thick Film
R3,R5, R6,R7	4.7kΩ/0.125W	CRG0805F4K7	Tyco Electronics	Resistor, Thick Film
R4	10kΩ/0.125W	CRG0805F10K	Tyco Electronics	Resistor, Thick Film
BH(3pins)	3pins	W81136T3843RC	RS	Board Header
SL*		W8010T50RC	RS	Short Link
BH(2pins)	2pins	M20 9763646	RS	Board Header
TP1-TP4		ST-4-2	MAC8	Test Point

• Setting method of ILM Output Voltage



ILM_F is equal to bandqap reference voltage. (typ=1.26V)

Fig56. ILM feed-back network

ILM calculating formula

$$Z_1 = R_2 // R_3 = \frac{R_2 \cdot R_3}{R_2 + R_3}$$

$$ILM = \frac{1.26[V]}{R_1} \times Z_1 + 1.26[V]$$

$$Z_1 = \frac{(ILM - 1.26) \cdot R_1}{1.26} \qquad R_3 = \frac{R_2 \cdot Z_1}{R_2 - Z_1}$$

(Ex.)Setup to ILM=9V

$$Z_1 = \frac{(9V - 1.26V) \cdot 7k\Omega}{1.26V} \cong 43k\Omega$$

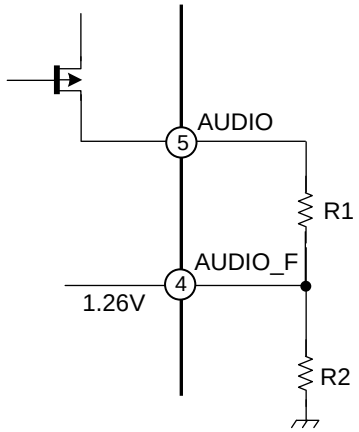
$$R_3 = \frac{59.67k\Omega \cdot 43k\Omega}{59.67k\Omega - 43k\Omega} \cong 153.9k\Omega \rightarrow \boxed{150k\Omega}$$

When R3=150kΩ, ILM output voltage is

$$Z_1' = \frac{59.67k\Omega \cdot 150k\Omega}{59.67k\Omega + 150k\Omega} \cong 42.69k\Omega$$

$$ILM = \frac{1.26V}{7k\Omega} \times 42.69k\Omega + 1.26V \cong \boxed{8.94V}$$

• Setting method of AUDIO Output Voltage



AUDIO_F is equal to bandqap reference voltage. (typ=1.26V)

Fig57. AUDIO feed-back network

AUDIO calculating formula

$$AUDIO = \frac{1.26[V]}{R_2} \times R_1 + 1.26[V]$$

$$\frac{R_1}{R_2} = \frac{(AUDIO - 1.26)}{1.26}$$

Please design so that the ratio of R1 and R2 may fill the above-mentioned expression for the set AUDIO voltage.

(Ex.) Setup to AUDIO=8.5V

$$\frac{R_1}{R_2} = \frac{(8.5 - 1.26)}{1.26} \cong 5.75$$

$$\frac{R_1}{R_2} = \frac{27k\Omega}{4.7k\Omega} \cong 5.74$$

$$AUDIO = 1.26V \times 5.74 + 1.26V \cong \boxed{8.49V}$$

*The above-mentioned are all the values at the typical. The error margin of output voltage is caused by the influence of the manufacturing variations of IC and external resistance.

Reference data for selecting output capacitor

VDD5V & ILM STABLE REGION

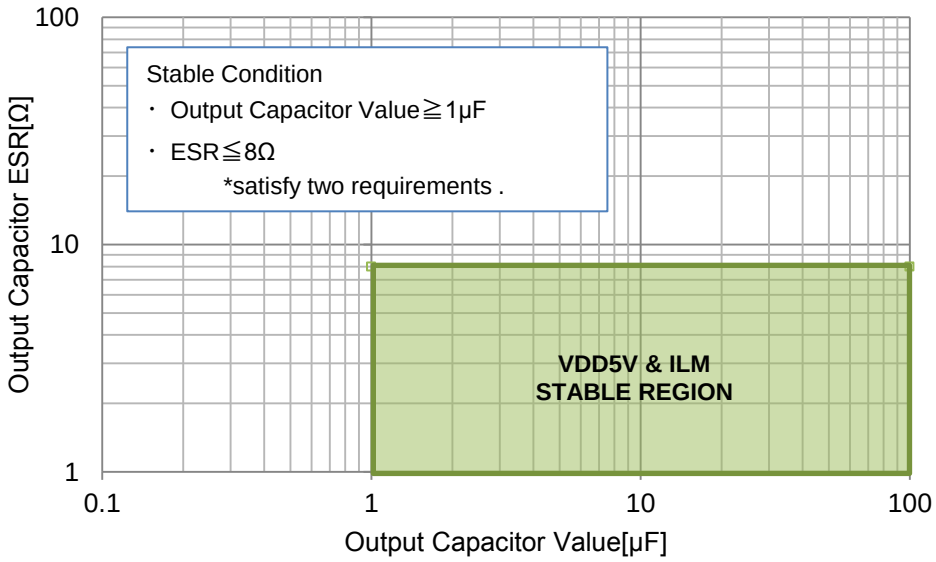


Fig58. VDD5V & ILM STABLE REGION

CD & AUDIO STABLE REGION

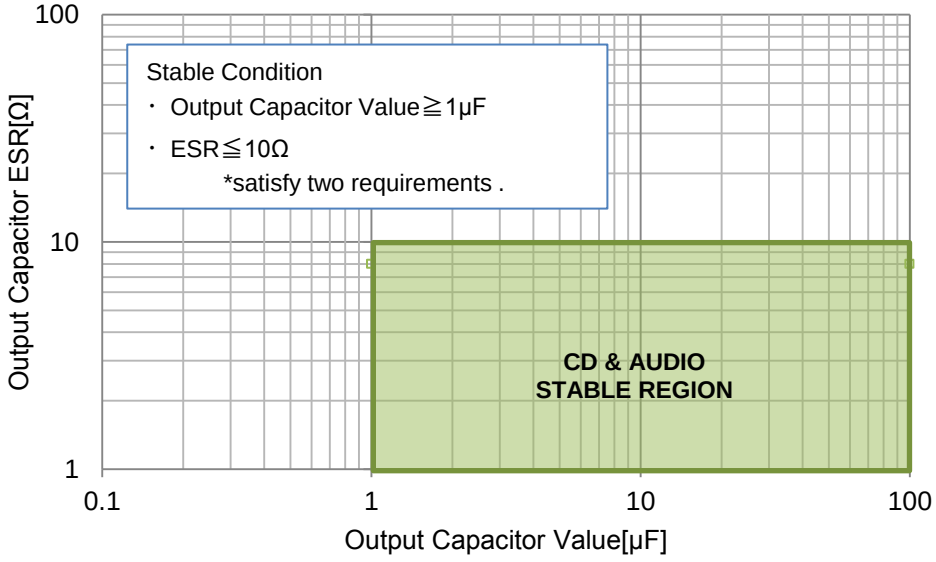


Fig59. CD & AUDIO STABLE REGION

Make sure that output capacitors is higher than 1uF and meets the condition of ESR, in which voltage/ temperature fluctuation and unit differences are taken into consideration. Moreover, RF characteristics of electrolytic capacitor should be sufficient.

*The above data is based on the result of the evaluation using our evaluation board under the specified conditions.

*Oscillation tolerance is influenced by PCB layout, connection, parasitic capacitance and inductance. Therefore, make sure to use the system that will actually be offered to the market and define a constant after a sufficient evaluation.

Functional Description

The LV5680P is a multiple output voltage regulator with two power switches, suitable for use in car audio system.

VCC

This IC has the tolerance value of 50V against VCC peak surge voltage, but for more safety set design, adding power clamp, such as power zenner diode, on battery connected line is recommended in order to absorb applied surge.

This IC has no protection against battery reverse connection, so adding Schottky diode is recommended to prevent a negative voltage.

Linear Regulators

All regulators in LV5680P are low dropout outputs, because the output stage of all regulators is PLDMOS.

When you select output capacitors for linear regulators, you should consider three main characteristics: startup delay, transient response and loop stability. The capacitor values and type should be based on cost, availability, size and temperature constraints. Tantalum, Aluminum electrolytic, Film, or Ceramic capacitors are all acceptable solutions. However, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but if the circuit operates at low temperatures(-25 to -40℃), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's datasheet usually provides this information.

VDD5V regulator (5.0V, 0.2A)

When VCC is applied, VDD5V output is active regardless of CTRL states.

VDD5V output supplies the current to SW5V and ACC5V output. Therefore, the current supply capability of VDD5V output and its other electrical characteristics are affected by the condition of SW5V and ACC5V output.

The over-current limiting circuit of VDD5V, SW5V, and ACC5V is common. So when the total output current value of three terminals reaches the limit value, the over-current limiting circuit operates.

CD regulator (8.0V, 1.3A)

When CTRL2 is “H”, CD output is active. CD output has the highest current capability of four regulators in LV5680P.

AUDIO regulator (8-9V, 0.3A)

When CTRL2 is “M” & “H”, AUDIO output is active. AUDIO output should set the output voltage by external resistance. For the setting method of the voltage, please refer to the explanation of this application note p.22.

ILM regulator (8-12V, 0.3A)

When CTRL1 is “M1”, “M2” & “H”, ILM output is active. ILM output voltage can be adjusted by external resistance between ILM and ILM_F. If there is no external resistance, ILM output voltage is 12V by built-in resistance. For the setting method of the voltage, please refer to the explanation of this application note p.22.

EXT & ANT high-side switches

The two high-side power switches connected to VCC are a 350mA output (EXT) and a 300mA output (ANT).

If these outputs are connected to inductive load or loads which have different ground potential, diodes (D2 and D4 in Fig.4) are necessary to protect the device from negative voltage.

SW5V switch

This high-side switch connected to VDD5V is a 200mA output. When CTRL2 is “M” & “H”, SW5V output is active. A pull-down resistance (50kΩ) is connected between SW5V and GND.

ACC detector circuit

When ACC input voltage is over 3V (typ), ACC5V output is active. ACC5V output is a high-side switch connected to VDD5V. A pull-down resistance (50kΩ) is connected between ACC5V and GND.

The ACC detection voltage has hysteresis characteristics, and the hysteresis value is

0.3V (typ). The ACC input has a pull-down resistance, and this resistance value is 60kΩ.
ACC terminal is high-voltage input as well as VCC terminal.

CTRL1, 2 input

CTRL1 accepts four input values (L/M1/M2/H), and CTRL2 accepts three input values (L/M/H).
CTRL1 & CTRL2 have a pull-down resistance, and this resistance value is 500kΩ.
Logic table is shown at p.19.

Protection

Thermal Shutdown

To protect the device from overheating a thermal shutdown circuit is included. If the junction temperature reaches approximately 175 ℃ (typ), all outputs are turned off regardless of CTRL state. Outputs remain disabled until the junction temperature drops below 145℃(typ)(automatic restoration).

The thermal shutdown circuit does not guarantee the protection of the final product because it operates out of maximum rating (exceeding Tjmax=150℃).

Current Limiting

When the each output becomes in over load condition, the device limits the output current. All outputs are also protected against short circuit by fold back current limiter.

Overvoltage

The device is protected against load dump.

When VCC voltage exceeds 21V, the device detects over voltage condition and turns all the outputs off except VDD to protect the device. If VCC voltage gets below 21V, outputs are automatically restored.

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TEST Procedure

Line regulation

Line regulation is defined as the maximum change in output voltage as the input voltage is varied through the specified range. It is measured by changing the input voltage and measuring the minimum/maximum voltage of the output. Line regulation is defined as the difference between maximum and minimum voltage.

Load regulation

Load regulation is defined as the maximum change in output voltage as the load current is varied through the specified range. It is measured by changing the load current and measuring the minimum/maximum voltage of the output. Load regulation is defined as the difference between maximum and minimum voltage.

Dropout voltage

Dropout voltage is defined as the minimum input-to-output differential voltage at the specified load current required by the regulator to keep the output voltage in regulation. It is measured by reducing input voltage until the output voltage drops below the nominal value.

Ripple rejection

Ripple rejection is defined as the ratio of input ripple amplitude versus that of output.

LV5680P Application Note

LV5680P is used, before the set design, must check the following

1. Absolute Maximum Rating (*Common notes to general semiconductor device)*

Stresses exceeding Maximum Ratings may damage the device. If a IC is applied stresses exceeding Maximum Ratings, a IC might smoke or fire by the breakdown and the overheating.

We recommend to derating design for reducing failure rate of device. A guide of general derating design is described below.

(1)Stress Voltage: 80% or less for Abs Max voltage.

(2)Maximum rating current: 80% or less for Abs Max Io.

(3)Temperature: 80% or less for Temperatures rating.

2. Recommended Operating Range

When LV5680P was used within Recommended Operating Range and Temperature Rating, unless otherwise specified, we do not guarantee the specified value in all temperature ranges. As long as the IC is at operation temperature range, IC's characteristic doesn't change suddenly. Operating conditions of the input voltage and the output current are limited by the chip maximum junction temperature (Tjmax). Please decide the value of the input voltage and the output current so as not to exceed Tjmax.

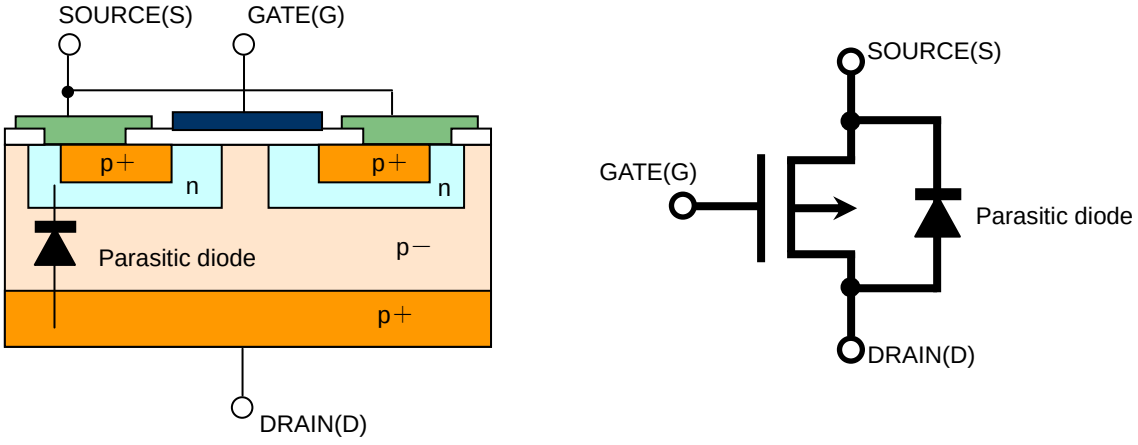
3. Output Capacitor

Between GND and each output, please be sure to put capacitor to prevent oscillation. Because abrupt changes of input voltage and output load interfere in the output voltage, make sure to use the system that will actually be offered to the market and define the output capacitor after a sufficient evaluation. When selecting the capacitor, to ensure the required minimum capacity over all operating conditions of the application, it is necessary to consider the influence of a temperature and a applied voltage on the capacity value.

Please design the PCB pattern that the output terminal and the capacitor are located as close as possible.

4. Parasitic Devices

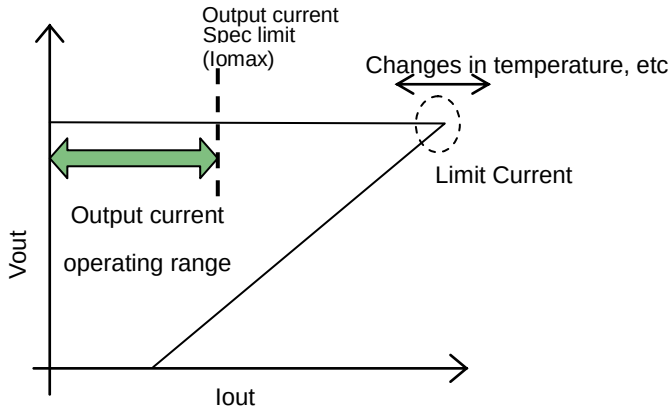
Output Power MOS-FET driver has, in device structure, parasitic diode like the figure below. Because in normal operating the input voltage is higher than the output voltage, the parasitic diode is reverse bias. If the output is higher than the input at abnormal operating, a current flows from the output to the input, because the parasitic diode is forward biased.

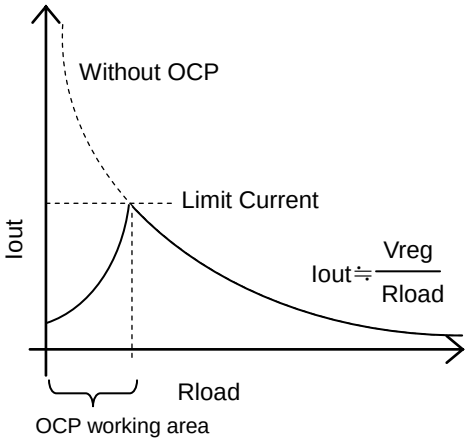


5. Over -Current Protection

Each channel has an Over-Current Protection (OCP) circuit which is the "Fold-Back" type, OCP circuit prevent IC's break down at an over current condition. This circuit is useful against sudden over current, but use of continuous operation is not allowed.

The limit value of output current is changed by ambient temperature and production tolerance. However, the limiting value doesn't fall below the output maximum current defined by the specification. When the output current uses it exceeding the maximum current, the OCP circuit might operate in some situations. Please design the equipment, to be sure than a specified value. Please design the output current to use without fail below a specified maximum value.





6. Over-Voltage Protection

When VCC voltage exceeds 21V, the device detects over voltage condition and shuts down all output but "VDD" to protect the device.

The peak voltage value (Vcc peak) changes depending on Surge-waveform condition. Adding power clamp, such as power zenner diode, on battery connected line is recommended in order to absorb applied surge.

7. Thermal shut-down

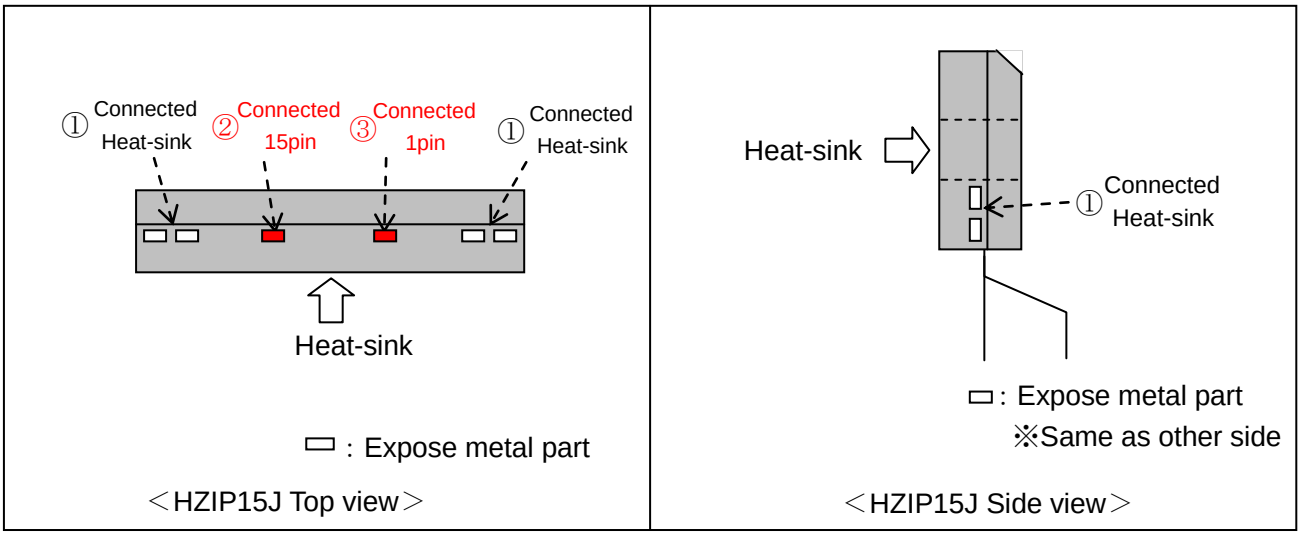
This IC built-in thermal shut-down circuit to prevent from thermal damage. If the state to exceed the Absolute Maximum Rating of the power dissipation continues, and the chip temperature (Junction temperature:Tj) reaches 175℃, the thermal shut-down circuit operates. When the thermal shut-down circuit operates, all outputs are turned off regardless of CTRL state. Outputs remain disabled until the junction temperature drops below 145℃(typ)(automatic restoration). If the operating condition is not changing, the output repeats on and off. The output seems to oscillate.

* The protector functions only improve the IC's tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under over-current protection range or thermal shutdown state may degrade the IC's reliability and eventually damage the IC.

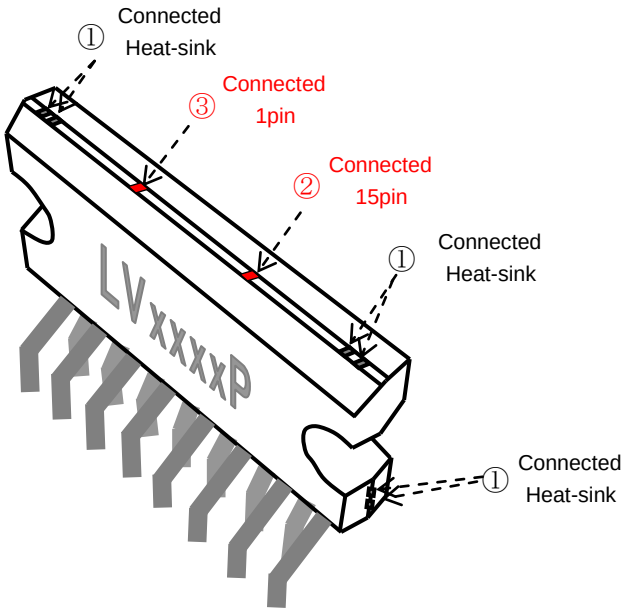
8. Notes on Installation

Package "HZIP15J", there are some places where metal is exposed except terminals and a heat sink. This includes the one connecting with the function pin. Especially, when the mounting hardware covers IC, do not bring "②" & "③" (in below figure) into contact with mounting hardware. The potential of point "①" as well as the heat sink is equal to GND.

・HZIP15J



*Caution :Do not bring “②” & ”③” into contact with mounting hardware.



9. Application Circuit Example

IC’s operating characteristics are influenced by PCB layout, connection, parasitic capacitance and inductance. Therefore, make sure to use the system that will actually be offered to the market and define a constant after a sufficient evaluation.

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