Ordering number : ENA2054A

LV5725JA

Bi-CMOS LSI

Step-down Switching Regulator

ON Semiconductor®

http://onsemi.com

Overview

The LV5725JA is a step-down voltage switching regulator.

Functions

- Wide input dynamic range: 4.5V to 50V.
- Current mode type.
- Built-in pulse-by-pulse OCP circuit: detection is on resistance of an external MOS.
- Over current protection: HICCUP mode.
- Thermal shutdown.
- Load-independent soft start circuit
- ON/OFF pin
- Synchronous operation by external signal.
- Power good pin
- External voltage is usable when output voltage is high.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter Sy		mbol	Conditions	Ratings	Unit
Supply voltage		V_{IN} max		55	V
Allowable pin voltage	V_{IN}, SW, OUT, PGOOD			55	V
	HDRV, CBOOT			61	V
	LDRV			6.0	V
	Between CBOOT to SW Between CBOOT to HDRV			6.0	V
	EN, ILIM			V_{IN}+0.3	V
	Between V_{IN} to ILIM			1.0	V
	V_{DD}			6.0	V
	SS, FB, COMP,RT, SYNC			V_{DD}+0.3	V
Allowable Power dissipation		Pd max	Mounted on a specified board. *	1.45	W
Operating temperature		Topr		-40 to +85	°C
Storage temperature		Tstg		-55 to +150	°C
Parameter		Symbol	Conditions	Ratings	Unit
Maximum junction temperature		Tj max		150	°C

* Specified board : 58.0mm × 78.0mm × 1.6mm, fiberglass epoxy printed board.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Semiconductor Components Industries, LLC, 2013

Recommended Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{IN}		4.5 to 50	V
Error amplifier input voltage	V_{FB}		0 to 1.6	V
Oscillatory frequency	F_{OSC}		50 to 500	kHz

Electrical Characteristics at Ta = 25°C, V_{IN} = 12V

Parameter Sy	mbol	Conditions	Ratings			Unit
			min ty	p	max	
Reference voltage block						
Internal reference voltage	Vref	Including offset of E/A 0.698		0.708	0.718	V
5V power supply	V_{DD}	I_{OUT} = 0 to 5mA	4.7	5.2	5.7	V
Triangular waveform oscillator block						
Oscillation frequency	F_{OSC} RT=	56kΩ 317		365	412	kHz
Frequency variation	F_{OSC} DV	V_{IN} = 4.5 to 50V		1		%
Fold back detection voltage	V_{OSC} FB	After power is supplied to SS, voltage is detected FB.		0.5		V
Fold back oscillation frequency	F_{OSC} FB RT=	56kΩ, V_{FB} = 0V	100	130	160	kHz
ON/OFF circuit block						
IC start-up voltage	V_{EN} on		-	2.5	3.0	V
Hysteresis of startup voltage	V_{EN} hys		0.3	0.6	-	V
Soft start circuit block						
Soft start source current	I_{SS} SC	EN > 3.0V	4	5	6	μA
Soft start sink current	I_{SS} SK	EN < 1V, V_{DD} = 5V		2		mA
Soft start end voltage	V_{SS} END		0.7	0.9	1.1	V
UVLO circuit block						
UVLO voltage	V_{UVLO}		3.7	4.0	4.3	V
Hysteresis of UVLO	V_{UVLO} H			0.3		V
Error amplifier						
Input bias current	I_{EA} IN				100	nA
Error amplifier gain	G_{EA}		1000	1400	1800	μA/V
Range of common-mode input voltage	V_{EA} R	V_{IN} = 4.5 to 50V	0		1.6	V
Output sink current	I_{EA} OSK	FB = 1.0V		-100		μA
Output source current	I_{EA} OSC	FB = 0V		100		μA
Current detection amplifier gain	GISNS			2.4		
Over current limiter circuit block						
Reference current	I_{LIM}		-10%	20	+10%	μA
Over current detection comparator offset voltage	V_{LIM_OFS}		-5		+5	mV
Range of over current detection comparator common mode input	V_{LIM_CM}		V_{IN}-0.45		V_{IN}	V
PWM comparator						
Input threshold voltage	Vt max	Duty cycle = D_{MAX}, SW = V_{IN} 1.15		1.25	1.35	V
	Vt0	Duty cycle = 0%, SW = V_{IN} 0.5		0.6	0.7	V
Maximum ON duty	D_{MAX}		92			%

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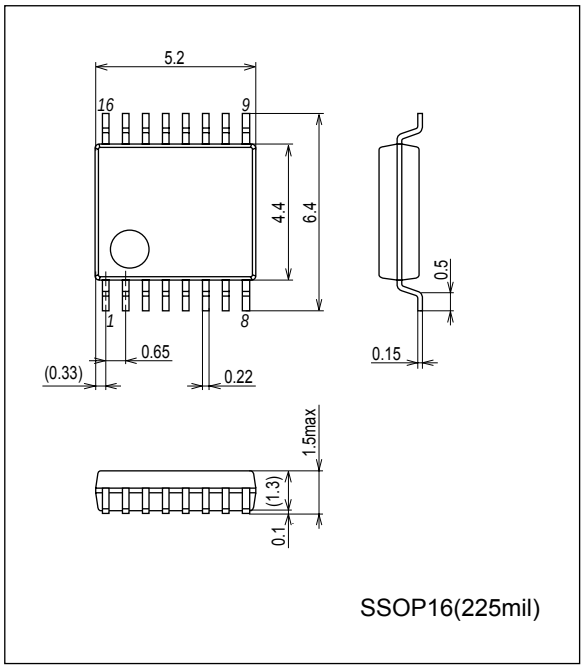
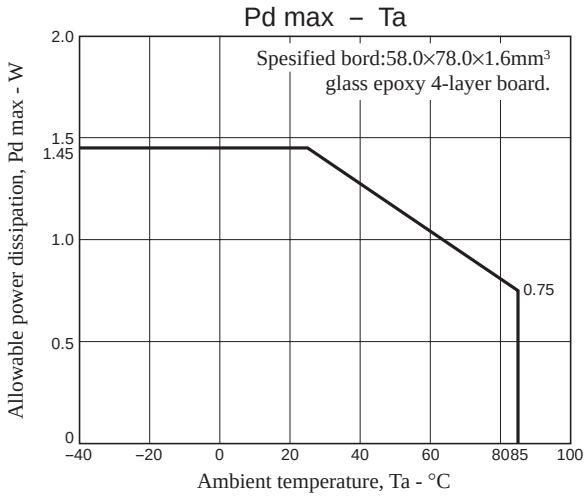
Parameter Sy	mbol	Conditions	Ratings			Unit
			min ty	p	max	
Power good						
Power good “L” sink current	$I_{PG}L$	PGOOD = 5V		5		mA
Power good “H” sink current	$I_{PG}H$	PGOOD = 5V			1	μA
Power good voltage	PG_{thresh}	When FB voltage rises		0.612		V
Hysteresis of power good	PG_{hys}			12		mV
Output block						
High side output ON resistance (upper)	R_{ONH}_HIGH	CBOOT – HDRV = -0.1V		12		Ω
High side output ON resistance (lower)	R_{ONL}_HIGH	HDRV – SW = +0.1V		3.3		Ω
Low side output ON resistance (upper)	R_{ONH}_LOW	V_{DD} – LDRV = -0.1V		7.9		Ω
Low side output ON resistance (lower)	R_{ONL}_LOW	LDRV – GND = +0.1V		3.8		Ω
High side output ON current (upper)	I_{ONH}_HIGH	CBOOT – HDRV = -4.5V	160			mA
High side output ON current (lower)	I_{ONL}_HIGH	HDRV – SW = +4.5V	330			mA
Low side output ON current (upper)	I_{ONH}_LOW	V_{DD} – LDRV = -5.2V	190			mA
Low side output ON current (lower)	I_{ONL}_LOW	LDRV – GND = +5.2V	250			mA
Entire device						
Standby current	I_{CCS} EN	< 1V			1	μA
Average current consumption	I_{CCA}	EN > 3.0V		2.5		mA

Package Dimensions

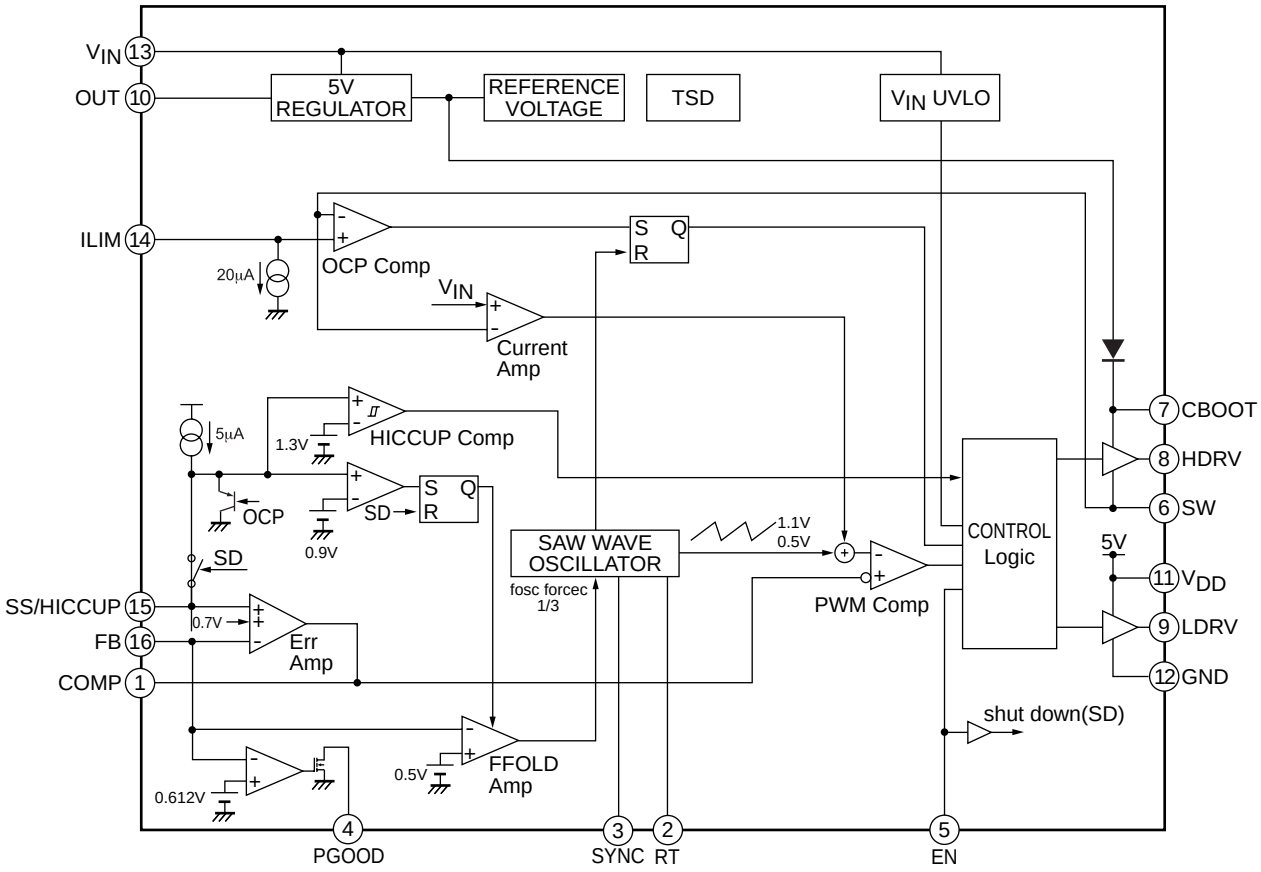
unit : mm (typ)

3178B

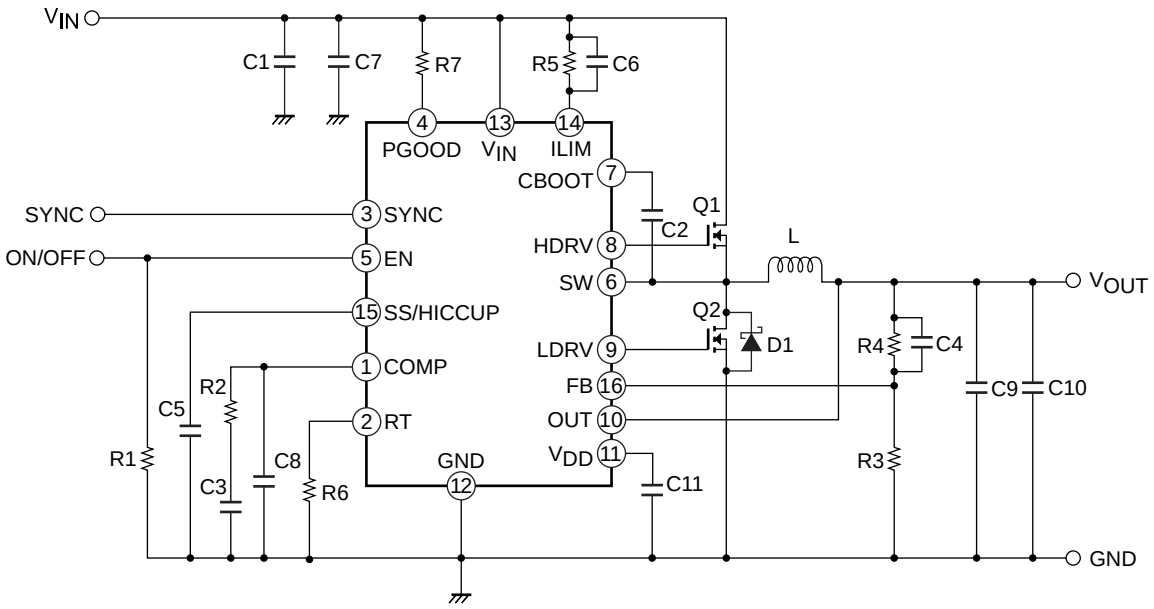




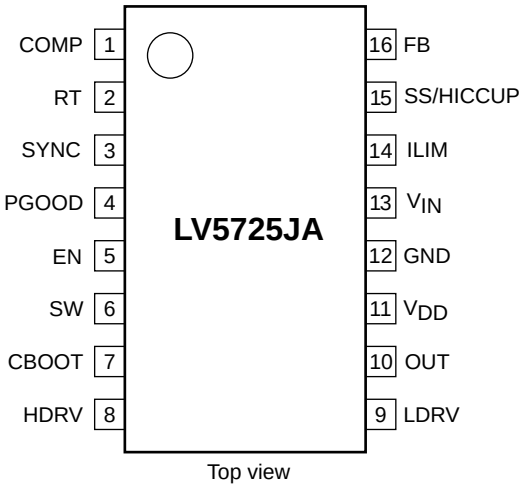
Block Diagram



Sample application circuit



Pin Assignment

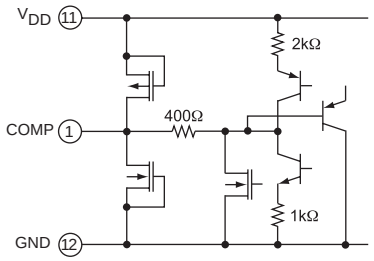
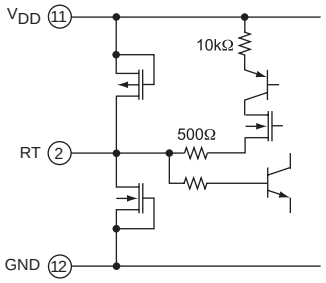
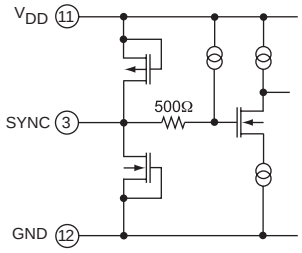
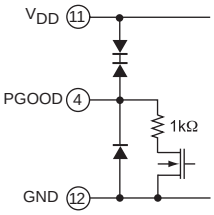
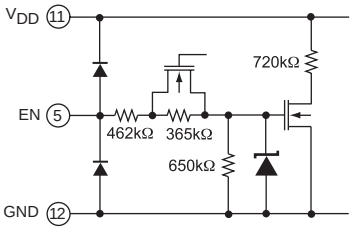
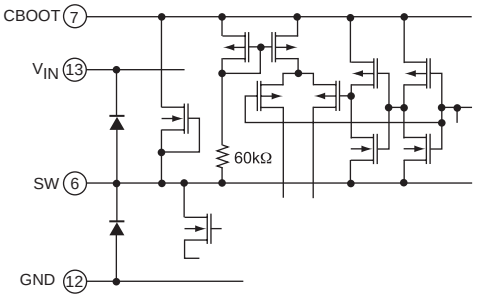


Top view

Pin Function

Pin No.	Pin name	Description
1	COMP	Error amplifier output pin. Make sure to connect a phase compensation network between COMP and GND.
2	RT	Oscillating frequency setting pin. Make sure to connect a resistor between this pin and GND.
3	SYNC	External synchronous signal input pin.
4	PGOOD	Power good pin.
5	EN	ON/OFF pin.
6	SW	This pin is connected to switching node. Connect the source of Nch MOSFET to this pin.
7	CBOOT	Bootstrap capacitor connected pin. This pin is used as gate driving power supply for external Nch MOSFET. Make sure to connect a capacitor between CBOOT and SW.
8	HDRV	External upper MOSFET gate driving pin.
9	LDRV	External lower MOSFET gate driving pin.
10	OUT	Internal regulator power supply pin. This pin is connected to V_{OUT}.
11	V_{DD}	Power supply pin for gate drive of the external lower MOS-FET.
12	GND	Ground pin. GND pin voltage is the reference for each reference voltage.
13 V	IN	Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes higher than 4.3V by UVLO function, the IC starts up and mode shifts to soft start operation.
14	ILIM	Reference current pin for current detection. The inlet current of approx. 20μA flows into this pin. Connect a resistor externally between this pin and VIN and when the voltage supplied to SW pin is lower than the pin voltage of this resistor, the upper Nch MOSFET is turned off by current limiter comparator. This operation is reset at every PWM pulse.
15	SS/HICCUP	Capacitor connection pin for soft start. This pin enables to charge the soft start capacitor by 5μA. (approx) When this pin turns approx. 0.9V, soft start period ends and frequency fold back function is activated.
16	FB	Error amplifier reverse input pin. Converter operates to set this pin to 0.708V. The output voltage divided by the external resistance is applied to this pin. After soft start, frequency fold back function operates when the voltage of this pin becomes 0.5V or lower. And oscillating frequency decreases together with FB voltage.

I/O pin equivalent circuit chart

Pin No.	Pin No.	Equivalent Circuit
1	COMP	
2	RT	
3	SYNC	
4	PGOOD	
5	EN	
6	SW	

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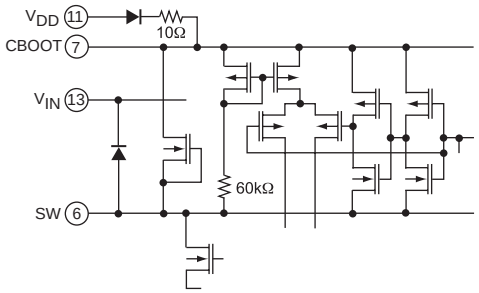
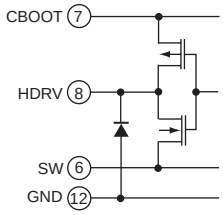
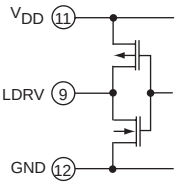
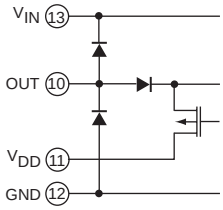
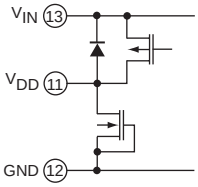
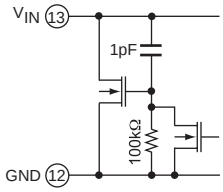
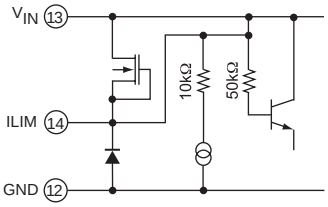
Pin No.	Pin No.	Equivalent Circuit
7	CBOOT	
8	LDRV	
9	HDRV	
10	OUT	
11	V_{DD}	
12, 13	GND, V_{IN}	
14	ILIM	

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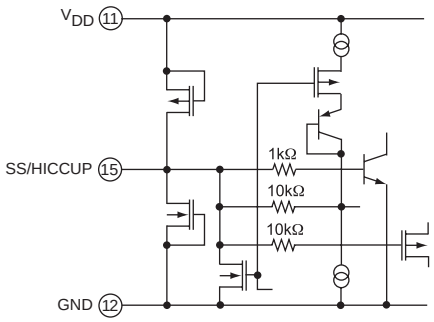
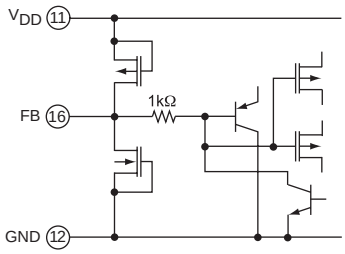
Pin No.	Pin No.	Equivalent Circuit
15	SS/HICCUP	
16	FB	

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