

# SANYO Semiconductors DATA SHEET

**Bi-CMOS LSI** 

# LV5743V — 2-channel Step-down Switching Regulator

#### Overview

The LV5743V is a 2-channel step-down switching regulator.

#### **Features**

- Provides dual switching regulator control circuits integrated on the chip.
- Output-stage push-pull structure enabling high efficient operation.
- Provides power supply (V<sub>CC</sub>-5V) for protecting the external P channel MOS gate.
- Built-in timer latch type SCP (short-circuit protection circuit)
- Built-in UVLO (Low voltage malfunction prevention circuit)
- Built-in reference voltage circuit
- Max\_On\_Duty is adjustable.

#### **Specifications**

#### **Absolute Maximum Ratings** at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
Maximum supply voltage		V <sub>CC</sub> max		35	V
Output voltage		V <sub>O</sub> max		33	V
Allowable power dissipation		Pd max	Mounted on a specified board *	0.74	W
Operating temperature		Topr		-20 to +85	°C
Storage temperature		Tstg		-55 to +150	°C
Allowa	Allowable pin voltage				
1	CT, NON1, NON2, INV1, INV2, FB1, FB2, DT1, DT2, SCP, VREF			7	V
2	V <sub>CC</sub> -5V			30	V
3	GND, OUT1, OUT2,			35	V

<sup>\*:</sup> Specified board: 114.3×76.1×1.6mm³, glass epoxy board

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# LV5743V

# Allowable Operating Ratings at $Ta=25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	Vcc		8 to 33	٧
Error amplifier input voltage	VIN		0 to 3.3	V
Timing capacitance	C <sub>CT</sub>		50 to 5000	pF
Oscillation frequency	FCT		20k to 1M	Hz

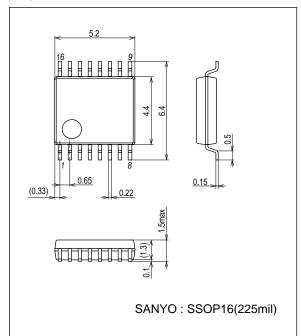
#### **Electrical Characteristics** at Ta = 25°C, $V_{CC} = 12V$

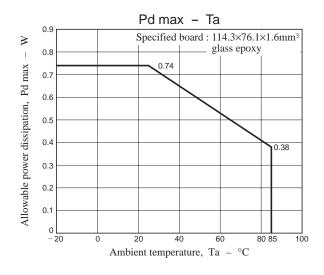
Min   Nyp   max   Nyp	Parameter	Symbol	Conditions		Ratings		
Output voltage         Vref         Iref = 1mA         2.4948         2.520         2.5452         V Input stability         VDLI         VCC = 8 to 33V         1         1 to 0         mV           Load stability         VDLO         Ivef = 0 to 5mA         1         1 to 0         mV           VI <sub>NS</sub> of Supply voltage         VNS         I <sub>QUT</sub> = 5mA         V <sub>CC</sub> -5.5         V <sub>CC</sub> -5.0         V <sub>CC</sub> -4.5         V           Triangular wave oscillator block           Tregenery fluctuation         FOSC         CCT = 220pF         320         400         480         H8         H2           Frequency fluctuation         FDV         VCC = 8 to 33V         1         1         1         0         M80         H8         H2           Protection circuit block           Trespond voltage         VT         1.5         1.7         1.9         V         Standby voltage         VSTB         50         100         mV           Standby voltage         VLT         30         100         mV         Augustable         1.6         2.1         2.6         µA           Standby voltage         VCT         1.4         1.5         1.6         2.1	Parameter	Symbol	Conditions	min	typ	max	Unit
Input stability   V_DL   V_CC = 8 to 33V   1   1   10   mV	Reference voltage block						
Load stability   V <sub>DLO</sub>   Iref = 0 to 5mA   V <sub>CC</sub> -5.5   V <sub>CC</sub> -5.0   V <sub>CC</sub> -5.0   V <sub>CC</sub> -5.5   V <sub>CC</sub> -5.0   V <sub>CC</sub> -5.5   V <sub>CC</sub> -5.5   V <sub>CC</sub> -5.0   V <sub>CC</sub> -5.5   V <sub>CC</sub> -5	Output voltage	Vref	Iref = 1mA	2.4948	2.520	2.5452	V
V <sub>IN</sub> -SV supply voltage         V <sub>NS</sub> I <sub>OUT</sub> = -5mA         V <sub>CC</sub> -5.5         V <sub>CC</sub> -6.0         V <sub>CC</sub> -4.5         V           Triangular wave oscillator block         Triangular wave oscillator block           Frequency fluctuation         F <sub>DV</sub> V <sub>CC</sub> = 8 to 33V         1         -         %           Protection circuit block         Threshold voltage         V <sub>IT</sub> 1.5         1.7         1.9         V           Standby voltage         V <sub>STB</sub> 50         1000         mV           Latch voltage         V <sub>LT</sub> 30         100         mV           Source current         I <sub>SCP</sub> 1.6         2.1         2.6         μA           Comparator threshold voltage         V <sub>CT</sub> 1.4         1.5         1.6         V           Mulescent time adjustment circuit block         V         V         0.45         0.5         0.55         V           Mores 20kHz)         V1100         Duty cycle = 0%         0.45         0.5         0.55         V           Mores 20kHz)         V1100         Duty cycle = 100%         0.95         1.0         1.06         V           Input offset voltage         V <sub>T</sub> 6.5         7         7.	Input stability	$V_{DLI}$	V <sub>CC</sub> = 8 to 33V		1	10	mV
Triangular wave oscillator block  Oscillation frequency	Load stability	$V_{DLO}$	Iref = 0 to 5mA		1	10	mV
Sociliation frequency   FOSC   CCT = 220PF   320   400   480   kHz	V <sub>IN</sub> -5V supply voltage	$V_{N5}$	I <sub>OUT</sub> = -5mA	V <sub>CC</sub> -5.5	V <sub>CC</sub> -5.0	V <sub>CC</sub> -4.5	>
Frequency fluctuation         F <sub>DV</sub> V <sub>CC</sub> = 8 to 33V         1         %           Protection circuit block           Threshold voltage         V <sub>IT</sub> 1.5         1.7         1.9         V           Standby voltage         V <sub>STB</sub> 50         100         mV           Latch voltage         V <sub>LT</sub> 30         100         mV           Source current         I <sub>SCP</sub> 1.6         2.1         2.6         μA           Comparator threshold voltage         V <sub>CT</sub> 1.4         1.5         1.6         V           Quiescent time adjustment circuit block         Input threshold voltage         VI         0.45         0.5         0.55         V           (fesc = 20kHz)         V100         Duty cycle = 0%         0.45         0.5         0.55         V           (fesc = 20kHz)         V1100         Duty cycle = 0%         0.95         1.0         1.05         V           Input bias current         I <sub>BDT</sub> DT1, DT2 = 0V         0.1         1         μA           Low voltage malfunction prevention circuit block         Input of set voltage malfunction prevention circuit block           Input of fest voltage         V <sub>ID</sub> 6         mV	Triangular wave oscillator block						
Protection circuit block   Threshold voltage	Oscillation frequency	Fosc	C <sub>CT</sub> = 220pF	320	400	480	kHz
Threshold voltage	Frequency fluctuation	$F_{DV}$	V <sub>CC</sub> = 8 to 33V		1		%
Standby voltage	Protection circuit block						
Latch voltage         VLT         30         100         mV           Source current         ISCP         1.6         2.1         2.6         μA           Comparator threshold voltage         VCT         1.4         1.5         1.6         V           Quiescent time adjustment circuit block         Unput threshold voltage         V10         Duty cycle = 0%         0.45         0.5         0.55         V           Input blas current         IBDT         DT1, DT2 = 0V         0.95         1.0         1.05         V           Input blas current         IBDT         DT1, DT2 = 0V         0.1         1         μA           Low voltage malfunction prevention circuit block         Treshold voltage         VUT         6.5         7         7.5         V           Input offset voltage         VUT         6.5         7         7.5         V           Input offset voltage         VID         9         6.5         7         7.5         V           Input offset voltage         VID         9         6.5         7         7.5         V           Input offset voltage         VID         10         30         nA         10         nA         10	Threshold voltage	VIT		1.5	1.7	1.9	V
Source current   Soc   Source current   Soc	Standby voltage	V <sub>STB</sub>			50	100	mV
Comparator threshold voltage   VCT   1.4   1.5   1.6   V	Latch voltage				30	100	mV
Quiescent time adjustment circuit block           Input threshold voltage         V10         Duty cycle = 0%         0.45         0.5         0.55         V           (fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Input bias current         IBDT         DT1, DT2 = 0V         0.1         1         µA           Low voltage malfunction prevention circuit block         Treshold voltage         VUT         6.5         7         7.5         V           Error amplifier           Input offset voltage         VID         8.5         7         7.5         V           Input offset voltage         VID         30         nA           Input offset current         IID         30         nA           Input bias current         IIB         15         100         nA           Open gain         AV         85         dB         dB           Common mode input voltage range         VOM         VCC = 8 to 33V         0         3.3         V           Common mode rejection ratio         CMRR         80         dB         dB           Maximum output voltage         VOH         2.6         V <td>Source current</td> <td>I<sub>SCP</sub></td> <td></td> <td>1.6</td> <td>2.1</td> <td>2.6</td> <td>μΑ</td>	Source current	I <sub>SCP</sub>		1.6	2.1	2.6	μΑ
Input threshold voltage   V10   Duty cycle = 0%   0.45   0.5   0.55   V     Vt100   Duty cycle = 100%   0.95   1.0   1.05   V     Input bias current   IBDT   DT1, DT2 = 0V   0.11   1   μA     Low voltage malfunction prevention circuit block     Threshold voltage   VUT   6.5   7   7.5   V     Error amplifier     Input offset voltage   VIO   6.5   7   7.5   V     Error amplifier     Input offset voltage   VIO   6   6   mV     Input offset current   IIO   30   nA     Input bias current   IIB   15   100   nA     Open gain   AV   85   dB     Common mode input voltage range   VOM   VCC = 8 to 33V   0   3.3   V     Common mode rejection ratio   CMRR   80   dB     Maximum output voltage   VOL   2.6   V     Minimum output voltage   VOL   2.6   V     Output sink current   IOI   FB = 1.25V   1   mA     Output source current   IOO   FB = 1.25V   85   μA     PVMC comparator     Input threshold voltage   V10   Duty cycle = 0%   0.45   0.5   0.55   V     Output stage on resistance (upper)   RONH   7   Ω     Output stage on resistance (lower)   RONL   2   Ω     Overall device characteristics   V100   Duty upper   V100   Duty cycle = 100%   0.95   1.0   1.05   V     Overall device characteristics   V100   Duty upper   V100   Duty cycle = 100%   0.95   1.0   1.05   V     Overall device characteristics   V100   Duty upper   V100   Duty cycle = 100%   0.95   1.0   1.05   V     Overall device characteristics   V100   Duty upper   V100   Dut	Comparator threshold voltage	VCT		1.4	1.5	1.6	V
(fosc = 20kHz)         V1100         Duty cycle = 100%         0.95         1.0         1.05         V           Input bias current         I <sub>BDT</sub> DT1, DT2 = 0V         0.1         1         μA           Low voltage malfunction prevention circuit block         Treshold voltage         V <sub>UT</sub> 6.5         7         7.5         V           Error amplifier           Input offset voltage         V <sub>IO</sub> 6         mV           Input offset current         I <sub>IO</sub> 30         nA           Input offset current         I <sub>IB</sub> 15         100         nA           Open gain         AV         85         dB           Common mode input voltage range         V <sub>OM</sub> V <sub>CC</sub> = 8 to 33V         0         3.3         V           Common mode rejection ratio         CMRR         80         dB         dB         dB           Maximum output voltage         V <sub>OH</sub> 2.6         V         V           Output sink current         I <sub>O</sub> FB = 1.25V         1         mA           PWM comparator         Input threshold voltage         V10         Duty cycle = 0%         0.45         0.5         0.55         V           Output bl	Quiescent time adjustment circuit t	olock		•			
Input bias current   IBDT   DT1, DT2 = 0V   0.1   1   μA	Input threshold voltage	Vt0	Duty cycle = 0%	0.45	0.5	0.55	V
Low voltage malfunction prevention circuit block           Threshold voltage         V <sub>UT</sub> 6.5         7         7.5         V           Error amplifier         Input offset voltage         V <sub>IO</sub> 6         mV           Input offset current         I <sub>IO</sub> 30         nA           Input bias current         I <sub>IB</sub> 15         100         nA           Open gain         AV         85         dB           Common mode input voltage range         V <sub>OM</sub> V <sub>CC</sub> = 8 to 33V         0         3.3         V           Common mode rejection ratio         CMRR         80         dB         dB           Maximum output voltage         V <sub>OH</sub> 2.6         V           Minimum output voltage         V <sub>OL</sub> 0.2         0.4         V           Output sink current         I <sub>OI</sub> FB = 1.25V         1         mA           Output source current         I <sub>OO</sub> FB = 1.25V         85         μA           PWM comparator         Input threshold voltage         Vt0         0.45         0.5         0.55         V           (fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V	(fosc = 20kHz)	Vt100	Duty cycle = 100%	0.95	1.0	1.05	V
Threshold voltage	Input bias current	I <sub>BDT</sub>	DT1, DT2 = 0V		0.1	1	μΑ
Input offset voltage	Low voltage malfunction prevention	n circuit block					
Input offset voltage	Threshold voltage	V <sub>UT</sub>		6.5	7	7.5	V
Input offset current	Error amplifier						
Input bias current   Input	Input offset voltage	V <sub>IO</sub>				6	mV
Open gain         AV         85         dB           Common mode input voltage range         VOM         V <sub>CC</sub> = 8 to 33V         0         3.3         V           Common mode rejection ratio         CMRR         80         dB           Maximum output voltage         VOH         2.6         V           Minimum output voltage         VOL         0.2         0.4         V           Output sink current         IOI         FB = 1.25V         1         mA           Output source current         IOO         FB = 1.25V         85         μA           PWM comparator           Input threshold voltage         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           Votosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Output block           Output stage on resistance (upper)         R <sub>ONL</sub> 7         Ω           Overall device characteristics	Input offset current	ΙΙΟ				30	nA
Common mode input voltage range         VOM         VCC = 8 to 33V         0         3.3         V           Common mode rejection ratio         CMRR         80         dB           Maximum output voltage         VOH         2.6         V           Minimum output voltage         VOL         0.2         0.4         V           Output sink current         IOI         FB = 1.25V         1         mA           Output source current         IOO         FB = 1.25V         85         μA           PWM comparator           Input threshold voltage         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           (fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Output block           Output stage on resistance (upper)         RONH         7         Ω           Overall device characteristics	Input bias current	I <sub>IB</sub>			15	100	nA
Common mode rejection ratio         CMRR         80         dB           Maximum output voltage         VOH         2.6         V           Minimum output voltage         VOL         0.2         0.4         V           Output sink current         I OI         FB = 1.25V         1         mA           Output source current         I OO         FB = 1.25V         85         μA           PWM comparator           Input threshold voltage         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           (fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Output block           Output stage on resistance (upper)         RONH         7         Ω           Overall device characteristics         2         Ω	Open gain	AV			85		dB
Maximum output voltage         VOH         2.6         V           Minimum output voltage         VOL         0.2         0.4         V           Output sink current         IQI         FB = 1.25V         1         mA           Output source current         IOO         FB = 1.25V         85         μA           PWM comparator           Input threshold voltage         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           (fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Output block           Output stage on resistance (upper)         RONH         7         Ω           Output stage on resistance (lower)         RONL         2         Ω           Overall device characteristics	Common mode input voltage range	Vом	V <sub>CC</sub> = 8 to 33V	0		3.3	V
Minimum output voltage   VOL   0.2   0.4   V	Common mode rejection ratio	CMRR			80		dB
Output sink current $I_{OI}$ FB = 1.25V 1 1 mA  Output source current $I_{OO}$ FB = 1.25V 85 $\mu$ A  PWM comparator  Input threshold voltage (fosc = 20kHz) Vt100 Duty cycle = 100% 0.45 0.5 0.55 V  Output block  Output stage on resistance (upper) RONH 7 $\Omega$ Output stage on resistance (lower) RONL 2 $\Omega$ Overall device characteristics	Maximum output voltage	Vон			2.6		V
Output source current $I_{OO}$ FB = 1.25V 85 $\mu$ A  PWM comparator  Input threshold voltage (fosc = 20kHz) Vt100 Duty cycle = 100% 0.45 0.5 0.55 V  Output block  Output stage on resistance (upper) RONH 7 $\Omega$ Output stage on resistance (lower) RONL 2 $\Omega$ Overall device characteristics	Minimum output voltage	V <sub>OL</sub>			0.2	0.4	V
PWM comparator           Input threshold voltage (fosc = 20kHz)         Vt0         Duty cycle = 0%         0.45         0.5         0.55         V           Output block           Output stage on resistance (upper)         RONH         7         Ω           Output stage on resistance (lower)         RONL         2         Ω           Overall device characteristics	Output sink current		FB = 1.25V		1		mA
Input threshold voltage $Vt0$ Duty cycle = 0% $0.45$ $0.5$ $0.55$ V $0.55$ V $0.55$ Duty cycle = 100% $0.95$ $0.9$	Output source current	100	FB = 1.25V		85		μА
(fosc = 20kHz)         Vt100         Duty cycle = 100%         0.95         1.0         1.05         V           Output block           Output stage on resistance (upper)         R <sub>ONH</sub> 7         Ω           Output stage on resistance (lower)         R <sub>ONL</sub> 2         Ω           Overall device characteristics	PWM comparator						
Output block  Output stage on resistance (upper) R <sub>ONH</sub> 7 Ω  Output stage on resistance (lower) R <sub>ONL</sub> 2 Ω  Overall device characteristics	Input threshold voltage	Vt0	Duty cycle = 0%	0.45	0.5	0.55	V
Output stage on resistance (upper) R <sub>ONH</sub> 7 Ω Output stage on resistance (lower) R <sub>ONL</sub> 2 Ω Overall device characteristics	(fosc = 20kHz)	Vt100	Duty cycle = 100%	0.95	1.0	1.05	٧
Output stage on resistance (lower) R <sub>ONL</sub> 2 Ω  Overall device characteristics	Output block						
Overall device characteristics	Output stage on resistance (upper)	RONH			7		Ω
Overall device characteristics	Output stage on resistance (lower)	R <sub>ONL</sub>			2		Ω
Standby current I <sub>CCS</sub> When output is off 5 mA	Overall device characteristics						
	Standby current	lccs	When output is off			5	mA

# **Package Dimensions**

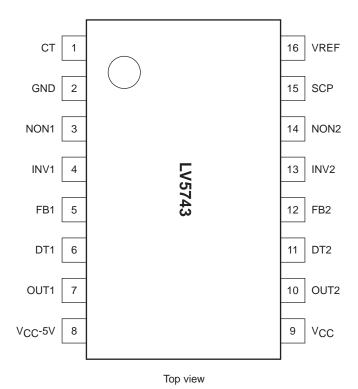
unit: mm (typ)

3178B





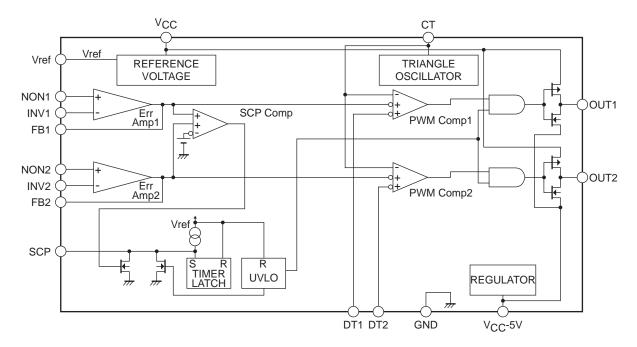
## **Pin Assignment**



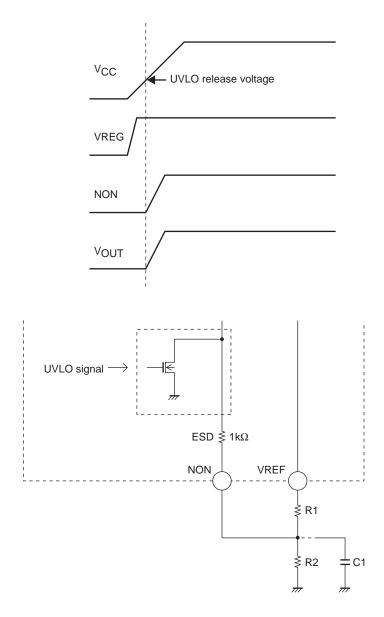
#### **Pin Function**

Pin No.	Pin Name	Description	
1	СТ	External timing capacitor connection pin	
2	GND	Ground	
3	NON1	Error amplifier 1 input (+)	
4	INV1	Error amplifier 1 input (-)	
5	FB1	Error amplifier 1 output	
6	DT1	Output 1 maximum duty setting	
7	OUT1	Output 1	
8	V <sub>CC</sub> -5V	Power supply for output stage drive	
9	V <sub>CC</sub>	Power supply	
10	OUT2	Output 2	
11	DT2	Output 2 maximum duty setting	
12	FB2	Error amplifier 2 input (+)	
13	INV2	Error amplifier 2 input (-)	
14	NON2	Error amplifier 2 output	
15	SCP	Timer latch setting	
16	VREF	Reference voltage output	

### **Block Diagram**

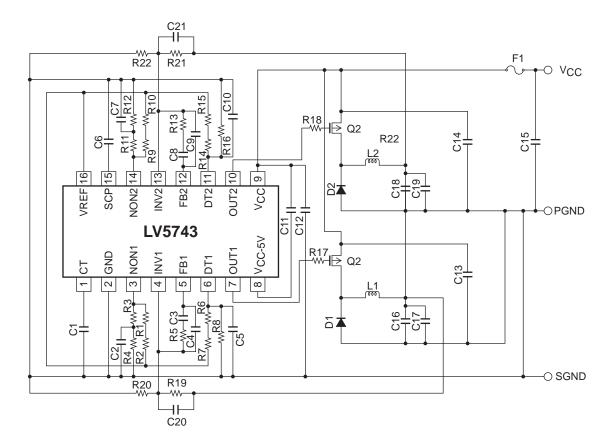


#### **Timing Chart**



<sup>\*</sup> The voltage at the NON pin is  $\{VREF/(R1+1k)\}\times 1k$  in UVLO mode.

#### **Sample Application Circuit Diagram**



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