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# LV5749NV

Bi-CMOS LSI

## 1-channel Step-down Switching Regulator

### Application

The LV5749NV is a 1-channel step-down switching regulator.

### Functions

- 1 channel step-down switching regulator controller.
- Load-independent soft start circuit.
- ON/OFF function.
- Built-in pulse-by-pulse OCP circuit. It is detected by using ON resistance of an external MOS.
- Synchronous rectification.
- Current mode control.
- Synchronous drive by external signal.

### Specifications

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
supply voltage	V <sub>IN</sub> max		45	V
Allowable Power dissipation	P <sub>d</sub> max	Mounted on a specified board. *	0.74	W
Operating temperature	T <sub>opr</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

\* : When mounted on the specified printed circuit board (114.3mm × 76.1mm × 1.6mm), glass epoxy

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### Recommended Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V <sub>IN</sub>		8.5 to 42	V
Error amplifier input voltage			0 to 1.6	V

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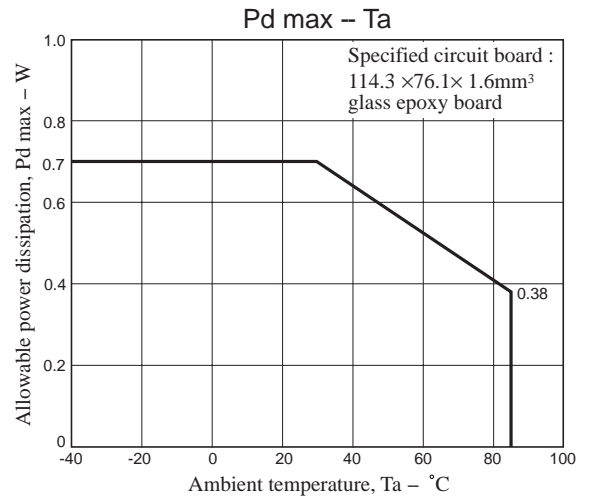
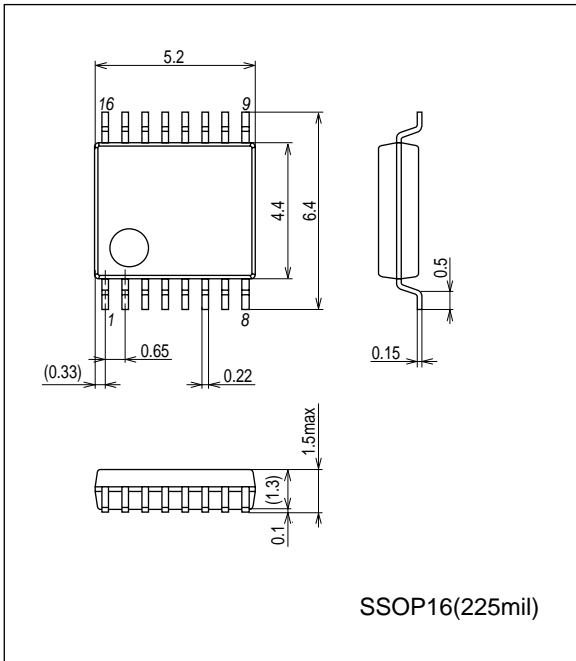
**Electrical Characteristics** at  $T_a = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>Reference voltage block</b>						
Internal reference voltage	$V_{ref}$	Including offset of E/A	0.654	0.67	0.686	V
5V power supply	$V_{DD}$	$I_{OUT} = 0$ to 5mA	4.7	5.2	5.7	V
<b>Triangular waveform oscillator block</b>						
Oscillation frequency	$F_{OSC}$	$RT = 220\text{k}\Omega$	110	125	140	kHz
Frequency variation	$F_{OSC DV}$	$V_{IN} = 8.5$ to 42V		1		%
<b>ON/OFF circuit block</b>						
IC start-up voltage	$V_{EN on}$		2.5	3.0	3.5	V
IC off voltage	$V_{EN off}$		1.1	1.3	1.5	V
<b>Soft start circuit block</b>						
Soft start source current	$I_{SS SC}$	$EN > 3.5\text{V}$	4	5	6	$\mu\text{A}$
Soft start sink current	$I_{SS SK}$	$EN < 1\text{V}$ , $V_{DD}=5\text{V}$		2		mA
<b>UVLO circuit block</b>						
UVLO lock release voltage	$V_{UVLO}$		7.5	8.0	8.5	V
UVLO hysteresis	$V_{UVLO H}$			0.7		V
<b>OCP circuit block</b>						
OCP charge current	$I_{OCP}$			5		$\mu\text{A}$
<b>Error amplifier</b>						
Input bias current	$I_{EA IN}$				100	nA
Error amplifier transconductance	$G_{EA}$		1000	1400	1800	$\mu\text{A/V}$
Sink output current	$I_{EA OSK}$	$FB = 1.0\text{V}$		-100		$\mu\text{A}$
Source output current	$I_{EA OSC}$	$FB = 0\text{V}$		100		$\mu\text{A}$
Current detection amplifier gain	$G_{ISNS}$			1.5		
<b>Over current limiter circuit block</b>						
Reference current 1	$I_{LIM1}$	$MODE = L (GND)$	-10%	18.5	+10%	$\mu\text{A}$
Reference current 2	$I_{LIM2}$	$MODE = H (V_{IN})$	-10%	37.0	+10%	$\mu\text{A}$
Over current detection comparator offset voltage	$V_{LIM OFS}$		-5		+5	mV
Over current detection comparator common mode input range			$V_{IN}-0.45$		$V_{IN}$	V
<b>PWM comparator</b>						
Input threshold voltage ( $f_{osc} = 125\text{kHz}$ )	$V_t \text{ max}$	Duty cycle = DMAX	0.9	1.0	1.1	V
	$V_t 0$	Duty cycle = 0%	0.4	0.5	0.6	V
Maximum ON duty	DMAX		80	85	90	%
<b>Output block</b>						
Output stage ON resistance (the upper side)	$R_{ONH}$			5		$\Omega$
Output stage ON resistance (the under side)	$R_{ONL}$			5		$\Omega$
Output stage ON current (the upper side)	$I_{ONH}$		240			mA
Output stage ON current (the under side)	$I_{ONL}$		240			mA
<b>The whole device</b>						
Standby current	$I_{CCS}$	$EN < 1\text{V}$			10	$\mu\text{A}$
Mean consumption current	$I_{CCA}$	$EN > 3.5\text{V}$		3		mA

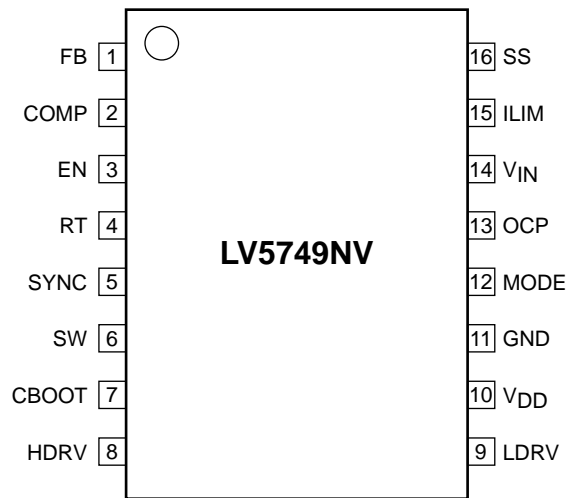
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## Package Dimensions

unit : mm (typ)  
3178B



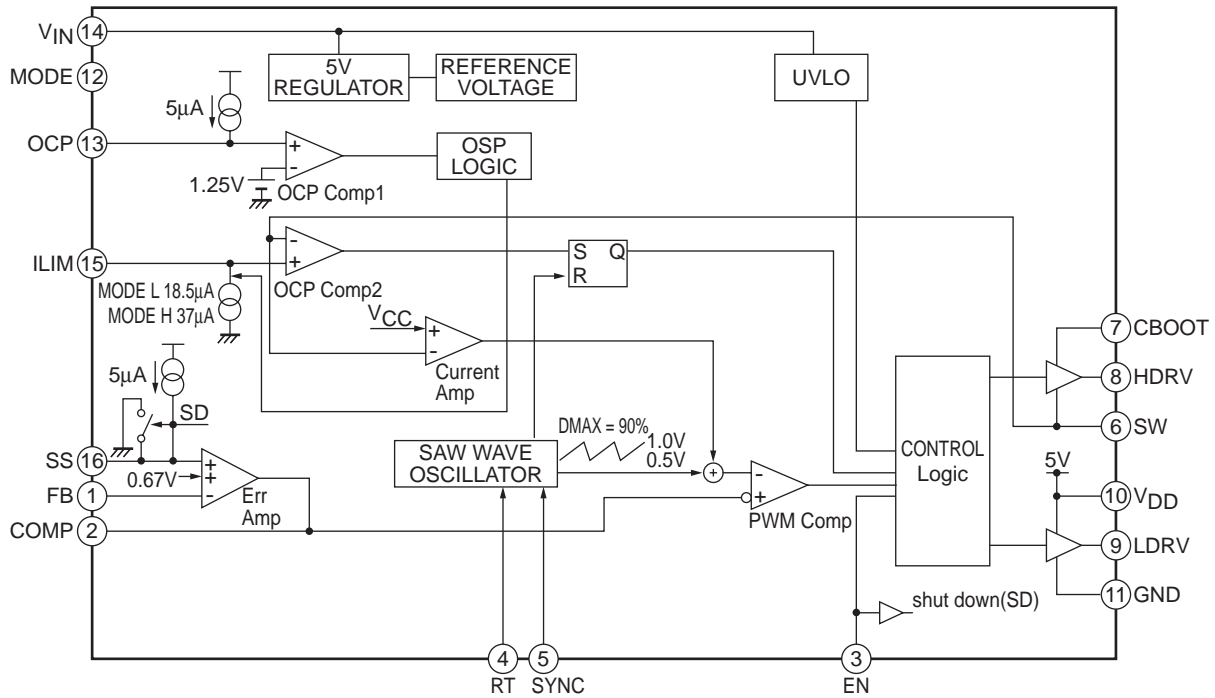
## Pin Assignment



Top view

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## Block Diagram



## Pin Function

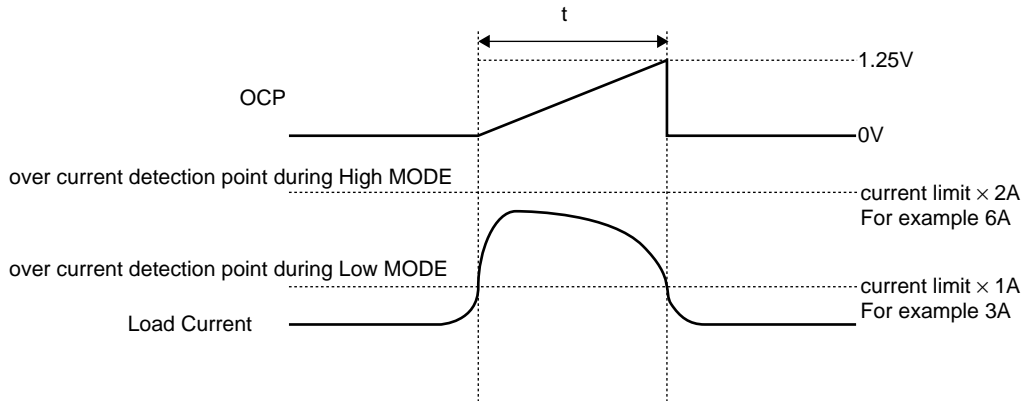
Pin No.	Pin name	Description
14	V <sub>IN</sub>	Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes 7.7V or more by UVLO function, The IC starts and the soft start function operates.
11	GND	Ground pin. Each reference voltage is based on the voltage of the ground pin.
10	V <sub>DD</sub>	Power supply pin for an external the lower MOS-FET gate drive.
7	CBOOT	Bootstrap capacity connection pin. This pin becomes a GATE drive power supply of an external NchMOSFET. Connect a bypath capacitor between CBOOT and SW.
6	SW	Pin to connect with switching node. The source of NchMOSFET connects to this pin.
5	SYNC	External synchronous signal input pin.
9	LDRV	An external the lower MOSFET gate drive pin.
8	HDRV	An external the upper MOSFET gate drive pin.
1	FB	Error amplifier reverse input pin. By operating the converter, the voltage of this pin becomes 0.67V. The voltage in which the output voltage is divided by an external resistance is applied to this pin.
2	COMP	Error amplifier output pin. Connect a phase compensation circuit between this pin and GND.
16	SS	Pin to connect a capacitor for soft start. A capacitor for soft start is charged by using the voltage of about 5μA. This pin ends the soft start period by using the voltage of about 1.1V and the frequency fold back function becomes active.
15	ILIM	Reference current pin for current detection. The sink current of about 20μA flows to this pin when Low level (GND) is set to the MODE pin. Also, the sink current of about 40μA flows to this pin when High level (V <sub>IN</sub> ) is set to the MODE pin. When a resistance is connected between this pin and V <sub>IN</sub> outside and the voltage applied to the SW pin is lower than the voltage of the terminal side of the resistance, the upper NchMOSFET is off by operating the current limiter comparator. This operation is reset with respect to each PWM pulse.
3	EN	ON/OFF pin.
13	OCP	Pin to set the time of the timer (during double the over current detection point) Connect a capacitor between this pin and GND. OCP charge current : 5μA
4	RT	Pin to set the oscillation frequency. Connect a resistance between this pin and GND.
12	MODE	Pin to switch the over current detection point. Set by the low level (GND) of the ILIM pin. Set by the high level (V <sub>IN</sub> ) of the OCP pin. When this MODE pin is set to the high level and the point of the over current detection is set by using the ILIM pin is exceeded, the value becomes double the original value. Also, when the MODE pin is set to the low level, the point of the over current detection remains an original value.

**Timing Chart**

When the MODE pin is set to the high level and the point of the over current detection is set by using the ILIM pin is exceeded, the value becomes double the original value.

Also, when the MODE pin is set to the low level, the point of over current detection remains an original value.

Timing chart of the over current detection point switching is as below.



**Setting Chart**

1. Output voltage setting

- Setting of the output voltage VOUT is as follows.

$$V_{OUT} = 1 + \frac{R4}{R3} \times V_{REF} = 1 + \frac{R4}{R3} \times 0.67(\text{typ}) \text{ [V]}$$

2. Soft Start setting

- Setting of capacitor C5 is as follows.

$$C5 = \frac{I_{ss} \times T_{ss}}{V_{REF}} = \frac{5\mu \times T_{ss}}{0.67} \text{ [F]}$$

I<sub>ss</sub> : Charge current value.

T<sub>ss</sub> : Soft Start time

3. OCP Timer setting

- Setting of OCP timer capacitor C11 is as follows.

$$C11 = \frac{I_{ocp} \times T_{ocp}}{V_{ocp \text{ comp1}}} = \frac{5\mu \times T_{ocp}}{1.3} \text{ [F]}$$

I<sub>ocp</sub> : Charge current value.

T<sub>ocp</sub> : OCP time

4. Current limiter setting

- Setting of the current limiter set resistance R5 is as follows.

$$R5 = \frac{R_{dson} \times I_{out}}{I_{lim}} = \frac{R_{dson} \times I_{L \text{ max}}}{18.5\mu} \text{ [\Omega]}$$

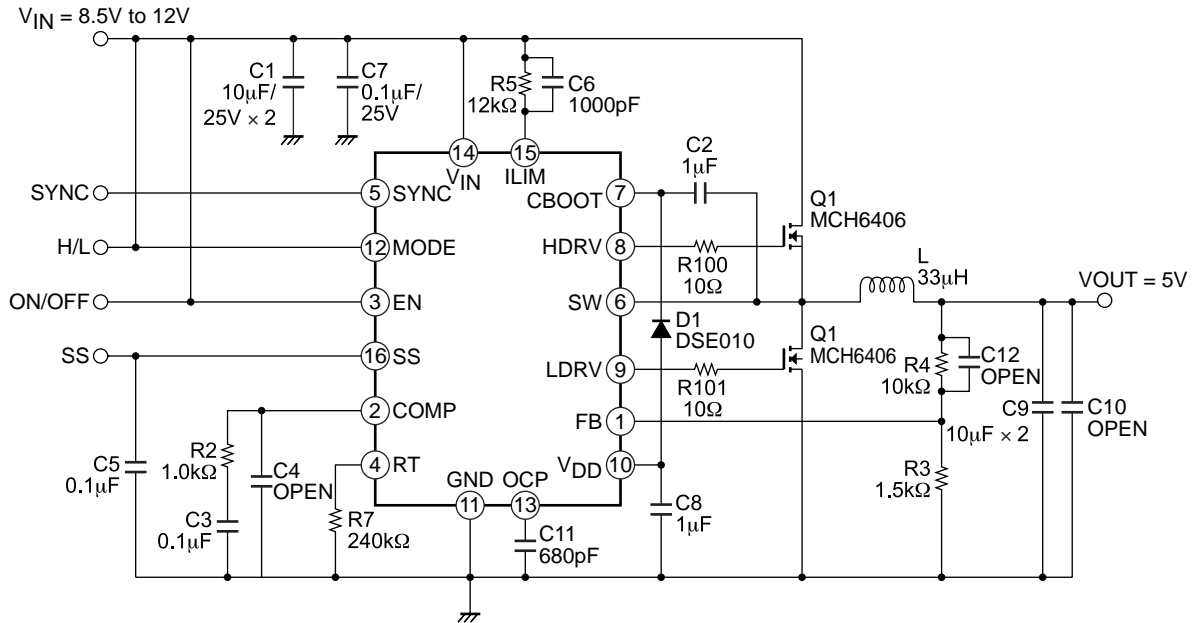
I<sub>lim</sub> : ILIM current value.

I<sub>L</sub> : inductance current value

R<sub>dson</sub> : ON resistance value between Q1 drain-sources.

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## Sample Application Circuit



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