



SANYO Semiconductors

# DATA SHEET

An ON Semiconductor Company

## LV5856MX — Bi-CMOS IC Step-down Switching Regulator

### Overview

LV5856MX is a 1ch step-down switching regulator. With built-in two 0.13Ω power MOSFET switch, it achieves high output current and high efficiency. With low-heat resistance, miniature package MFP8 (200mil) with heat-sink is adopted. Since it is Current mode control type, it has good load current response, and phase compensation is easy. With ON/OFF pin, operating can be less than 60μA at stand-by mode. It has cycle-by-cycle over current protection for load devices. With external capacitor, it achieves soft start.

### Functions

- 3A 1ch step-down
- Small package: MFP8 (200mil) with heat sink
- High efficiency (93%  $I_{OUT} = 1A$ ,  $V_{IN} = 12V$ ,  $V_O = 5V$ )
- Standby mode
- Over-current protection(HICCUP)
- Thermal shutdown protection
- Reference voltage: 0.923V
- Fixed frequency: 340kHz
- Soft start / Soft stop

### Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input $V_{IN}$ voltage	$V_{IN\ max}$		20	V
BOOT pin maximum voltage	$V_{BT\ max}$		25	V
SW pin maximum voltage	$V_{SW\ max}$		$V_{IN\ max}$	V
BOOT pin-SW pin maximum voltage	$V_{BS-SW\ max}$		7	V
EN Maximum Voltage	$V_{EN\ max}$		20	V
FB, COMP, SS pin maximum voltage	$V_{fs\ max}$		7	V
Allowable power dissipation	$P_d\ max$	Mount on a specified board *	2.05	W
Junction temperature	$T_j\ max$		150	$^\circ\text{C}$
Operating temperature	$T_{opr}$		-20 to 80	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to 150	$^\circ\text{C}$

Specified substrate : 46.0mm x 32.0mm x 1.6mm glass epoxy substrate.

Note: Plan the maximum voltage while including coil and surge voltages, so that the maximum voltage is not exceeded even for an instant.

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# LV5856MX

## Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V <sub>IN</sub> pin voltage	V <sub>IN</sub>		8 to 18	V
BOOT pin voltage	V <sub>BT</sub>		-0.3 to 23	V
SW pin voltage	V <sub>SW</sub>		-0.4 to V <sub>IN</sub>	V
BOOT pin-SW pin voltage	V <sub>BS-SW</sub>		6.5	V
EN voltage	V <sub>EN</sub>		18	V
FB, COMP, SS pin voltage	V <sub>FSO</sub>		6	V

## Electrical Characteristics at Ta = 25°C, V<sub>IN</sub> = 12V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
IC current drain at standby	I <sub>CC1</sub>	EN=0V		60		μA
IC current drain in operation	I <sub>CC2</sub>	EN=5V, FB=1V		2.5		mA
Efficiency	Effcy	V <sub>IN</sub> =12V, I <sub>OUT</sub> =1A, V <sub>o</sub> =5V, Design target *2		93		%
Reference voltage	V <sub>ref</sub>	V <sub>IN</sub> =8V to 28V (±2%)	-2%	0.923	+2%	V
FB pin bias current	I <sub>ref</sub>	FB=0.923V		10	100	nA
High-side ON resistance	R <sub>onH</sub>	BOOT=5V, I <sub>OUT</sub> =1A		0.13		Ω
Low-side ON resistance	R <sub>onL</sub>			0.13		Ω
Oscillation frequency	f <sub>OSC</sub>			340		kHz
Oscillation frequency during short-circuit protection	f <sub>OSCS</sub>			100		kHz
EN high-threshold voltage	V <sub>enth</sub>			1.5		V
Maximum ON DUTY	D max		80			%
Minimum ON DUTY	D min				8	%
SW Peak Current limit	I <sub>cl1</sub>	V <sub>IN</sub> =12V, V <sub>OUT</sub> =5V, L=10μH	4			A
Thermal shutdown temperature	T <sub>tsd</sub>	*Design guarantee *3		160		°C
Thermal shutdown temperature hysteresis	D <sub>tsd</sub>	*Design guarantee *3		40		°C
Soft start current	I <sub>SS</sub>	SS=0V		6		μA
Discharge On-Resistance	V <sub>SWON</sub>			35		Ω
V <sub>IN</sub> UVLO lock voltage	V <sub>UVLO<sup>L</sup></sub>			6.0		V
V <sub>IN</sub> UVLO lock release voltage	V <sub>UVLO<sup>H</sup></sub>			6.9		V

\*2: Reference value (not tested before shipment)

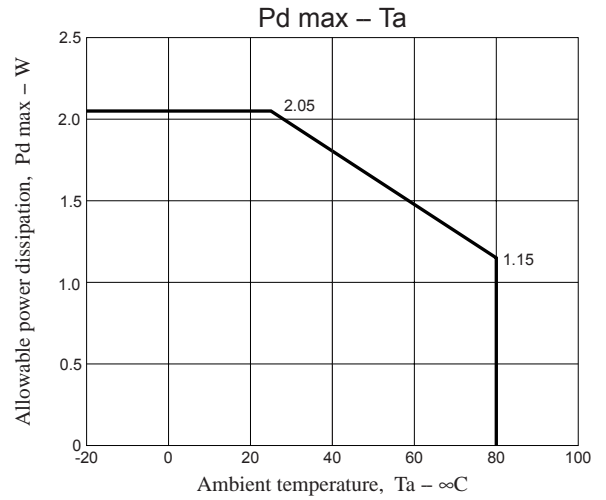
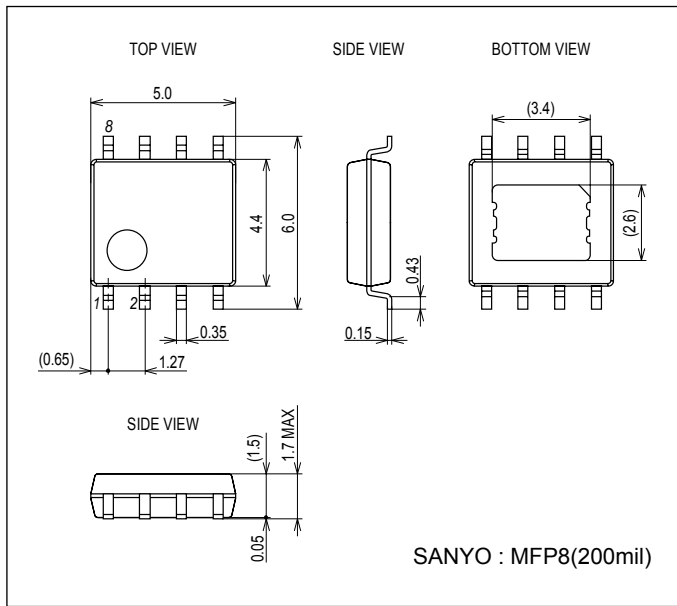
\*3: Design guarantee (value guaranteed by design and not tested before shipment)

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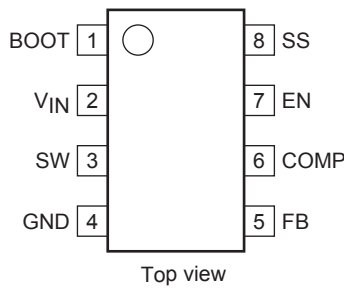
## Package Dimensions

unit : mm (typ)

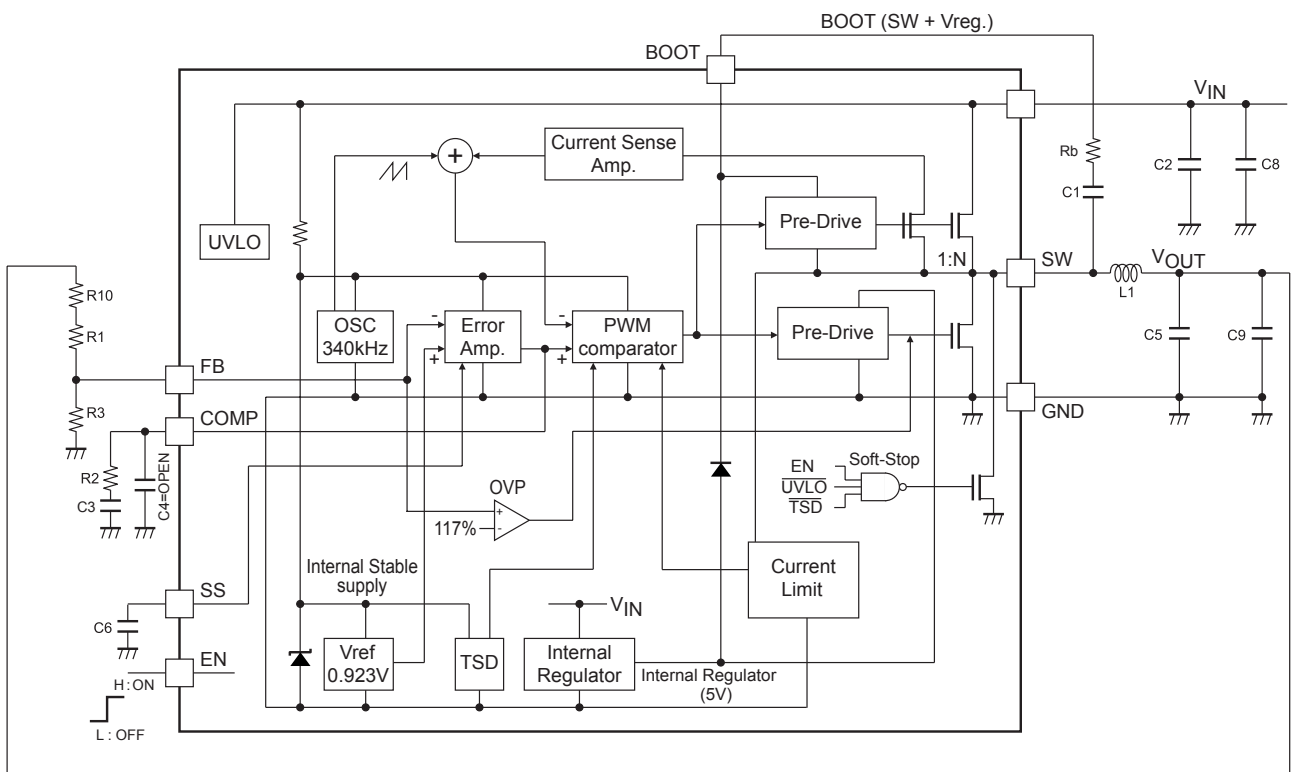
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## Pin Assignment



## Block Diagram and Sample Application Circuit



C1,C2,C5,C8,C9=Ceramic capacitor

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## Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	BOOT	Upper MOS transistor boot strap capacitance connection pin. Connect the boot capacitance of about 0.1uF between SW pins. To protect the SW pin's absolute maximum rating , to ensure stable operation, and to eliminate noise , the boot capacitance serial resistance (about 15Ω) Rb proves effective.	
2	V <sub>IN</sub>	Input Voltage Pin. Connect substantially large (10uF 2 parallel or more) capacitance between this pin and GND.	
3	SW	Power Switch pin. Connect the output LC filter. Connect the above capacitance between this pin and BOOT pin. The discharge transistor for a Soft-Stop is connected with this terminal (typcal 35Ω). It turns it on by either EN=L, UVLO or a thermal shutdown.	
4	GND	Ground pin.	
5	FB	Feedback pin. Set the output voltage by means of split resistor in the section of the output voltage V <sub>OUT</sub> -FB-GND. V <sub>OUT</sub> setting is made as calculated below. $V_{OUT} = V_{ref} \times \left\{ 1 + \frac{(R1 + R10)}{R3} \right\}$ V <sub>ref</sub> = 0.923V Example: 3.3V output voltage (See, Block Diagram and Application example) $V_{OUT} = 0.923 \times \left\{ 1 + \frac{(22k + 3.9k)}{10k} \right\}$ =3.314V	
8	SS	Soft start pin. Sets the soft start time by means of the built-in 6μA source voltage and external soft start capacity. The soft start capacity C6 can be set as follows: $C6 = 6\mu A \times \frac{T_{ss}}{V_{ref}}$ Where, T <sub>ss</sub> is the soft start time and V <sub>ref</sub> is the reference voltage. Example:2.3ms soft start time achieved $C6 = 6\mu A \times \frac{2.3ms}{0.923V} = 0.015\mu F$	
6	COMP	Phase compensation pin. Connects with the phase compensation external capacitance and resistance of DC/DC converter close loop.	
7	EN	Enable pin. Converter enabled when set to the HIGH voltage and disabled when LOW voltage or OPEN state.	

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