Ordering number : ENA1992

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV7109E — AC Switch Europe SCART Standard

Overview

The LV7109E is a rationalized IC of AC switch LV7108 complying with the Europe SCART standard.

Features and functions

- Video/Audio Canal-SW
- 6dB-VideoAmp
- 6MHz/12MHz/27MHz-LowPassFilter
- 9ch VideoDriver (AV1/AV2/Line/RGB/Component)
- V-Sync. Detection
- 3ch Stereo Audio Input
- 2ch Stereo Audio Output

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	$V_{CC}1$ max		6.0	V
Maximum supply voltage 2	$V_{CC}2$ max		13.0	V
Recommended supply voltage 1	$V_{CC}1$		5.0	V
Recommended supply voltage 2	$V_{CC}2$		12.0	V
Operating supply range 1	$V_{CC}1$ opg		4.5 to 5.3	V
Operating supply range 2	$V_{CC}2$ opg		11.1 to 12.5	V
Allowable power dissipation	Pd max	* With specified substrate	1070	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-40 to +150	°C

* With specified substrate : 76.1mm × 114.3mm × 1.6mm, glass epoxy.

Electrical Characteristics at Ta = 25°C, $V_{CC}V$ = 5.0V, $V_{CC}A$ = 12V

Parameter	Symbol	Input point	Output point	Test condition	Ratings min	Ratings typ	Ratings max	Unit
Current dissipation 1 (5V)	$I_{CC}1$			Non-signal	69.7	82.0	94.3	mA
Current dissipation 2 (ALL5V)	$I_{CC}2$			Non-signal	11.1	13.0	15.0	mA
Current dissipation 3 (12V)	$I_{CC}3$			Non-signal	7.7	9.0	10.4	mA
Video Canal SW part								
Output voltage 1	VDCC			AV1, AV2-OUT (Sync tip)	0.5	0.7	0.9	V
Voltage gain	VGC			V_{IN} = 1Vp-p, f = 100kHz, AV1, AV2-OUT	5.5	6.0	6.5	dB
Frequency characteristics 1	VFC1	17 38	12	V_{IN} = 1Vp-p, f = 10MHz/100kHz (P17, P19: Through)	-1.0	0.0	+1.0	dB
Frequency characteristics 2	VFC2	40		V_{IN} = 1Vp-p, f = 6MHz/100kHz (P38, P40: 6MHz-LPF)	-1.5	0.0	+1.5	dB
DG Differential gain	DGC	19		V_{IN} = Video : 1Vp-p	-1	0	+1	%
DP Differential phase	DPC	38	14	V_{IN} = Video : 1Vp-p	-1.5	0	+1.5	°C
Cross talk between channel	CTC	40		Selected input = GND Non-selected input = 1Vp-p, f = 4.43MHz		-60	-50	dB
Picture S/N	VSNC			V_{IN} = Video (50%White)		-70	-65	dB
Maximum output level 1	V_OMAXC1	17 19	12 14	Output level (Trough output) whose linearity exceeds 1% V_{IN} = Linearity (lamp) signal Output level at linearity 1%	2.8	3.0		Vp-p
Maximum output level 2	V_OMAXC2	38 40	12 14	Output level (ENC output) whose linearity exceeds 1% V_{IN} = Linearity (lamp) signal Output level at linearity 1%	2.6	2.7		Vp-p
Video INPUT SW part								
Output voltage 1	VDCI1	17, 19, 21	35	Composite (Sync-Tip)	0.8	1.0	1.2	V
Output voltage 2	VDCI2	17, 19, 21	35	Y (Sync-Tip)	0.8	1.0	1.2	V
Output voltage 3	VDCI3	3	33	Chroma (Center)	1.8	2.1	2.4	V
Voltage gain 1	VGI1	17, 19, 21 3	33 35	V_{IN} = 1Vp-p, f = 100kHz, load = 10kΩ	-0.5	0.0	+0.5	dB
Frequency characteristics	VFI	17, 19, 21 3	33 35	V_{IN} = 1Vp-p, f = 10MHz/100kHz	-1.0	0.0	+1.0	dB
DG Differential Gain	DGSW	17, 19, 21	35	V_{IN} = Video :1Vp-p	-1	0	+1	%
DP Differential Phase	DPSW	17, 19, 21	35	V_{IN} = Video :1Vp-p	-1.5	0	+1.5	°C
Cross talk between channel	CTAD	17, 19, 21 3	33 35	Selected input = GND Non-selected input = 1Vp-p, f = 4.43MHz		-60	-50	dB
Picture S/N	VSNC	17, 19, 21	35	V_{IN} = Video (50%White)		-66	-60	dB
Maximum output level	V_OMAXSW	17, 19, 21	35	Output level (ENC output) whose linearity exceeds 1% V_{IN} = Linearity (lamp) signal Output level at linearity 1%	1.8	2.0		Vp-p
Video Driver part								
Output voltage 1	VDCD1	64, 46 1, 44 3, 42	6 8 10	RGB (Pedestal)	0.6	0.8	1.0	V
Output voltage 2	VDCD2	40	16 27	CVBS (Sync tip) Y (Sync tip)	0.5	0.7	0.9	V
Output voltage 3	VDCD3	3 46 42	10 23 25	C, Pr, Pb (Center)	1.7	2.0	2.3	V
Output voltage 4	VDCD4	40	27	Y (Sync tip)	0.8	1.0	1.2	V
Voltage gain 1	VGD1	64, 46 1, 44 3, 42 40, 38	6, 23 8, 27 10, 25 12, 14, 16	For V_{IN} = 1Vp-p and f = 100kHz Line output only: 2 drives, Other outputs: 1drive	5.5	6.0	6.5	dB

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Parameter	Symbol	Input point	Output point	Test condition	Ratings min	Ratings typ	Ratings max	Unit
Frequency characteristics 1	VFD1	46, 44, 42 40, 38	6, 8, 10 23, 27, 25 12, 14 16	V_{IN} = 1Vp-p, f = 6MHz/100kHz when 6MHzLPF is selected	-1.5	0.0	+1.5	dB
Frequency characteristics 2	VFD2	46 44 42	6 8 10	f = 27MHz/100kHz when 6MHzLPF is selected		-35	-25	dB
Frequency characteristics 3	VFD3	46 44 42	23 27 25	f = 12MHz/100kHz when 12MHzLPF is selected	-1.5	0.0	+1.5	dB
Frequency characteristics 4	VFD4	46 44 42	23 27 25	f = 54MHz/100kHz when 12MHzLPF is selected		-40	-30	dB
Frequency characteristics 5	VFD5	46 42	23 25	f = 13.5MHz/100kHz when 13.5MHzLPF is selected	-1.5	0.0	+1.5	dB
Frequency characteristics 6	VFD6	46 42	23 25	f = 74MHz/100kHz when 13.5MHzLPF is selected		-40	-30	dB
Frequency characteristics 7	VFD7	44	27	f = 25MHz/100kHz when 27MHzLPF is selected	-1.5	0.0	+1.5	dB
Frequency characteristics 8	VFD8	44	27	f = 74MHz/100kHz when 27MHzLPF is selected		-40	-30	dB
Group delay 1	VGDD1	46, 44, 42 40, 38	6, 8, 10 23, 27, 25 12, 14 16	f = 6MHz/100kHz when 6MHzLPF is selected		20	35	ns
Group delay 2	VGDD2	46 44 42	23 27 25	f = 12MHz/100kHz when 12MHzLPF is selected		14	25	ns
Group delay 3	VGDD3	46 42	23 25	f = 27MHz/100kHz when 13.5MHzLPF is selected		10	18	ns
Group delay 4	VGDD4	44	27	f = 27MHz/100kHz when 27MHzLPF is selected		10	18	ns
Mute attenuation	VMUD		ALL	V_{IN} = 1Vp-p, f=4.43MHz		-60	-50	dB
DG Differential gain	DG1		ALL	V_{IN} = Video : 1Vp-p	-1	0	+1	%
DP Differential phase	DP1		ALL	V_{IN} = Video : 1Vp-p	-1.5	0	+1.5	°C
Cross talk between channel	CTD		ALL	V_{IN} = 1Vp-p, f=4.43MHz Driver output terminated with 75Ω		-60	-50	dB
Picture S/N	VSND		ALL	V_{IN} = Video (50%White)		-70	-65	dB
Maximum output level 1	V_OMAXD1	64, 46 1, 44 3, 42	6 8 10	Output level (RGB) whose linearity exceeds 1% V_{IN} = Linearity (lamp) signal Output level at linearity 1%	2.5	2.7		Vp-p
Maximum output level 2	V_OMAXD2	40	16 27	Output level (brightness, CVBS) whose linearity exceeds 1% V_{IN} = Linearity (lamp) signal Output level at linearity 1%	2.6	2.8		Vp-p
Maximum output level 3	V_OMAXD3	46 42	23 25	Output level (color difference) whose linearity exceeds 1% V_{IN} = sin 10kHz Output level at linearity 1%	2.0	2.5		Vp-p
Sync-SEP part								
V.SYNC output High voltage	VVSH	17, 19, 21	34		4.3	4.7	5.0	V
V.SYNC output Low voltage	VVSL	17, 19, 21	34		0.0	0.3	0.6	V
V.SYNC output delay time	TDVS	17, 19, 21	34	Note 2)	7	15	25	μs
V.SYNC output pulse width	TWVS	17, 19, 21	34	V_{IN} = PAL Video : 1Vp-p Note 2)	125	155	185	μs

Note 2) When pin 10 is open

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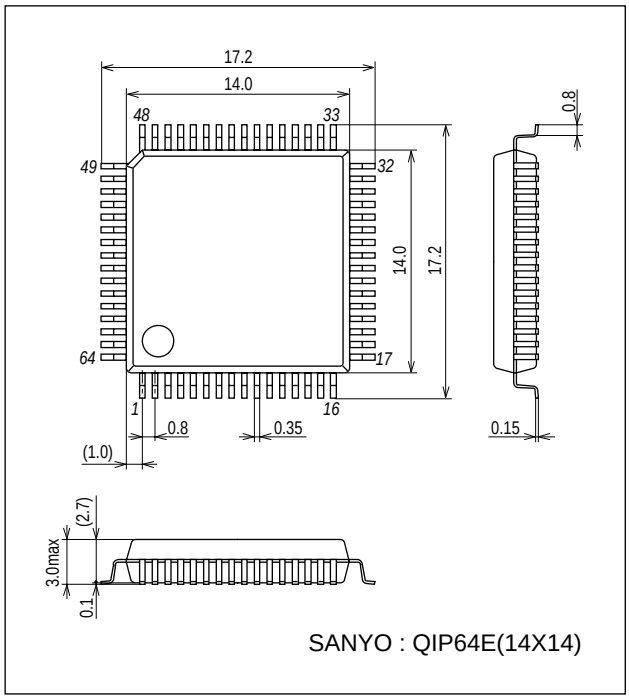
Parameter	Symbol	Input point	Output point	Test condition	Ratings min	Ratings typ	Ratings max	Unit
Audio canal switches part								
Maximum output level	V_OMAXC	R-Ch. 49, 50, 51 L-Ch. 54, 55, 56	R-Ch. 58, 61 L-Ch. 59, 62	AV1, AV2-OUT (L, R) Output level at f = 1kHz, THD = 1% BW = 400 to 30kHz	2.2	2.5		Vrms
Channel balance	CVSW			V_{IN} = 2Vrms, f = 1kHz Lch Gain-Rch Gain	-1.5	0.0	+1.5	dB
Total harmonic distortion	THDAC			V_{IN} = 2Vrms, f = 1kHz, BW = 400 to 30kHz		0.003	0.01	%
Output noise voltage	VNAC			Rg = 0Ω, BW = JIS-A		-100	-80	dBV
Mute attenuation	VMUAC			V_{IN} = 2Vrms, f = 1kHz, BW = JIS-A 20log (V_{OUT}/V_{IN})		-90	-75	dB
Input impedance	Z_{IN}				80	100	120	kΩ
Cross talk between channel and selctors	CTSW			V_{IN} = 2Vrms, f = 1kHz Rg = 0Ω, BW = JIS-A		-110	-80	dB
Output off set voltage	V_{OFSET}			Off set voltage at the time of changeover SW.	-20	0	+20	mV
External control part								
I^2C-BUS High level input voltage	V_{IH}	36 37			2.5		V_{CC}5	V
I^2C-BUS Low level input voltage	V_{IL}	36 37			GND		0.8	V
FSS output H voltage	VHFSS		7	Serial control select FSS OUT H, load = 10kΩ external output resistor 470 recommended	10.6	11.1	11.6	V
FSS output M voltage	VMFSS		7	Serial control select FSS OUT M, load = 10kΩ external output resistor 470 recommended	5.5	6.3	7.0	V
FSS output L voltage	VLFSS		7	Serial control select FSS OUT, load = 10kΩ	0.0	0.1	0.5	V
FSS risinge time	TFSSLH		7				1.0	ms
FB output H voltage	VHFB		18	Serial control select FB OUT H, load = 150Ω	3.0	4.0	5.0	V
FB output L voltage	VLFB		18	Serial control select FB OUT L, load = 150Ω	0.0	0.2	0.4	V
FB external control L range	VLFBIN	20	18	Pin 20 input voltage range at which the pin 18 output becomes “L”.	0.0		0.5	V
FB external control H range	VHFBIN	20	18	Pin 20 input voltage range at which the pin 18 output becomes “H”.	1.0		3.0	V
External control output H voltage	V_{EXTH}		26	2kΩ load for data 1	4.0	4.5	5.0	V
External control output L voltage	V_{EXTL}		26	2kΩ load for data 0	0.0	0.3	1.0	V
Internal reference regulator								
REG2.5V	VREG25		2 31		2.3	2.5	2.7	V
REG9.0V	VREG90		52 57		8.7	9.0	9.3	V
VRE4.5	VREG45		48		4.3	4.5	4.7	V

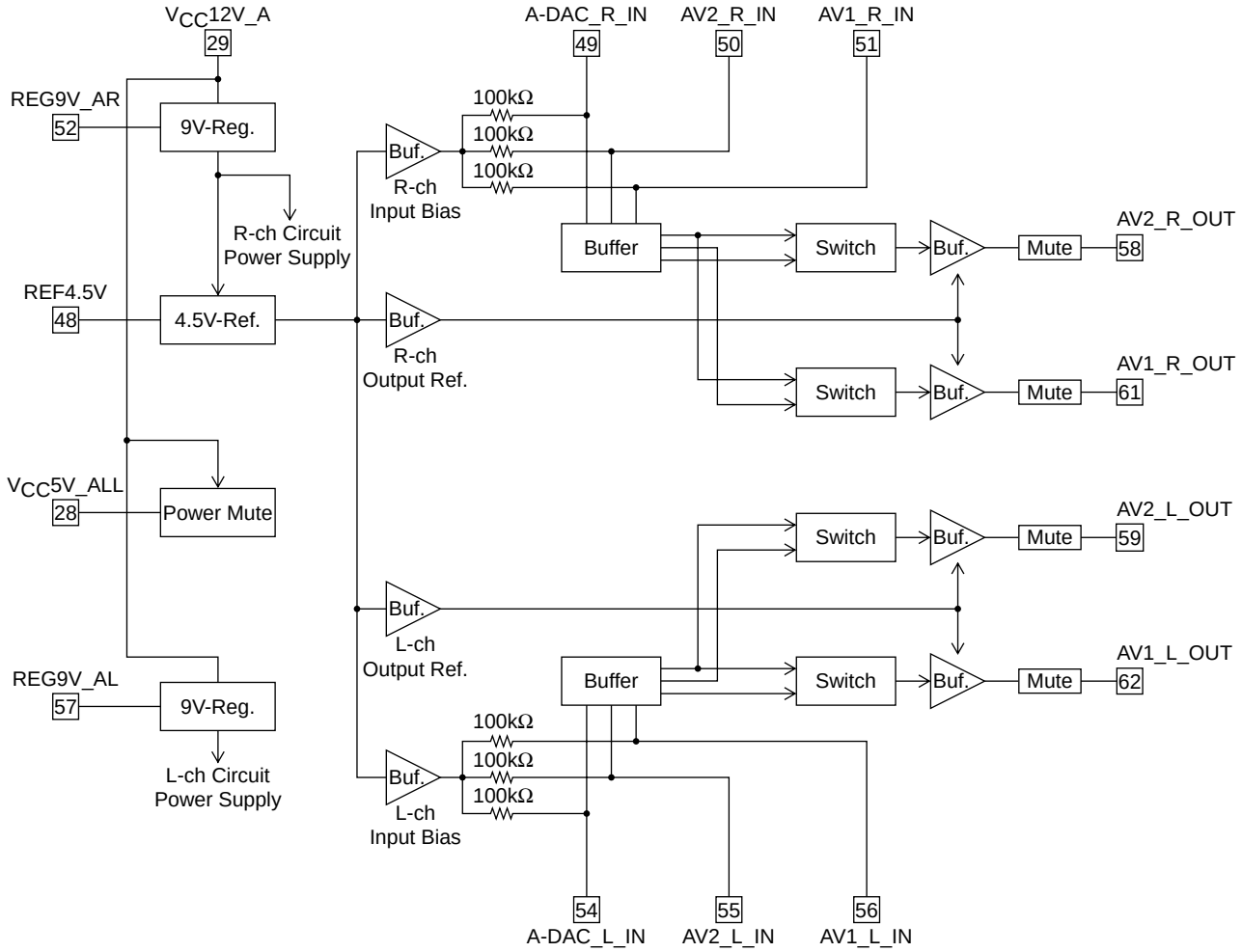
Package Dimensions

unit : mm (typ)

3159A



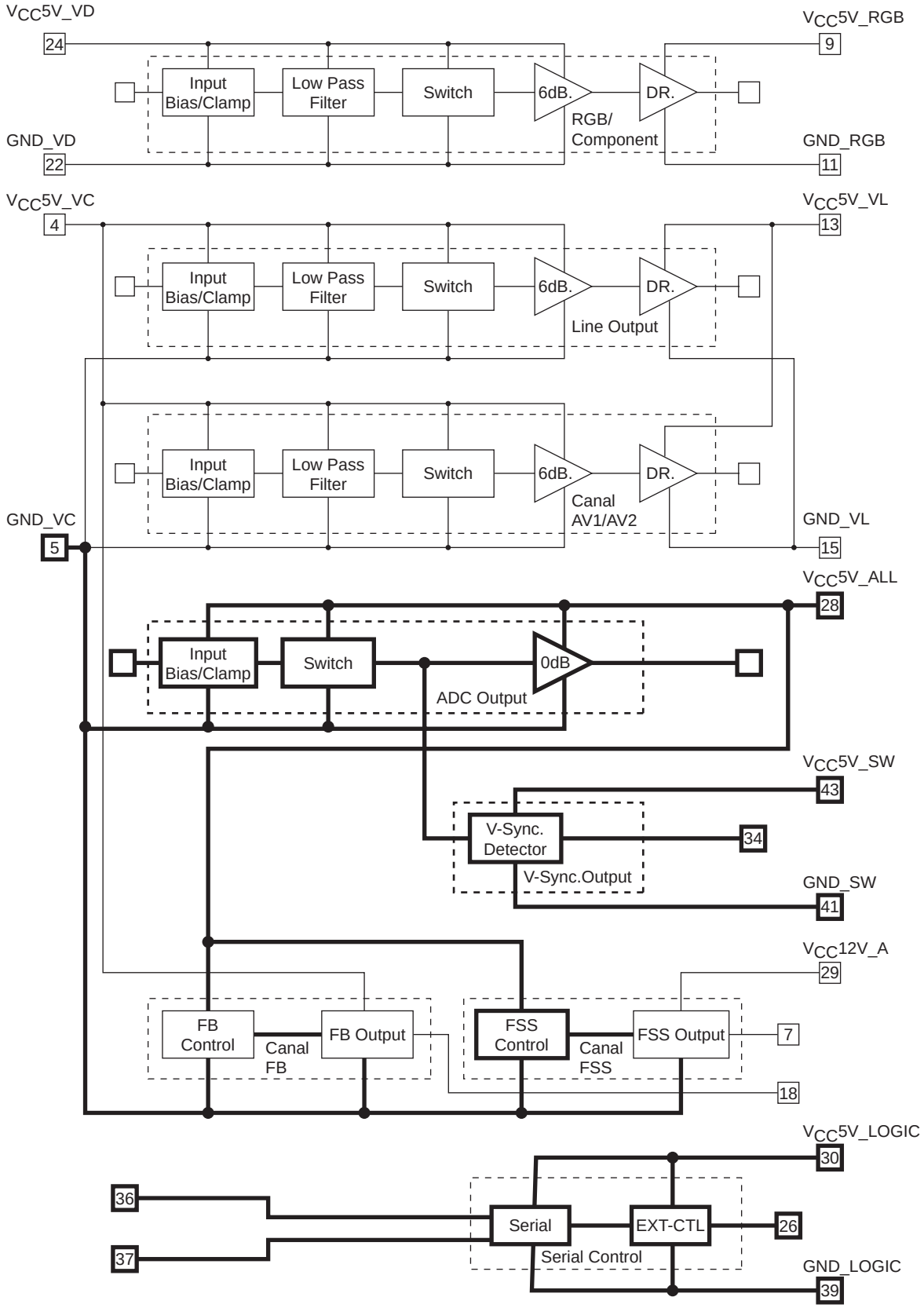
AudioPower Supply Block Diagram



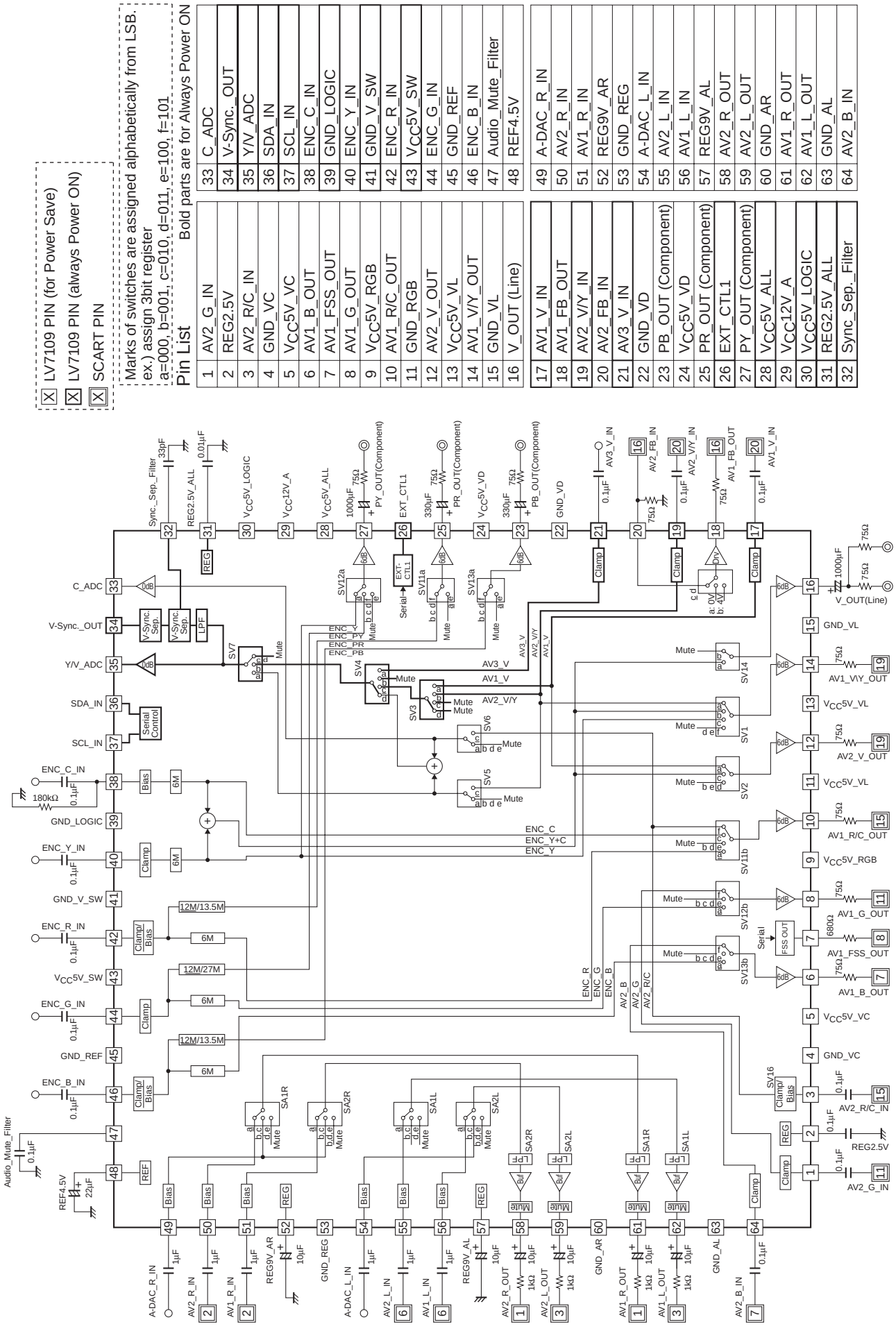
Video Power Supply Block Diagram

The thick line indicates the circuit operative in the power save mode.

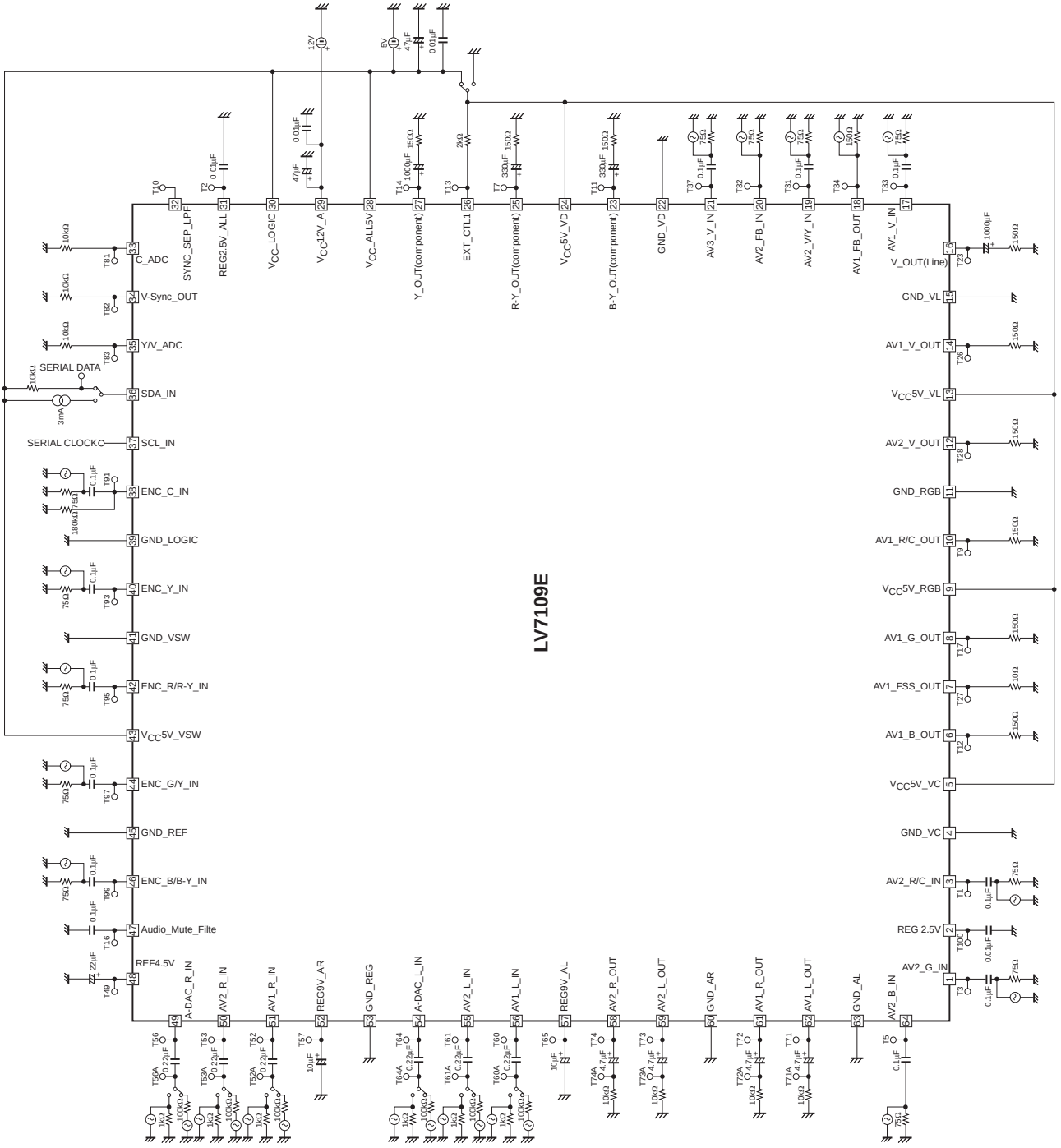
Applied power to V_{CC}5_All, V_{CC}5V_SW and V_{CC}_LOGIC only in the power save mode.



Block Diagram



Test Circuit



LV7109E Serial Control Table

* indicates initial.

ADDRESS		8	7	6	5	4	3	2	1	Symbol	Input						Output	Remarks	
Group 1 0000 0001 VIDEO CANAL-SW VIDEO	SV1						0	0	0	a	P19	AV2_V/Y_IN					P10: AV1_R/C_OUT		*
							0	0	1	b	-	ENC_Y+C_MIX							
							0	1	0	C	P40	ENC_Y							
							0	1	1	d	-	MUTE							
							1	0	0	e	-	MUTE							
							1	0	1	f	-	MUTE							
							1	1	X	-	-	PROHIBIT							
	SV2			0	0	0				a	P17	AV1_V_IN					P12: AV2_V_OUT		*
				0	0	1				b	-	MUTE							
				0	1	0				c	-	ENC_Y+C_MIX							
				0	1	1				d		MUTE							
				1	0	0				e		MUTE							
				1	0	1	and after			-		PROHIBIT							
	SV3	0	0							a	P17	AV1_V_IN					SV4		
		0	1							b	P19	AV2_V/Y_IN							*
		1	0							c	-	N/A							
		1	1							d	-	N/A							

ADDRESS		8	7	6	5	4	3	2	1	Symbol	Input						Output	Remarks	
Group 2 0000 0010 VIDEO INPUT-SW	SV4							0	0	a	P21	AV3_V_IN					SV7		
								0	1	b	-	N/A							
								1	0	C	According to SV3 control								*
								1	1	d	-	SV5/6 MIX							
	SV2				0	0	0			a	-	MUTE		MUTE			Y+C MIX SV7 P33: C_ADC		
					0	0	1			b	-	MUTE		MUTE					
					0	1	0			c	P19	AV2_V/Y_IN		AV2_R/C_IN					
					0	1	1			d	-	MUTE		MUTE					
					1	0	0			e	-	MUTE		MUTE					*
					1	0	1	and after		-	-	PROHIBIT		PROHIBIT					
	SV3		0	0						a	SV5	Y					P35: Y/V_ADC		
			0	1						b	SV4	Composit Video							
			1	0						c	-	MUTE							*
			1	1						d	-	MUTE							
	SV16 Note 1)	0								-	-	THROUGH							*
		1								-	-	CLAMP input							

ADDRESS		8	7	6	5	4	3	2	1	Symbol	Input						Output	Remarks	
Group 3 0000 0011 VIDEO OTHER-1	12/27MHz LPF SW								0	-								x = 12MHz	*
									1	-								x = 27MHz	
	RGB output							0		-	According to G3D3-5 control								
								1		-	Switch of SV11b-13b set to “f”							f: AV2_RGB (EXTERNAL)	*
	SV11a SV12a SV13a				0	0	0			a	-	MUTE	P40	ENC_Y_IN	-	MUTE	P25: PR_OUT P27: PY_OUT P23: PB_OUT	a: ENC_Y	*
					0	0	1			b	P42	ENC_R_IN	P44	ENC_G_IN	P46	ENC_B_IN		b: Component (× MLPF)	
					0	1	0			c	P42	ENC_R_IN	P44	ENC_G_IN	P46	ENC_B_IN		c: Component (× MLPF)	
					0	1	1			d	P42	ENC_R_IN	P44	ENC_G_IN	P46	ENC_B_IN		d: Component (× MLPF)	
					1	0	0			e	-	MUTE	-	MUTE	-	MUTE		e: mute	
					1	0	1			f	P42	ENC_R_IN	P44	ENC_G_IN	P46	ENC_B_IN		f: Component (× MLPF)	
					1	1	X			-	-	PROHIBIT	-	PROHIBIT	-	PROHIBIT			
	SV11b SV12b SV13b * effective at G3D2 = “0”				0	0	0			a	P42	ENC_R_IN	P44	ENC_G_IN	P46	ENC_B_IN	P10: AV1_R/C_OUT P8: AV1_G_OUT P6: AV1_B_OUT	a: ENC_RGB (6MLPF)	*
					0	0	1			b	-	MUTE	-	MUTE	-	MUTE		b: mute	
					0	1	0			c	P38	ENC_C_IN	-	MUTE	-	MUTE		c: ENC_C	
					0	1	1			d	-	MUTE	-	MUTE	-	MUTE		d: mute	
					1	0	0			e	-	MUTE	-	MUTE	-	MUTE		e: mute	
					1	0	1			f	P3	AV2_R/C_IN	P1	AV2_G_IN	P64	AV2_B_IN		f: AV2_RGB (EXTERNAL)	
					1	1	X			-	-	PROHIBIT	-	PROHIBIT	-	PROHIBIT			
	SV14			0						a	-	ENC_Y+C					P16: V_OUT (Line)		
				1						b	-	MUTE							*
	N/A		0							a	-	-	-	-					
			1							b	-	-	-	-					*
	SV16 Note 1)	0								-	-	THROUGH							
		1								-	-	BIAS input							*

Note 1) G2D8/G3D8 = “11” is prohibited. Follow the AV2 (16) FB_IN (Pin32) control in case of THROUGH.

AV2_16pin SV16

H a : Clamp input (RGB)

L b : Bias input (Y+C)

* indicates initial.

ADDRESS		8	7	6	5	4	3	2	1	Symbol	Input						Output	Remarks	
Group 4 0000 0100 VIDEO & AUDIO OTHER-1	N/A								0	a	-	N/A	-	N/A					*
									1	b	-	N/A	-	N/A					
	N/A							0		a	-	N/A	-	N/A					*
								1		b	-	N/A	-	N/A					
	FB AV1 (16) Note 2)					0	0			a	-	0V					P18: AV1_FB_OUT		
						0	1			b	-	5V							
						1	0			c	P20	THROUGH							*
						1	1			d	P20	THROUGH							
	FSS AV1 (8)			0	0					-	-	LOW (0.5V)					P7: AV1_FSS_OUT		*
				0	1					-	-	MID (6.0V)							
				1	0					-	-	HIGH (11.0V)							
				1	1					-	-	HIGH (11.0V)							
	N/A		0							-	-	-							*
			1							-	-	-							
	A-MUTE	0								-	-	THROUGH							
		1								-	-	MUTE						P58,59,61,62 output MUTE	*

Note 2) Same polarity as the AV2 (16) FB_IN (Pin20) control in case of THROUGH.

ADDRESS		8	7	6	5	4	3	2	1	Symbol	Input						Output	Remarks	
Group 5 0000 0101 AUDIO CANAL-SW	SA1L/R						0	0	0	a	P55	AV2_L_IN	P50	AV2_R_IN			P62: AV1_L_OUT P61: AV1_R_OUT		*
							0	0	1	b	P54	A-DAC_L_IN	P49	A-DAC_R_IN					
							0	1	0	c	P54	A-DAC_L_IN	P49	A-DAC_R_IN					
							0	1	1	d	-	MUTE	-	MUTE					
							1	0	0	e	-	MUTE	-	MUTE					
				and after			1	0	1	f	-	PROHIBIT	-	PROHIBIT					
	SA2L/R			0	0	0				a	P56	AV1_L_IN	P51	AV1_R_IN			P59: AV2_L_OUT P58: AV2_R_OUT		*
				0	0	1				b	-	MUTE	-	MUTE					
				0	1	0				c	P54	A-DAC_L_IN	P49	A-DAC_R_IN					
				0	1	1				d	-	MUTE	-	MUTE					
				1	0	0				e	-	MUTE	-	MUTE					
				1	0	1	and after			-	-	PROHIBIT	-	PROHIBIT					
	N/A	0	0							a	-	N/A	-	N/A					
		0	1							b	-	N/A	-	N/A					
		1	0							c	-	N/A	-	N/A					*
		1	1							d	-	N/A	-	N/A					

ADDRESS		8	7	6	5	4	3	2	1	Symbol	Input						Output	Remarks	
Group 6 0000 0110 N/A	N/A						0	0	0	a	-	N/A	-	N/A					
							0	0	1	b	-	N/A	-	N/A					*
							0	1	0	c	-	N/A	-	N/A					
							0	1	1	d	-	N/A	-	N/A					
							1	0	0	e	-	N/A	-	N/A					
				and after			1	0	1	-	-	PROHIBIT	-	PROHIBIT					
	N/A					0				a	-	N/A							
						1				b	-	N/A							*
	N/A			0	0					a	-	N/A							
				0	1					b	-	N/A							*
				1	0					c	-	N/A							
				1	1					-	-	PROHIBIT							
	N/A	0	0							a	-	N/A							
		0	1							b	-	N/A							*
		1	0							c	-	N/A							
		1	1							-	-	PROHIBIT							

ADDRESS		8	7	6	5	4	3	2	1	Symbol	Input						Output	Remarks	
Group 7 0000 0111	N/A			0	0	0	0	0	0	-	-	N/A							
				0	0	1	1	0	0	-	-	N/A							
				1	1	1	1	1	1	-	-	N/A							*
				Other than above						-	-	PROHIBIT							
	EXT-CTL1		0							-	-	L					P26: EXT_CTL1	General purpose OUT1	*
			1							-	-	H							
	Changeover of VIDEO input BIAS/CLAMP	-	-	-	-	-	-	-	-	-	P42	ENC_R_IN	P44	ENC_G_IN	P46	ENC_B_IN		Input changeover	
		0								-		BIAS input		CLAMP input		BIAS input		Component	
		1								-		CLAMP input		CLAMP input		CLAMP input		RGB	*

* indicates initial.

ADDRESS		8	7	6	5	4	3	2	1	Symbol	Input							Output	Remarks	
Group 8 0000 1000 N/A	N/A			0	0	0	0	0	0	-	-	N/A								
				0	0	1	1	0	0	-	-	N/A								
				1	1	1	1	1	1	-	-	N/A								*
				Other than above						-	-	PROHIBIT								
	N/A		0							-	-	N/A								*
			1							-	-	N/A								
	N/A	0								-	-	N/A								*
		1								-	-	N/A								

Cautions for Use

1. Drive capacity of video driver
   Line outputs can drive two systems through capacitive coupling.
   Component outputs can drive one systems through capacitive coupling.
   Scart output can drive one system only through DC coupling.

2. Audio Mute
   This IC incorporates a mute transistor to reduce the POP noise of audio output when power is turned ON/OFF.
   Mute control can be made by serial control.

3. Resistor to limit the Audio input
   When the large signal is input in the input pin with power OFF, cross-talke between input and output occurs through the protective diode and parasitic elements. Because of the structure of LSI, such cross-talke is difficult to avoid.
   If cross-talk at a time of power OFF presents a problem, the cross-talk amount can be reduced by inserting the limiting resistor in the input.
   In this case, the input signal level changes depending on the resistance value. Determine the constant while taking both the cross-talk amount and input level into account.

4. Pin treatment when external control is not to be used
   When external control pins (Pins 26) are not used, pull-down to GND is recommended.

5. Audio 9V_REG pin external capacitance
   Use the Audio 9V_REG pins (pins 52 and 57) external capacitance of 10μF or more and with the equivalent series resistance component of 7Ω or less.

6. Power application and disconnection sequences
   The recommended power application sequence to this IC is V_{CC}_ALL5V (Pin28) → V_{CC}5V (Pins 5, 9, 13, 24, 30 and 43), V_{CC}12V (Pin29).
   (No particular order is established between V_{CC}5V and V_{CC}12V.) It is recommended to reverse the above sequence when power supply is turned OFF.

Serial Control Specification

1. Slave address

MSB							LSB
1	0	0	1	0	1	0	0

↑ Slave receiver
One-way communication (this IC is dedicated to receive)

2. DATA TRANSFER MANUAL : [1] is High level. [0] is Low level.
I^{2}C-BUS control system is adopted in SW LSI. SW LSI is controlled by SCL (Serial Clock) and SDA (Serial Data) At first, please set up the START condition[*1] by these two terminals (SCL and SDA). And next, please input the 8bits data, which should be synchronized with SCL into SDA terminal. Still more, please give priority to high rank bit at data transfer order (MSB→LSB). The 9th bit is called as ACK (Acknowledge), SW LSI sends [0] to the SDA terminal during SCL [1] period. So, please open the port of microprocessor during this period. LV7107M adopt auto-increment, so you input only first group-address and you can transfer data in order. As thus the Data transfer Stop condition[*2] is finished.
[*1] SDA rise up during SCI is [1]
[*2] SDA fall down during SCL is [1]

3. TRANSFER DATA FORMAT
The transfer data is composed by START condition, Slave address, Group address[*4], data, and STOP condition.
After setting up the START condition, please transfer the Slave Address (regulated as “1001000” in SW LSI). Group and next control data (Please see the Fig.1)
Slave Address is composed by 7bits, and this bit 8th bit[*5] should be set as [0].

The both of Group address and control data are composed by 8bits, and the one control action is defined with combination of these two data. And if you want to control 2 or more groups at the same mode, you can realize it by sending some control data together.
The data makes meaning with all bits, so you cannot stop the sending until all data transfer is over.
But LV7107M adopt auto-increment, for example you can stop to transfer STOP condition after group 2 data.
If you want to stop transfer action, please transfer the STOP condition without fail.
[*4] There are 8 control groups.
[*5] This 8th bit called as R/W bit, and this bit shows the data transmission direction. [0] means send mode (accept mode with SW LSI) and [1] means accept mode (send mode with SW LSI) fundamentally. But SW LSI is not equipped with such a data out function, please keep this bit as [0].

Fig. 1 DATA STRUCTURE

START condition	Slave address	R/W	ACK	Group address	ACK	Control data	ACK	.....	STOP condition

↑ Start condition
↑ Acknowledge
↑ Stop condition

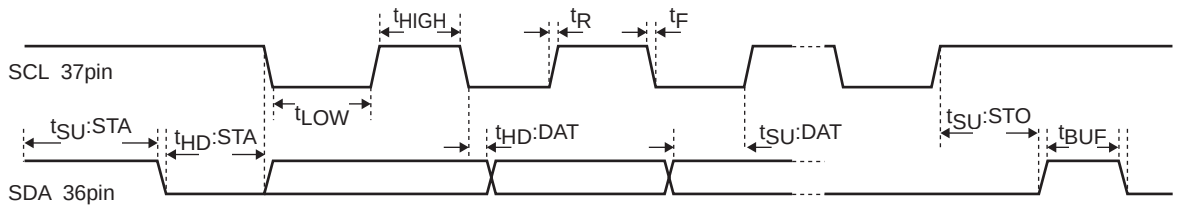
4. INITIALIZE AND OTHERS

SW LSI is initialized as the following mode for circuit protection. Please see “SERIAL CONTROL TABLE”.

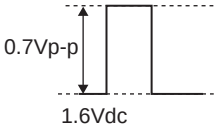
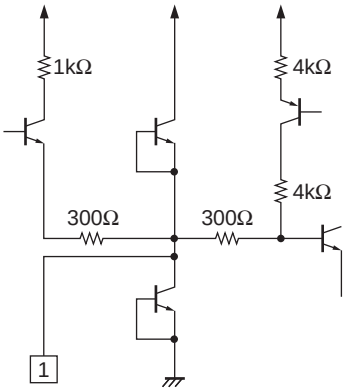
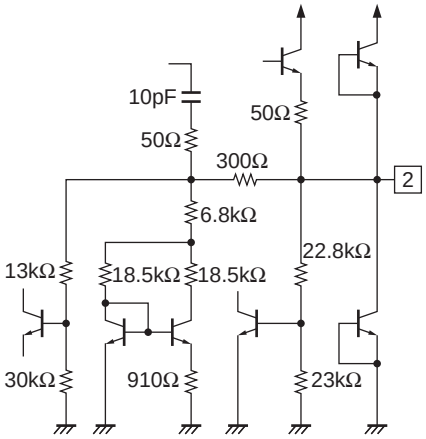
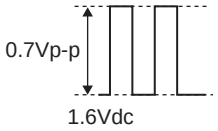
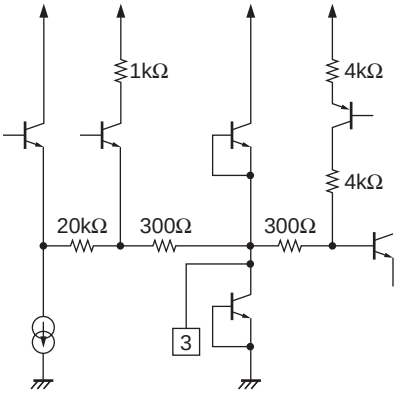
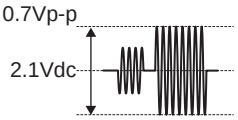
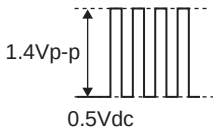
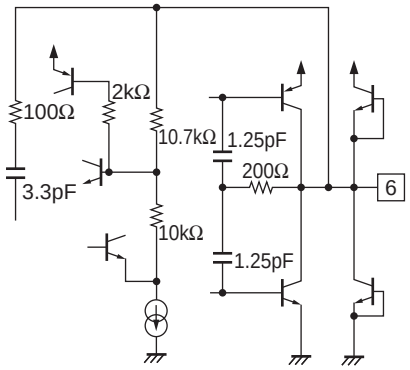
Characteristics of the SDA and SCL 1/0 stages for SW LSI

Parameter	Symbol	Min	Max	Unit
LOW level input voltage	V_{IL}	0	0.8	V
HIGH level input voltage	V_{IH}	3.0	5.0	V
LOW level output current	I_{OL}		3.0	mA
SCL clock frequency	f_{SCL}		400	kHz
Set-up time for a repeated START condition	t_{SU} : STA	0.6		μs
Hold time START condition. After this period, the first clock pulse is generated.	t_{HD} : STA	0.6		μs
LOW period of the SCL clock	t_{LOW}	1.3		μs
Rise time of both SDA and SDL signals	t_R	0	0.3	μs
HIGH period of the SCL clock	t_{HIGH}	0.6		μs
Fall time of both SDA and SDL signals	t_F	0	0.3	μs
Data hold time:	t_{HD} : DAT	0	0.9	μs
Data set-up time	t_{SU} : DAT	100		ns
Set-up time for STOP condition	t_{SU} : STO	0.6		μs
BUS fredd time between a STOP and START condition	t_{BUF}	1.3		μs

Fig.2 Definition of timing.



Pin Function

Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P1	AV2_G_IN	1.6Vdc +Green			
P2	REG2.5V	2.5Vdc	DC		
P3	AV2_R/C_IN	1.6Vdc +Red			
		2.1Vdc +Chroma			
P4	GND_VC				
P5	V_{CC}5V_VC				
P6	AV1_B_OUT	0.5V +Blue			

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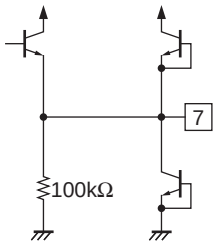
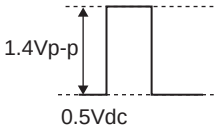
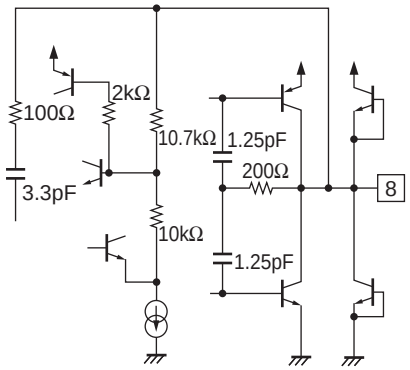
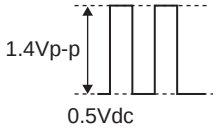
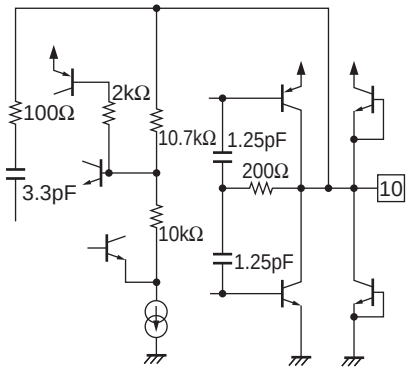
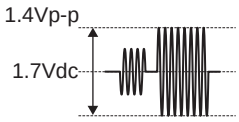
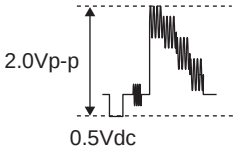
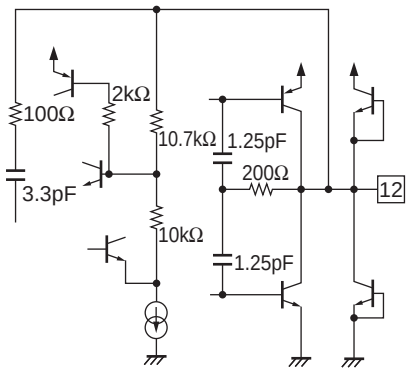
Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P7	AV1_FSS_OUT	Low : 0.5V Mid : 6.0V High : 11.1V	DC		
P8	AV1_G_OUT	0.5Vdc +Green			
P9	V_{CC}_RGB				
P10	AV1_R/C_OUT	0.5Vdc +Red			
		1.7Vdc +Chroma			
P11	GND_RGB				
P12	AV2_V_OUT	0.5Vdc +Video			
P13	V_{CC}5V_VL				

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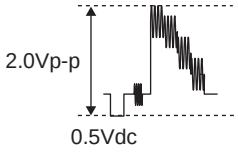
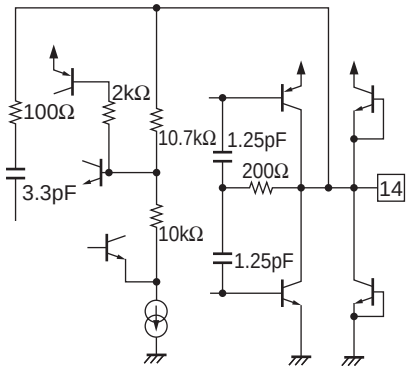
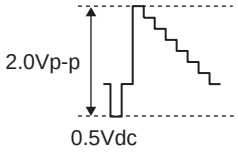
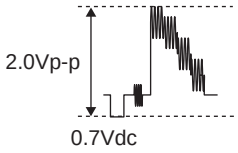
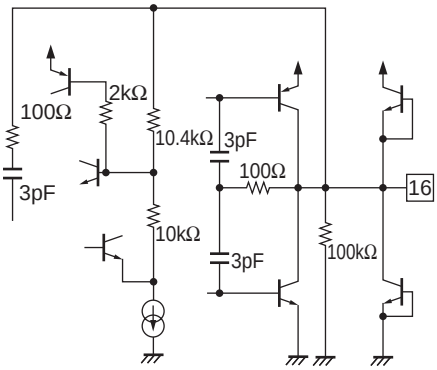
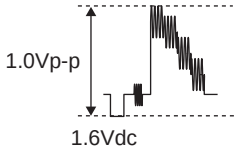
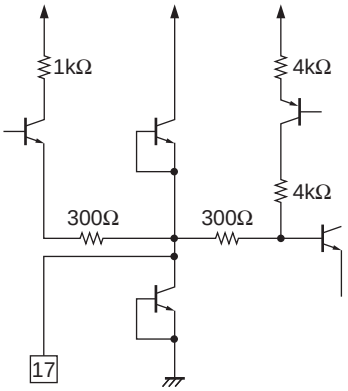
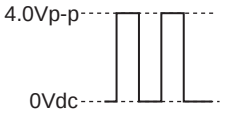
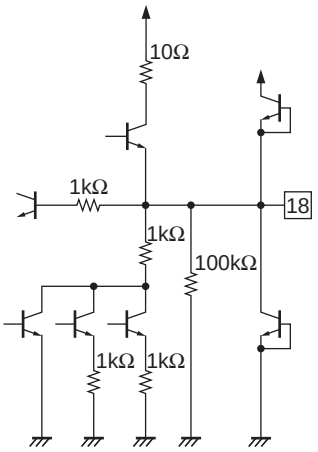
Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P14	AV1_V/Y_OUT	0.5Vdc +Video			
		0.5Vdc +Y			
P15	GND_VL				
P16	V_OUT (Line_OUT)	0.7Vdc +CVBS			
P17	AV1_V_IN	1.6Vdc +CVBS			
P18	AV1_FB_OUT	Low : 0V High : 4.0V Through : 0/4.0V			

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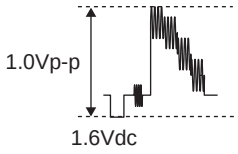
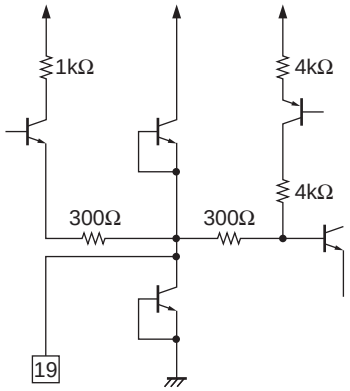
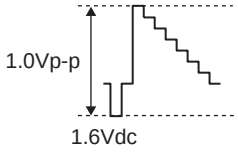
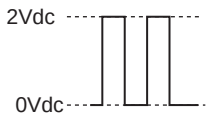
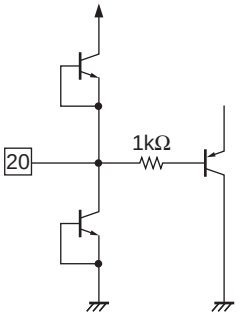
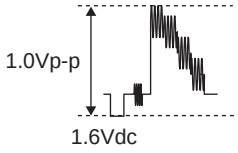
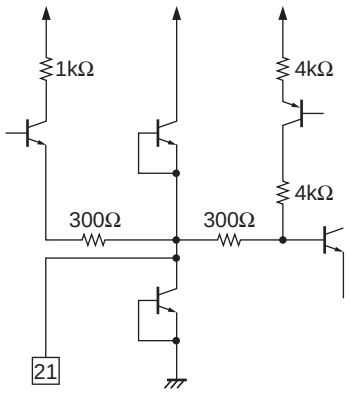
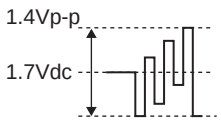
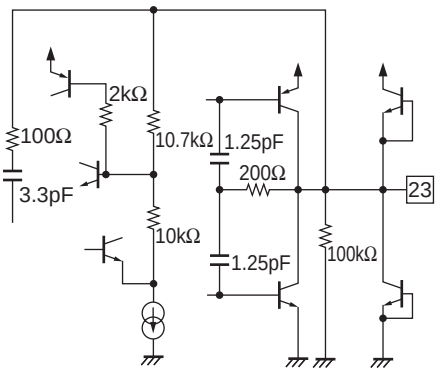
Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P19	AV2_V/Y_IN	1.6Vdc +CVBS			
		1.6Vdc +Y			
P20	AV1_FB_IN	Low : 0V High : 2V			
P21	AV3_V_IN	1.6Vdc +CVBS			
P22	GND_VD				
P23	PB_OUT (Component)	1.7V +Pb			
P24	V_{CC}5V_VD				

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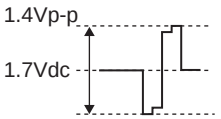
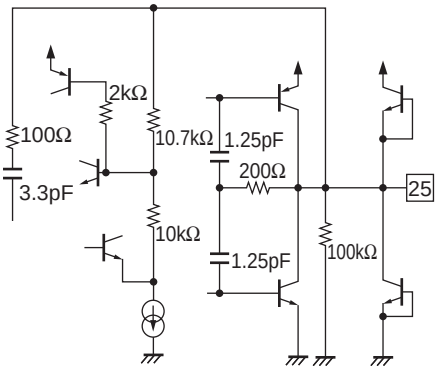
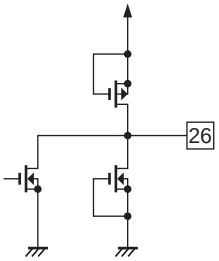
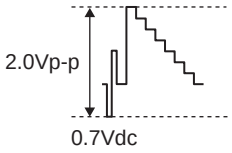
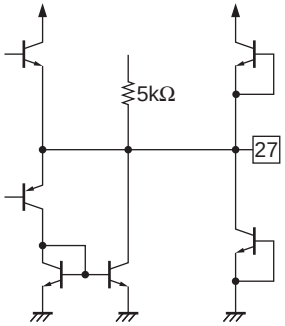
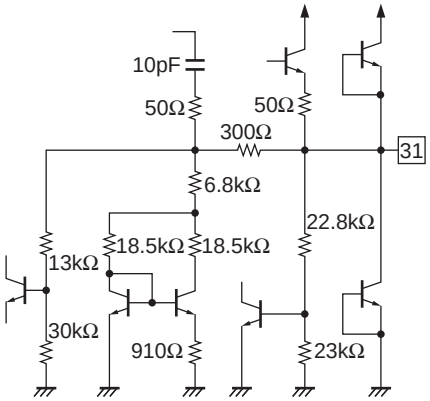
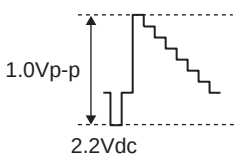
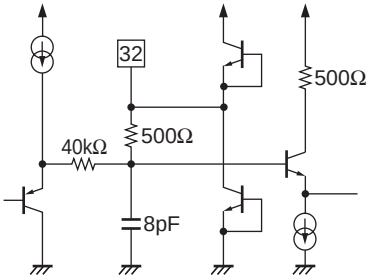
Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P25	PR_OUT (Component)	1.7V +Pr			
P26	EXT-CTL1 (OUT)	Low : 0V High : 5V			
P27	PY_OUT (Component)	0.7Vdc +Py			
P28	V_{CC}5V_ALL				
P29	V_{CC}12V_A				
P30	V_{CC}5V_LOGIC				
P31	REG2.5V_ALL	2.5Vdc	DC		
P32	SYNC_SEP _FILTER	2.2Vdc +Y			

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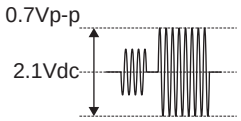
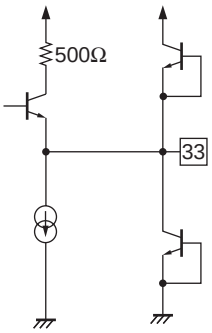
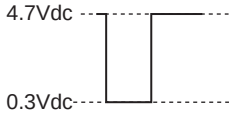
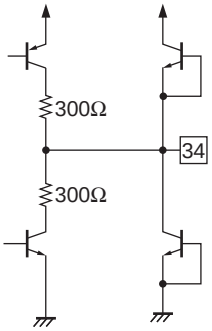
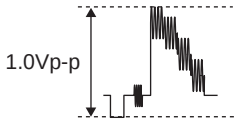
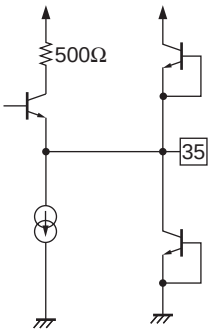
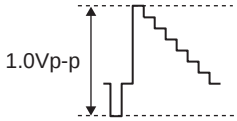
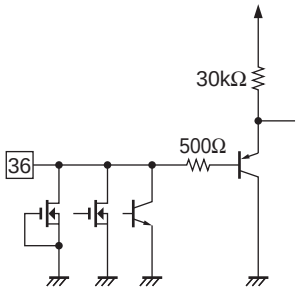
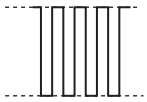
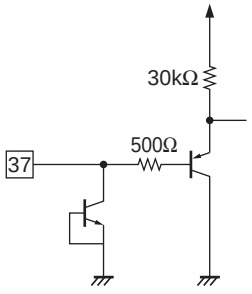
Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P33	ADC_C_OUT	2.1Vdc +Chroma			
P34	V_SYNC_OUT	Low : 0.3V High : 4.7V			
P35	ADC_V/Y_OUT	1.0Vdc +CVBS			
		1.0Vdc +Y			
P36	SDA_IN	I^2C DATA			ACK_OUT
P37	SCL_IN	I^2C CLOCK			

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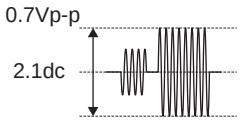
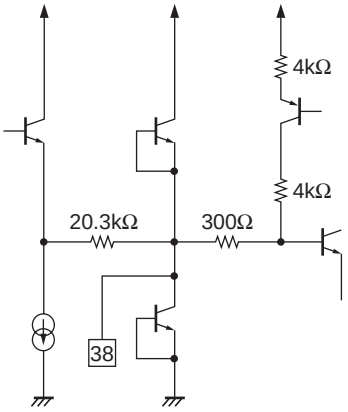
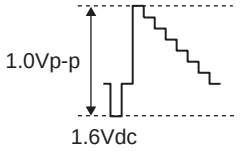
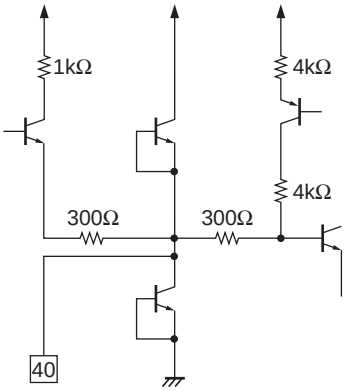
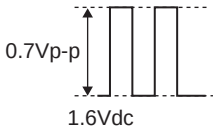
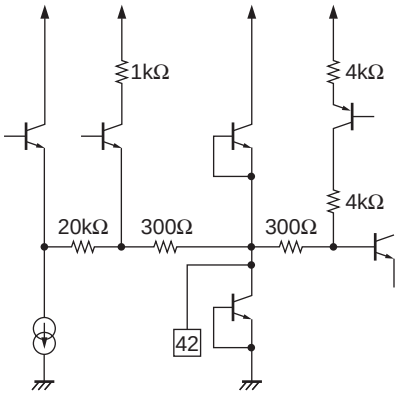
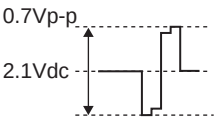
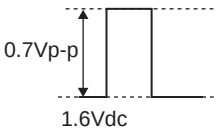
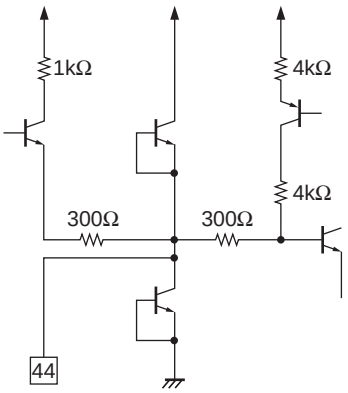
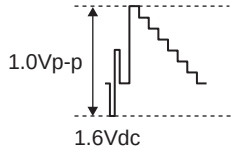
Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P38	ENC_C_IN	2.1Vdc +Chroma			
P39	GNG_LOGIC				
P40	ENC_Y_IN	1.6Vdc +Y			
P41	GND_VSW				
P42	ENC_R/PR_IN	1.6Vdc +Red			
		2.1Vdc +Pr			
P43	V_{CC}5V_SW				
P44	ENC_G/PY_IN	1.6Vdc +Green			
		1.6Vdc +Py			
P45	GNG_REF				

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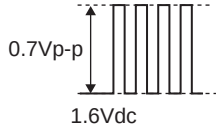
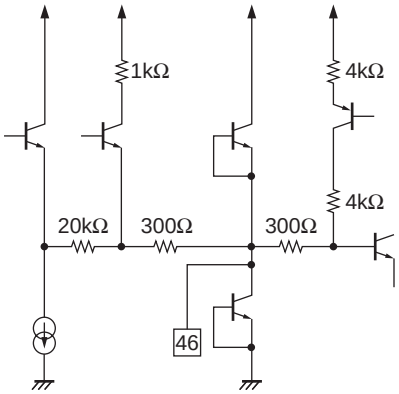
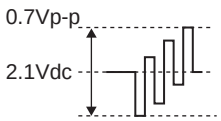
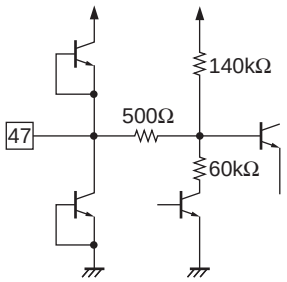
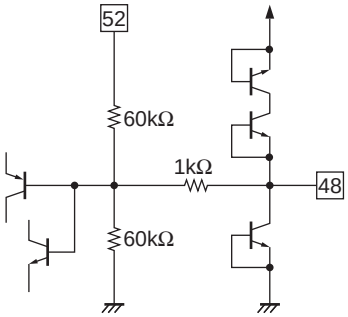
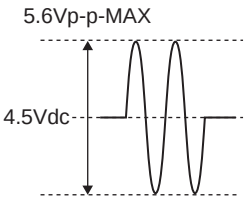
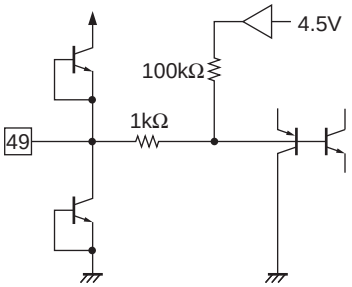
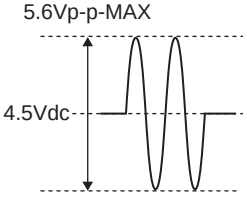
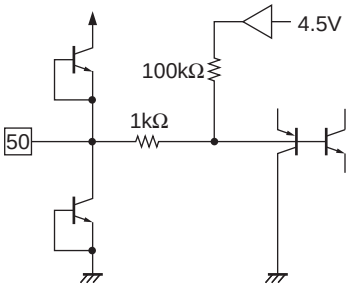
Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P46	ENC_B/PB_IN	1.6Vdc +Blue			
		2.1Vdc +Pb			
P47	Audio_Mute_Filter				
P48	REF4.5V	4.5Vdc	DC		
P49	A-DAC_R_IN	4.5Vdc +Right			
P50	AV2_R_IN	4.5Vdc +Right			

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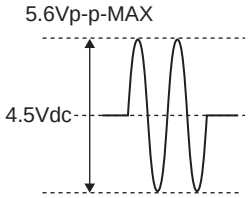
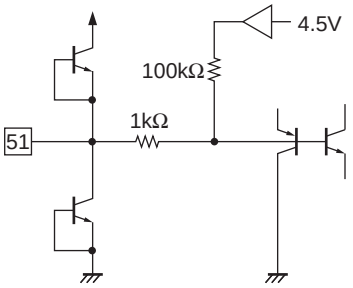
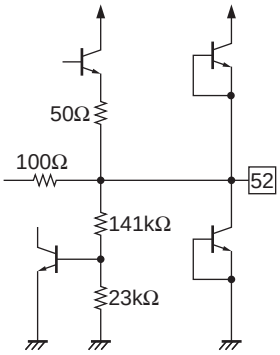
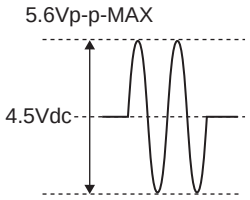
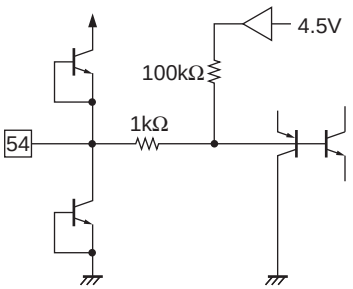
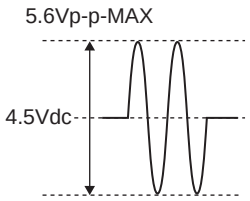
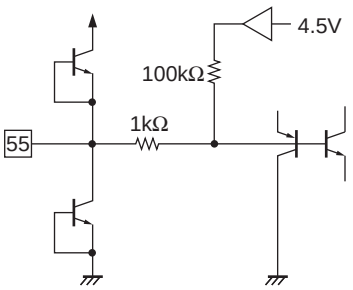
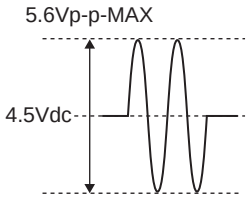
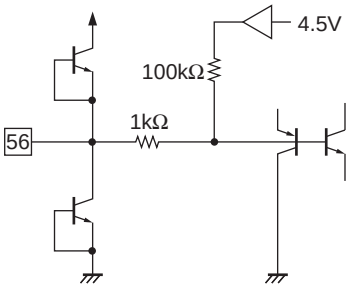
Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P51	AV1_R_IN	4.5Vdc +Right			
P52	REG9V_AR	9Vdc	DC		
P53	GND_REG				
P54	A-DAC_L_IN	4.5Vdc +Left			
P55	AV2_L_IN	4.5Vdc +Left			
P56	AV1_L_IN	4.5Vdc +Left			

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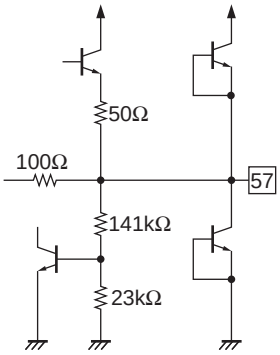
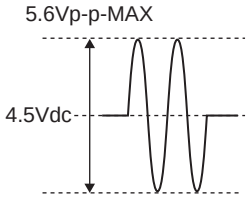
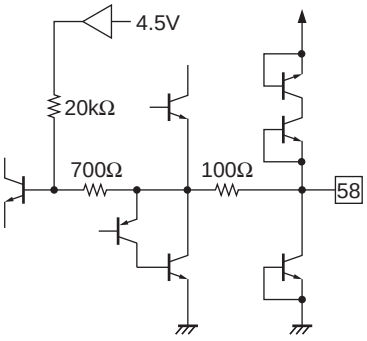
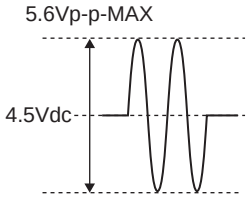
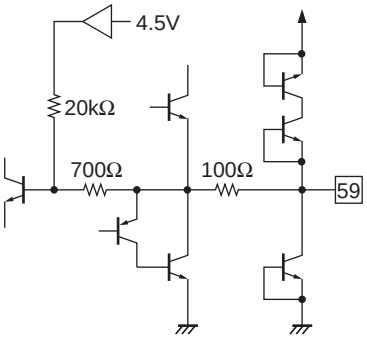
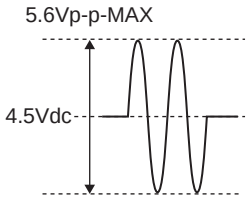
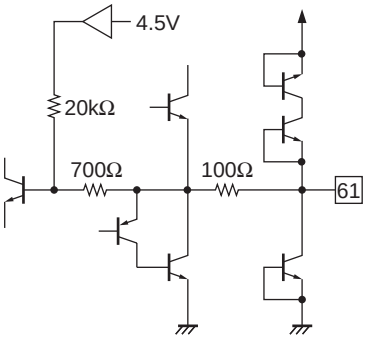
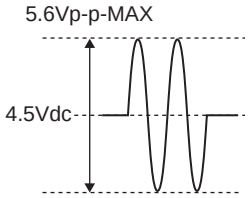
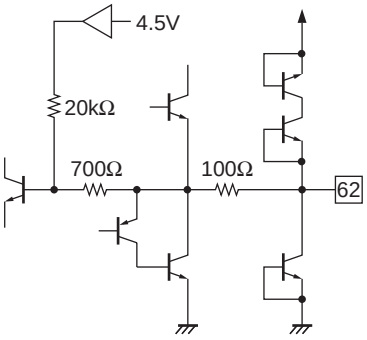
Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P57	REG9V_AL	9Vdc	DC		
P58	AV2_R_OUT	4.5Vdc +Right			
P59	AV2_L_OUT	4.5Vdc +Left			
P60	GND_AR				
P61	AV1_R_OUT	4.5Vdc +Right			
P62	AV1_L_OUT	4.5Vdc +Left			
P63	GND_AL				

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Pin No.	Pin name	DC voltage	Signal wave form	Input/Output form	Note
P64	AV2_B_IN	1.6Vdc +Blue