Ordering number : ENA0167B

SANYO Semiconductors
DATA SHEET

LV8054LP — Bi-CMOS IC For Digital Cameras Single-chip motor Driver IC

Overview

LV8054LP is single-chip motor driver IC for digital cameras.

Functions

- Integrates the digital camera actuator drivers on a single chip
- Four constant voltage output channels, two constant current output channels
- All actuators can be driven at the same time
- The AF and zoom stepping motors are driven by the clock signal
- Supports PWM control of a DC zoom motor.
- Can switch between an external input or an internal reference for the constant voltage output setting reference voltage
- The constant voltage output multiplier can be set to one of 16 levels
- The constant current output reference voltage can be set to one of 16 internal reference voltage levels
- Built-in photosensor drive transistor
- Three built-in Schmitt buffer circuits (the presence or absence of hysteresis can be set individually)

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_B max		6.0	V
Supply voltage 2	V_{CC} max		6.0	V
Peak output current	I_O peak	OUT1 to 12 (t≤10mS, ON-duty≤20%)	600	mA
Continuous output current	I_O max1	OUT1 to 12	400	mA
	I_O max2	PI	85	mA
Allowable power dissipation	Pd max	Mounted on a circuit board*	1100	mW
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Standard circuit board: 40×50× 0.8 mm^3 glass epoxy four-layer board

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	V_B		2.7 to 5.5	V
Supply voltage range 2	V_{CC}		2.7 to 5.5	V
Logic level input voltage	V_{IN}		0 to V_{CC}+0.3	V
Constant voltage setting input range	V_C		0.1 to V_{CC}	V
Clock frequency	F_{CLK}	CLK1, CLK2/PWM	-64	KHz
PWM frequency	F_{PWM}	CLK2/PWM	-100	KHz

Electrical Characteristics at Ta = 25°C, V_B = 5V, V_{CC} = 3.3V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	ST = low, BI1/2/3 = low			1	μA
Current drain 1	I_B	ST = high, IN51/52/61/62 = low, BI1/2/3 = low, With no output load		500	950	μA
Current drain 2	I_{CC}	ST = high, IN51/52/61/62 = low, BI1/2/3 = low, With no output load		1.5	2.0	mA
VCC low-voltage cutoff voltage	$V_{th}V_{CC}$		2.1	2.35	2.6	V
Low-voltage hysteresis	$V_{th}HYS$		100	150	200	mV
Thermal shutdown temperature	TSD	Design target value	160	180	200	°C
Thermal shutdown hysteresis	ΔTSD	Design target value	20	40	60	°C
AF/Zoom Motor Drivers (OUT1/2, OUT3/4, OUT5/6, OUT7/8)						
Output on-resistance 1	Ronu1	Ta = 25°C, I_O = 200mA, High side on-resistance		0.7	0.85	Ω
	Rond1	Ta = 25°C, I_O = 200mA, Low side on-resistance		0.5	0.65	Ω
Output leakage current 1	$I_O$leak1				1	μA
Diode forward voltage 1	V_D1	I_D = -400mA	0.7	0.9	1.2	V
Internal reference voltage	V_{REF}		0.84	0.88	0.92	V
Constant voltage output	$V_{OUT}1$	V_C = 0.88V	4.2	4.4	4.6	V
	$V_{OUT}2$	V_C = 0.88V (internal reference)	4.2	4.4	4.6	V
VC voltage divider voltage ratio	$V_{CR}1$	(D3, D4, D5, D6) = (0, 0, 0, 0)	95	100	105	%
	$V_{CR}2$	(D3, D4, D5, D6) = (1, 0, 0, 0)	92.8	97.7	102.6	%
	$V_{CR}3$	(D3, D4, D5, D6) = (0, 1, 0, 0)	90.7	95.5	100.2	%
	$V_{CR}4$	(D3, D4, D5, D6) = (1, 1, 0, 0)	88.5	93.2	97.8	%
	$V_{CR}5$	(D3, D4, D5, D6) = (0, 0, 1, 0)	86.4	90.9	95.5	%
	$V_{CR}6$	(D3, D4, D5, D6) = (1, 0, 1, 0)	84.2	88.6	93.1	%
	$V_{CR}7$	(D3, D4, D5, D6) = (0, 1, 1, 0)	82.0	86.4	90.7	%
	$V_{CR}8$	(D3, D4, D5, D6) = (1, 1, 1, 0)	79.9	84.1	88.3	%
	$V_{CR}9$	(D3, D4, D5, D6) = (0, 0, 0, 1)	77.7	81.8	85.9	%
	$V_{CR}10$	(D3, D4, D5, D6) = (1, 0, 0, 1)	75.6	79.5	83.5	%
	$V_{CR}11$	(D3, D4, D5, D6) = (0, 1, 0, 1)	73.4	77.3	81.1	%
	$V_{CR}12$	(D3, D4, D5, D6) = (1, 1, 0, 1)	71.2	75.0	78.7	%
	$V_{CR}13$	(D3, D4, D5, D6) = (0, 0, 1, 1)	69.1	72.7	76.4	%
	$V_{CR}14$	(D3, D4, D5, D6) = (1, 0, 1, 1)	66.9	70.5	74.0	%
	$V_{CR}15$	(D3, D4, D5, D6) = (0, 1, 1, 1)	64.8	68.2	71.6	%
	$V_{CR}16$	(D3, D4, D5, D6) = (1, 1, 1, 1)	62.6	65.9	69.2	%

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Logic pin input current	$I_{IN}L$	V_{IN} = 0V (ST, CLK1, CLK2/PWM)			1.0	μA
	$I_{IN}H$	V_{IN} = 3.3V (ST, CLK1, CLK2/PWM)		33	50	μA
High-level input voltage	$V_{IN}H$	ST, CLK1, CLK2/PWM	2.5			V
Low-level input voltage	$V_{IN}L$	ST, CLK1, CLK2/PWM			1.0	V
Shutter/AE Motor Drivers (OUT9-10, OUT11-12)						
Output on-resistance 2	Ronu2	Ta = 25°C, I_O = 200mA, High side on-resistance		0.7	0.85	Ω
	Rond2	Ta = 25°C, I_O = 200mA, Low side on-resistance		0.5	0.65	Ω
Output leakage current 2	$I_O$leak2				1	μA
Diode forward voltage 2	VD2	I_D = -400mA	0.7	0.9	1.2	V
Constant current output	I_O	R_f = 1Ω, (D3, D4, D5, D6) = (0, 0, 0, 0)	190	200	210	mA
Internal current setting reference voltages	$V_{REF}1$	(D3, D4, D5, D6) = (0, 0, 0, 0)	0.190	0.200	0.210	V
	$V_{REF}2$	(D3, D4, D5, D6) = (1, 0, 0, 0)	0.162	0.170	0.179	V
	$V_{REF}3$	(D3, D4, D5, D6) = (0, 1, 0, 0)	0.157	0.165	0.173	V
	$V_{REF}4$	(D3, D4, D5, D6) = (1, 1, 0, 0)	0.152	0.160	0.168	V
	$V_{REF}5$	(D3, D4, D5, D6) = (0, 0, 1, 0)	0.147	0.155	0.163	V
	$V_{REF}6$	(D3, D4, D5, D6) = (1, 0, 1, 0)	0.143	0.150	0.158	V
	$V_{REF}7$	(D3, D4, D5, D6) = (0, 1, 1, 0)	0.138	0.145	0.152	V
	$V_{REF}8$	(D3, D4, D5, D6) = (1, 1, 1, 0)	0.133	0.140	0.147	V
	$V_{REF}9$	(D3, D4, D5, D6) = (0, 0, 0, 1)	0.128	0.135	0.142	V
	$V_{REF}10$	(D3, D4, D5, D6) = (0, 0, 0, 1)	0.124	0.130	0.137	V
	$V_{REF}11$	(D3, D4, D5, D6) = (0, 1, 0, 1)	0.119	0.125	0.131	V
	$V_{REF}12$	(D3, D4, D5, D6) = (1, 1, 0, 1)	0.114	0.120	0.126	V
	$V_{REF}13$	(D3, D4, D5, D6) = (0, 0, 1, 1)	0.109	0.115	0.121	V
	$V_{REF}14$	(D3, D4, D5, D6) = (1, 0, 1, 1)	0.105	0.110	0.116	V
	$V_{REF}15$	(D3, D4, D5, D6) = (0, 1, 1, 1)	0.100	0.105	0.110	V
	$V_{REF}16$	(D3, D4, D5, D6) = (1, 1, 1, 1)	0.095	0.100	0.105	V
Logic pin input current	$I_{IN}L$	V_{IN} = 0V (IN51, IN52, IN61, IN62)			1.0	μA
	$I_{IN}H$	V_{IN} = 3.3V (IN51, IN52, IN61, IN62)		33	50	μA
High-level input voltage	$V_{IN}H$	IN51, IN52, IN61, IN62	2.5			V
Low-level input voltage	$V_{IN}L$	IN51, IN52, IN61, IN62			1.0	V
Photosensor peripheral circuits (PI, BI1, BO1, BI2, BO2, BI3, BO3)						
Output on-resistance 3	Ron3	Ta=25°C, I_O= 60mA		2	2.5	Ω
Output leakage current 3	$I_O$leak3				1	μA
Schmitt buffer threshold level (hysteresis)	$V_{th}H$		1.50	1.70	1.90	V
	$V_{th}L$		0.85	1.05	1.25	V
Schmitt buffer hysteresis	V_{th}hys		0.5	0.7	0.9	V
Schmitt buffer threshold level (no hysteresis)	V_{th}		1.4	1.6	1.8	V

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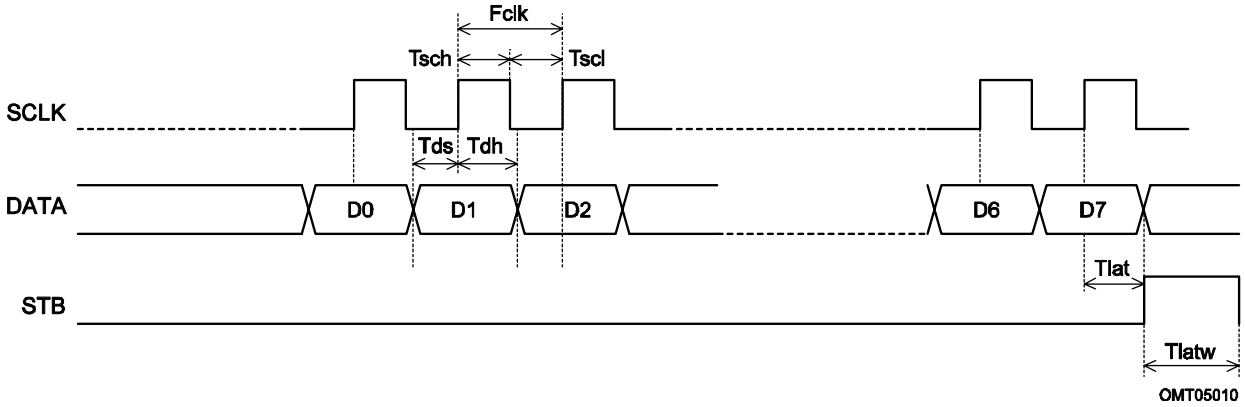
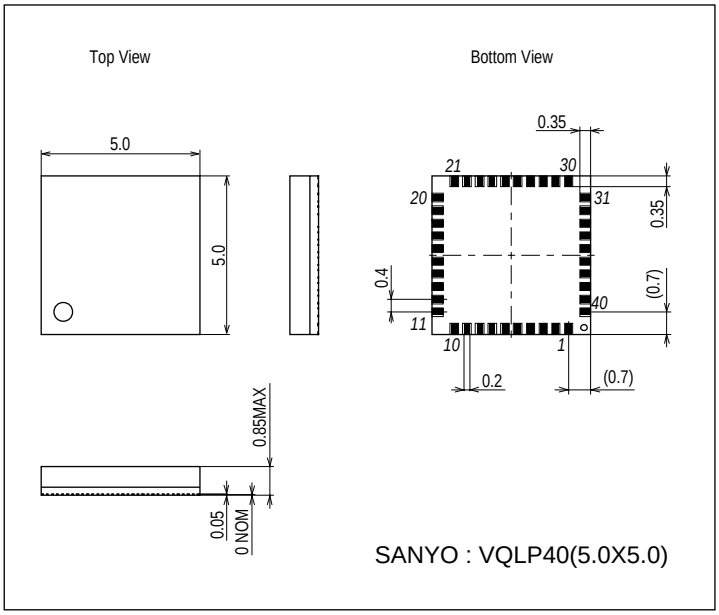
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Serial Data Transfer Pins						
Logic pin input current	$I_{IN}L$	V_{IN} = 0V (SCLK, DATA, STB)			1.0	μA
	$I_{IN}H$	V_{IN} = 3.3V (SCLK, DATA, STB)		33	50	μA
High-level input voltage	$V_{IN}H$	SCLK, DATA, STB	2.5			V
Low-level input voltage	$V_{IN}L$	SCLK, DATA, STB			1.0	V
Minimum SCLK high-level pulse width	Tsch		0.125			μS
Minimum SCLK low-level pulse width	Tscl		0.125			μS
Stipulated STB time	Tlat		0.125			μS
Minimum STB pulse width	Tlatw		0.125			μS
Data setup time	Tds		0.125			μS
Data hold time	Tdh		0.125			μS
Maximum CLK frequency	Fclk				4	MHz



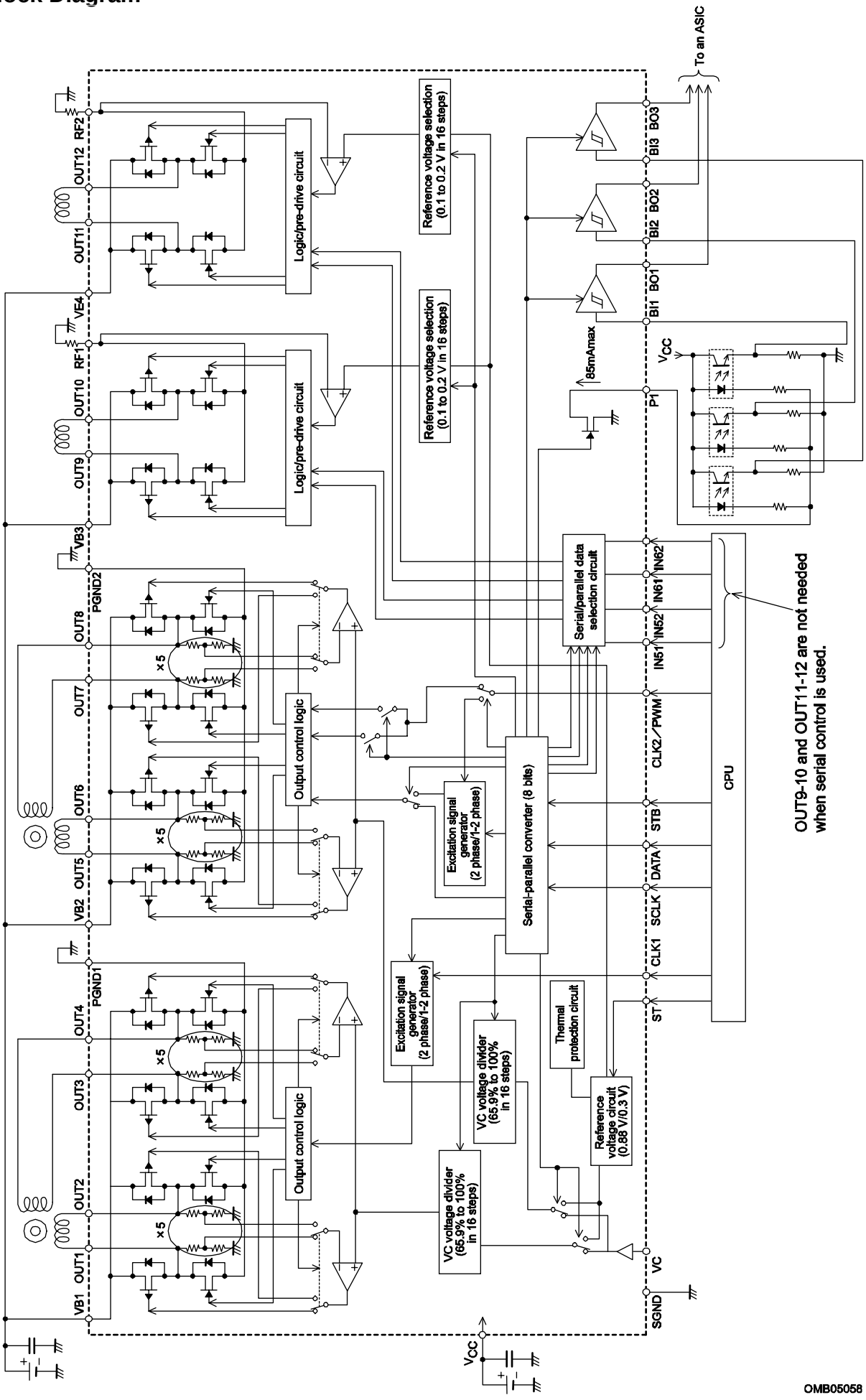
Package Dimensions

unit : mm (typ)

3302A



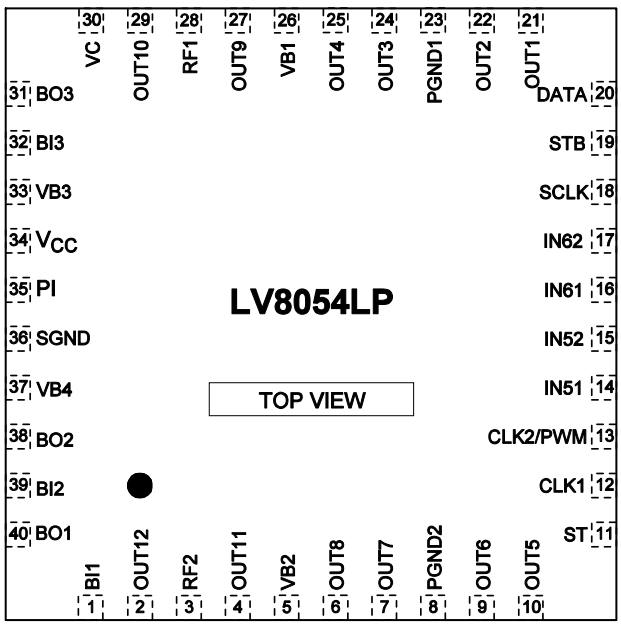
Block Diagram



Pin Functions

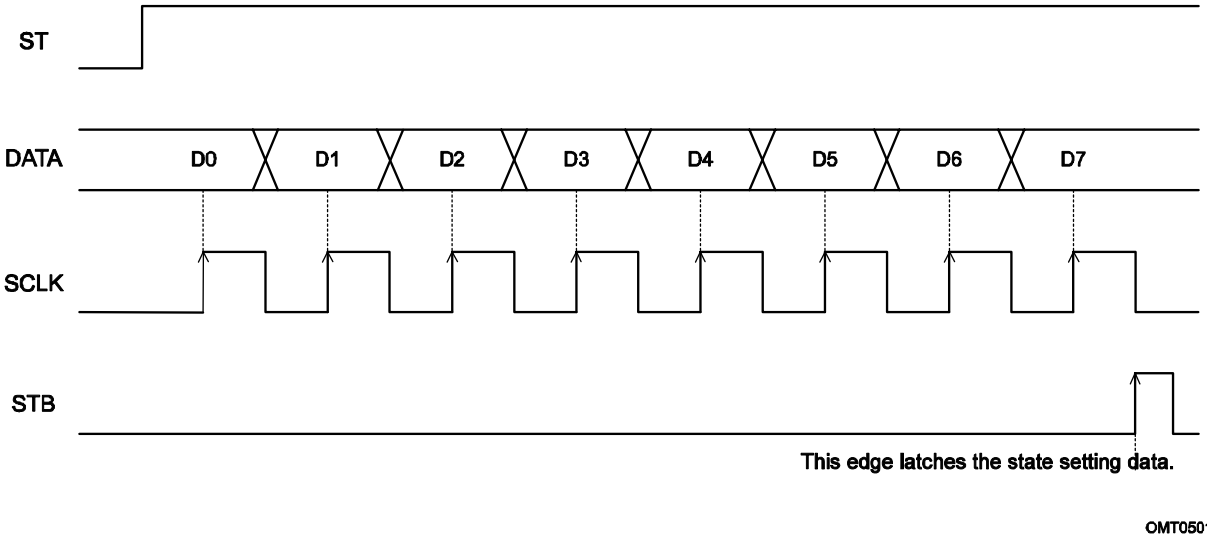
Pin No.	Symbol	Description	Pin No.	Symbol	Description
26	VB1	Power supply for OUT1-4	4	OUT11	Motor driver output
5	VB2	Power supply for OUT5-8	2	OUT12	Motor driver output
33	VB3	Power supply for OUT9-10	30	VC	External reference voltage input for the OUT1-8 constant current output
37	VB4	Power supply for OUT11-12	11	ST	Chip enable
34	VCC	Control system power supply	12	CLK1	Stepping motor clock for OUT1-4
23	PGND1	Power system ground for OUT1-4	18	SCLK	Serial data transfer clock
8	PGND2	Power system ground for OUT5-8	20	DATA	Serial data
28	RF1	Current detection connection for OUT9-10	19	STB	Serial data latch pulse input
3	RF2	Current detection connection for OUT11-12	13	CLK2/PWM	Stepping motor clock/PWM signal input for OUT5-8
36	SGND	Control system ground	14	IN51	Control input for OUT9-10
21	OUT1	Motor driver output	15	IN52	Control input for OUT9-10
22	OUT2	Motor driver output	16	IN61	Control input for OUT11-12
24	OUT3	Motor driver output	17	IN62	Control input for OUT11-12
25	OUT4	Motor driver output	35	PI	Photosensor drive output
10	OUT5	Motor driver output	1	BI1	Schmitt buffer input 1
9	OUT6	Motor driver output	40	BO1	Schmitt buffer output 1
7	OUT7	Motor driver output	39	BI2	Schmitt buffer input 2
6	OUT8	Motor driver output	38	BO2	Schmitt buffer output 2
27	OUT9	Motor driver output	32	BI3	Schmitt buffer input 3
29	OUT10	Motor driver output	31	BO3	Schmitt buffer output 3

Pin Assignment



Serial Data Input Overview

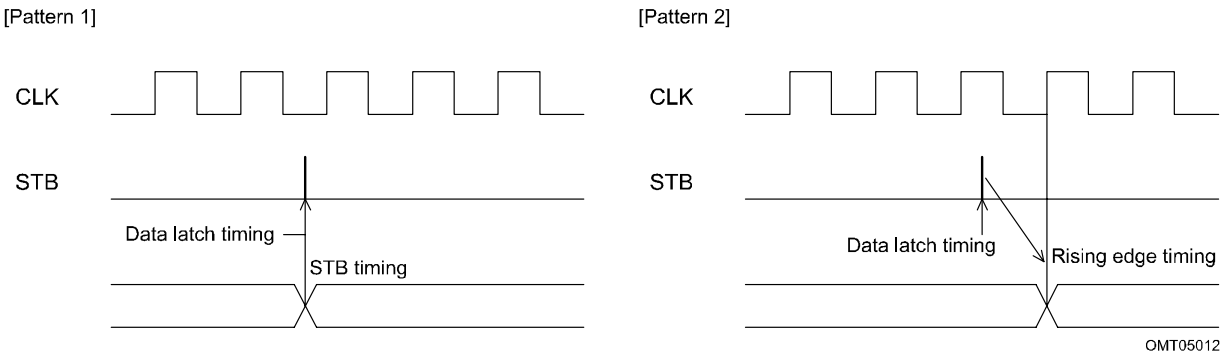
Serial Data Input Timing Chart



Data is input in order from D0 to D7. Data is transferred on the SCLK rising edge and, after all data has been transferred, the data is latched by the rising edge of the STB signal.
Note that the IC internal circuits will not accept the SCLK signal while the STB signal is high.

Timing with which the Serial Data is Reflected in the Outputs

Basically, the new values are reflected in the output at the point the data is latched with the STB signal. → Pattern 1
However, the "Excitation direction" and "Excitation mode" settings used in stepping motor clock drive mode for channels 1 through 4 are an exception. In this case only, after the data is latched with the STB signal, the new values are reflected on the next rising edge of the CLK signal. → Pattern 2



Detailed Description of Serial Data Input

Note: This IC's channels are assigned as follows.

OUT1/OUT2	→	Channel 1
OUT3/OUT4	→	Channel 2
OUT5/OUT6	→	Channel 3
OUT7/OUT8	→	Channel 4
OUT9/OUT10	→	Channel 5
OUT11/OUT12	→	Channel 6

Stepping motor excitation type for channels 1 through 4

This IC supports connecting stepping motors to channels 1 and 2 and to channels 3 and 4. Either of these stepping motors can be controlled by a single clock signal.

When this capability is used, the clock signal input pins and the channels as associated as shown below.

CLK1:	Controls channel 1 and 2 drive.
CLK2/PWM:	Controls channel 3 and 4 drive

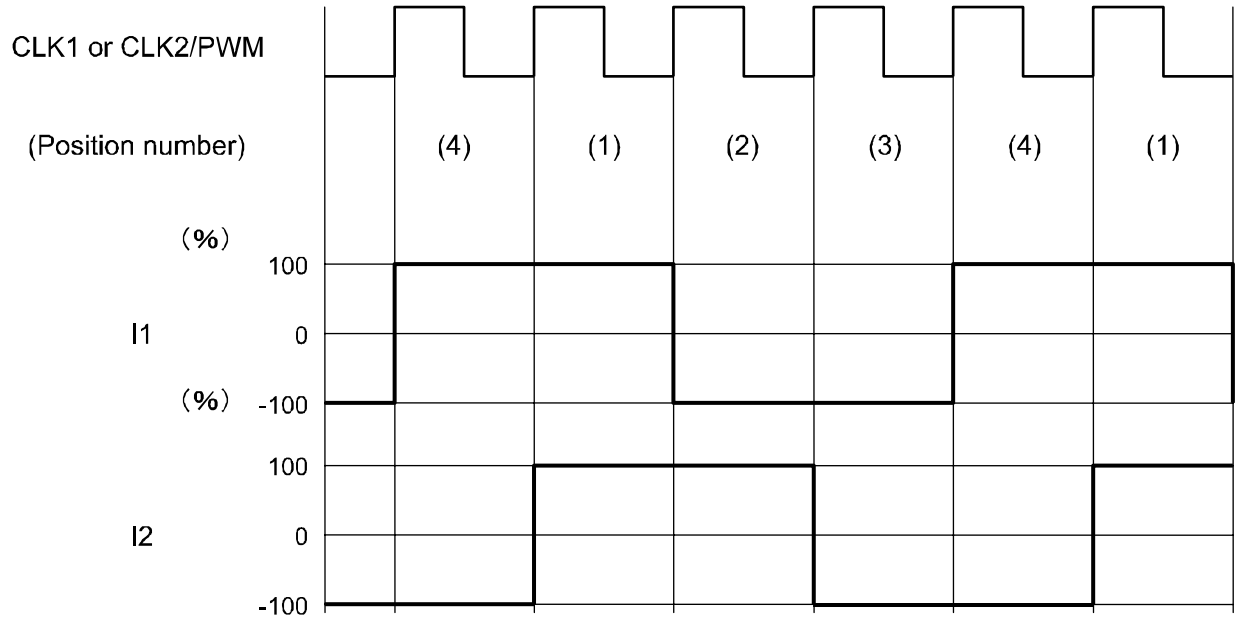
The following state settings related to control of these stepping motors are set using the serial data. (See subsection, Serial Logic Table 1, in section ,Truth Tables, for a detailed description of this data.)

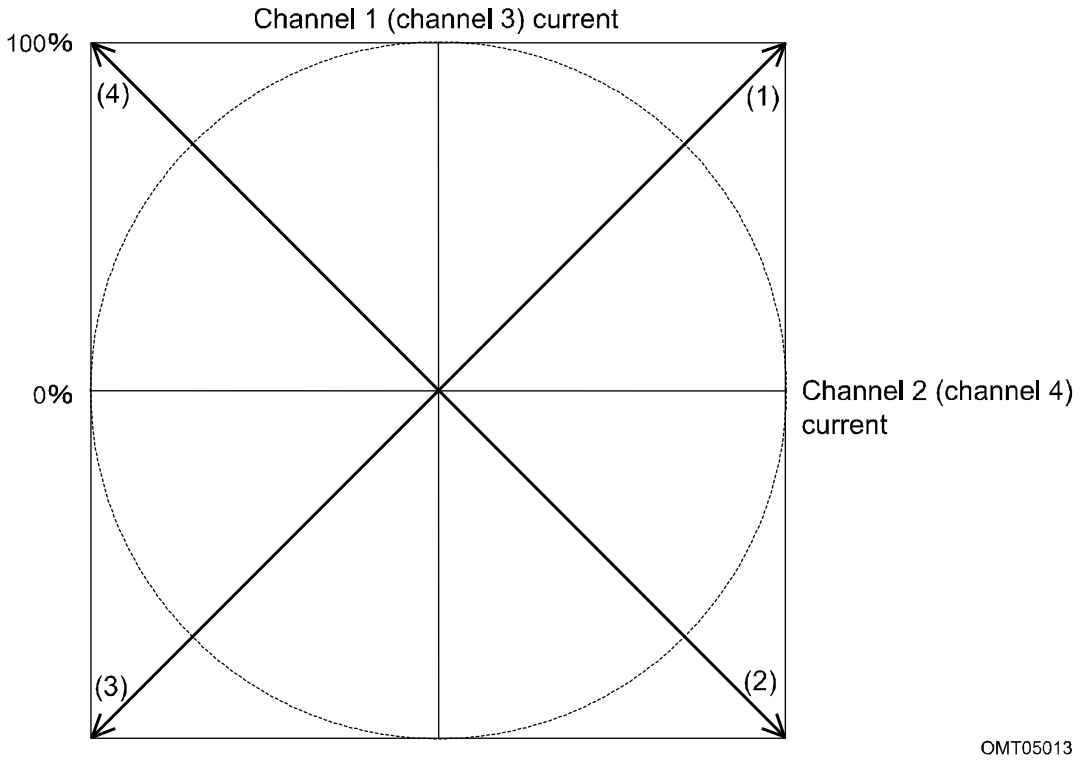
- Excitation mode: 2-phase excitation or 1-2 phase excitation
- Excitation direction: CW (clockwise) or CCW (counterclockwise)
- Step/Hold: Clear or Hold
- Counter reset: Normal Operation or Reset
- Output enable: Output Off or Output On
- VC voltage divisor: Selects one of 16 values
- VC voltage selection: Internal or External

Excitation Mode Setting

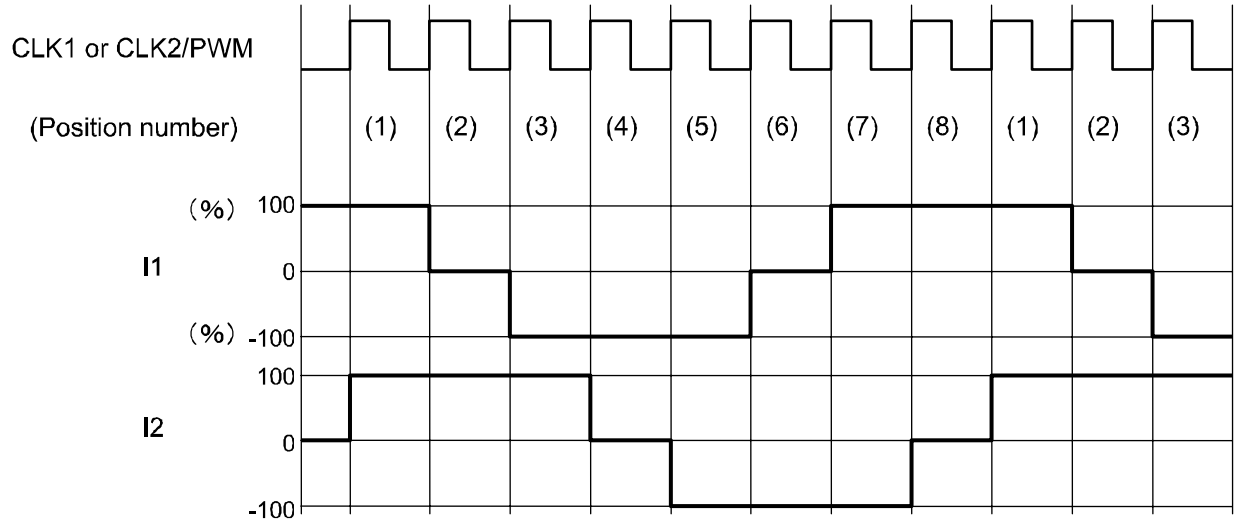
This section presents the timing charts for each excitation mode.

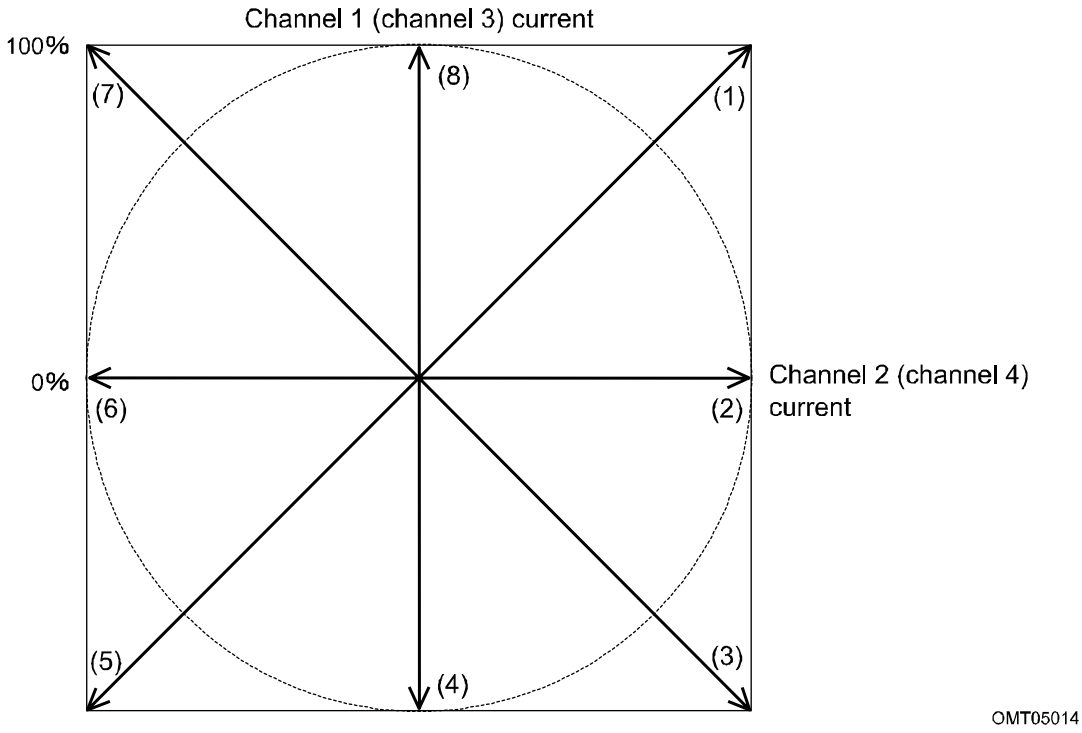
Two-Phase Excitation Timing Chart





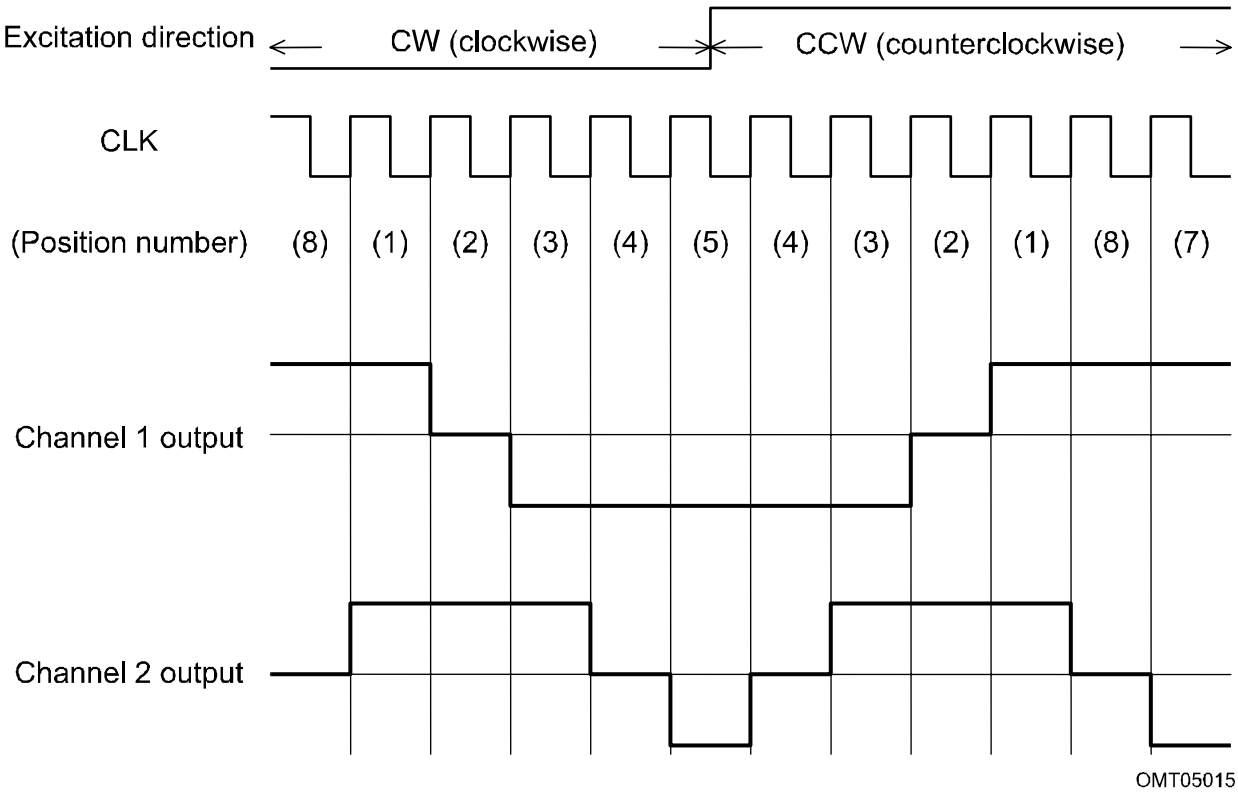
1-2 Phase Excitation Timing Chart



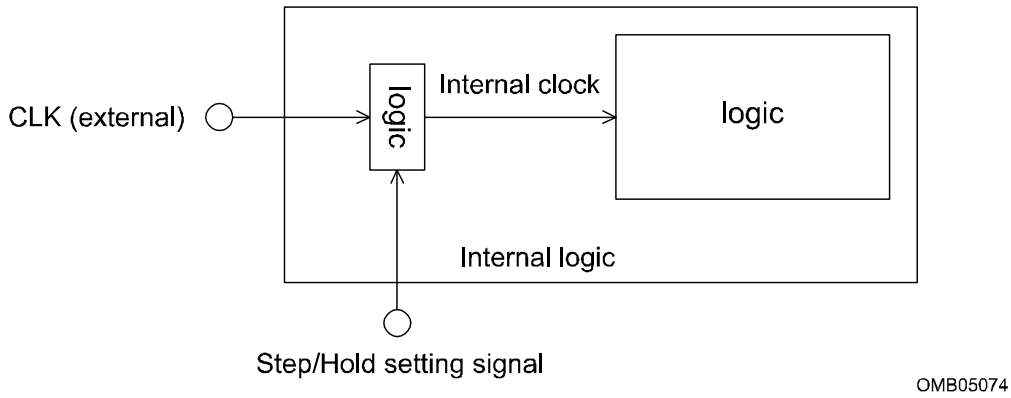


Sample Timing Chart for the Excitation Direction Setting

The excitation direction setting sets the excitation (rotation) direction of the stepping motor.
With the CW (clockwise) setting, the phase of the channel 2 current is delayed from that of the channel 1 current by 90°.
With the CCW (counterclockwise) setting, the phase of the channel 2 current leads that of the channel 1 current by 90°.



Step/Hold Operation Overview

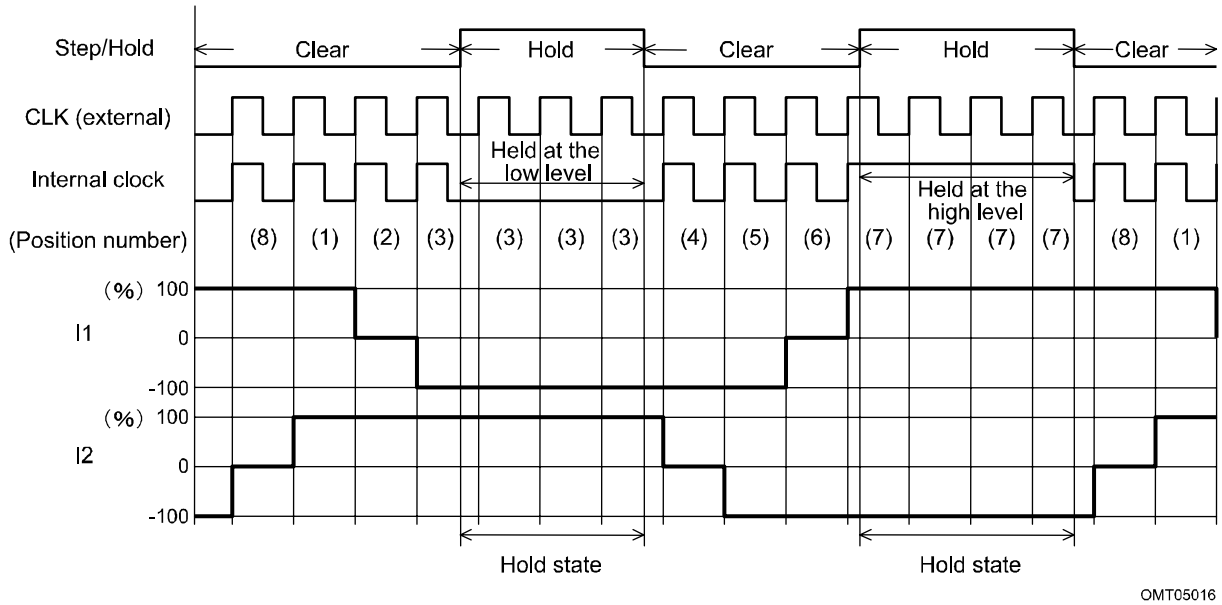


Sample Timing Chart for the Step/Hold Setting

When the Step/Hold data is set to the Hold state, the state of the external clock signal (CLK) at that time is latched and held as the internal clock signal.

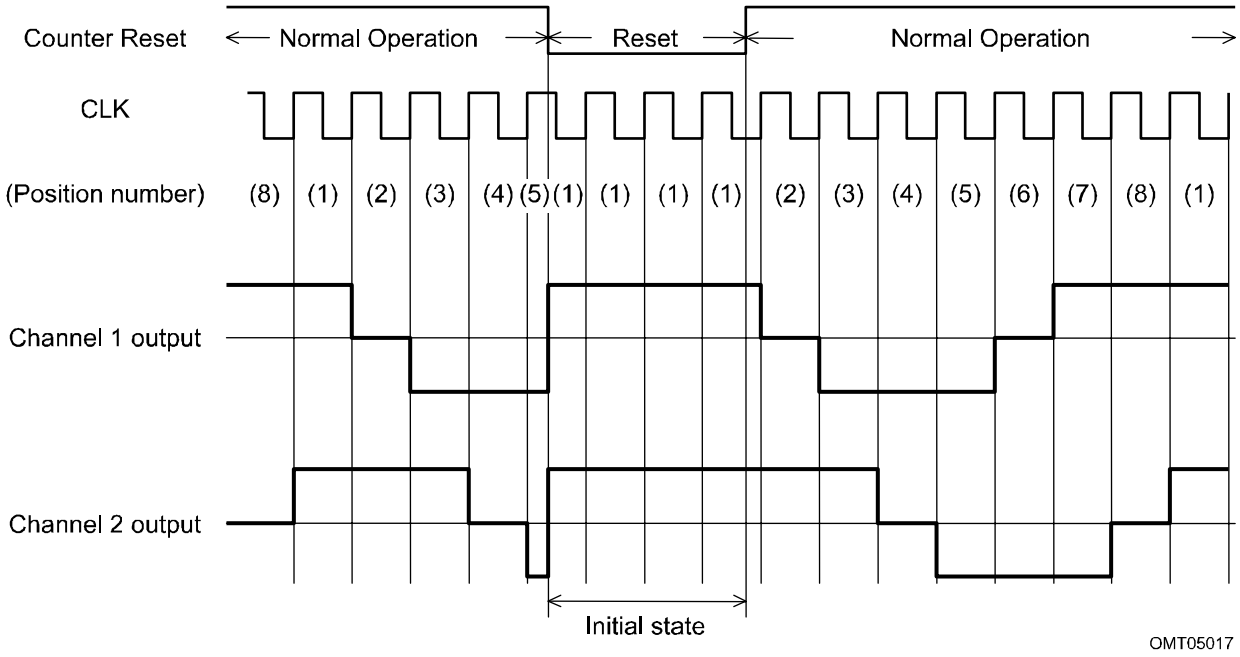
At the timing with which Step/Hold is set to the Hold state for the first time in the figure below, the internal clock signal will be held at the low level because the external clock (CLK) was at the low level. In contrast, at the timing with which Step/Hold is set to the Hold state for the second time, the internal clock signal will be held at the high level because the external clock (CLK) was at the high level.

When Step/Hold is set to the Clear state, the internal clock is synchronized with the external clock (CLK). The output holds the state it was in at the point Step/Hold is set to the Hold state, and advances on the next clock signal rising edge after Step/Hold is set to the Clear state.
As long as Step/Hold is in the Hold state, the position number does not advance even if an external clock (CLK) signal is applied.



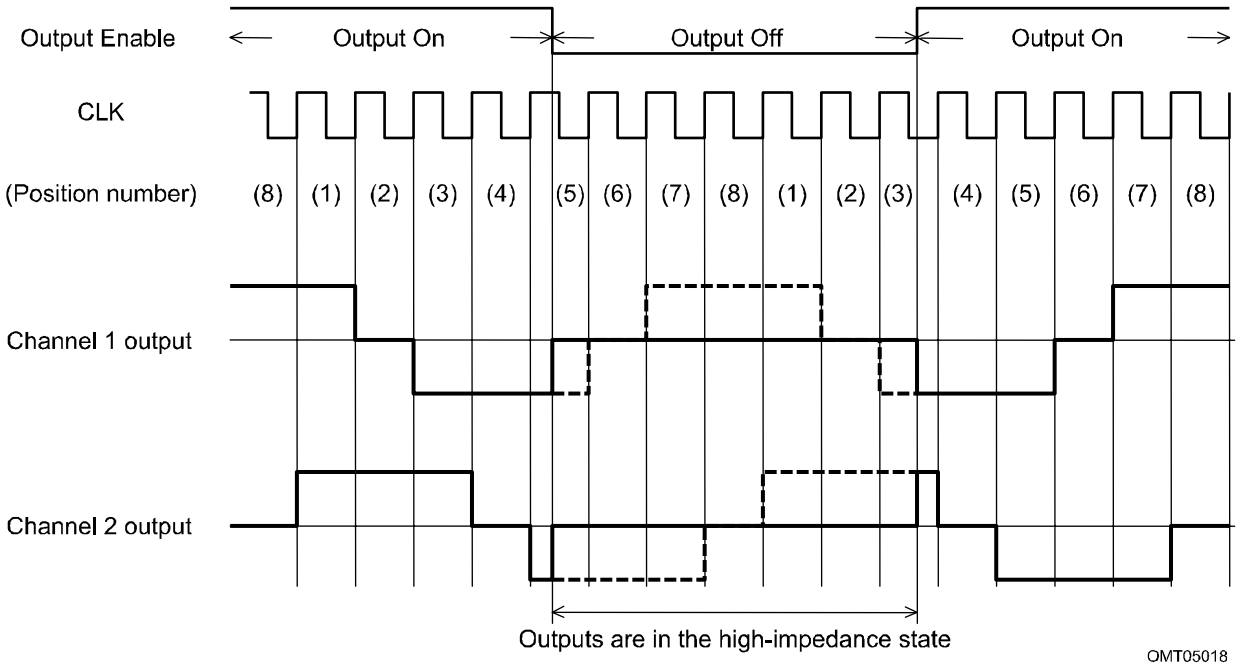
Sample Timing Chart for the Counter Reset Setting

When the Counter Reset setting is set to the Reset state, the output goes to the initial state on the rising edge of the STB signal. Then, when the Counter Reset setting is set to the Normal Operation (cleared) state, the output begins to advance the position number on the rising edge of the CLK signal following the rise of the STB signal.



Sample Timing Chart for the Output Enable Setting

When the Output Enable setting is set to the Output Off state, the outputs are turned off and set to the high-impedance state on the rising edge of the STB signal.
Note, however, that since the internal clock continues to operate, the position number advances as long as a clock signal (CLK) is input. Therefore, when the Output Enable setting is next set to the Output On (cleared) state, the output is turned on at the STB signal rising edge and the output levels at that time will be those for the position number to which the state has advanced due to the CLK signal input.



DC Motor and Voice Coil Motor Drive Methods (Channels 3 and 4)

When channels 3 and 4 are used to drive a DC or voice coil motor, the drive polarity is set with the serial data. The procedure for setting the drive polarity is shown below.
(See subsection, Serial Logic Table 2, in section, Truth Tables, for a detailed description of this data.)

Setting Procedure

(1) Select PWM signal input with the CLK2/PWM selection item in the serial data.
→ This sets up the signal input to the CLK2/PWM pin to be accepted as a PWM signal for channel 3 or channel 4. (In this case, it is not used as a clock signal.)
(2) If the output is to be controlled by PWM control, set up PWM mode and PWM signal allocation with the serial data.
(3) Set the drive polarity for each channel with the serial data.
(4) If the output is to be controlled by PWM control, input the PWM signal to the CLK2/PWM pin.
The following tables describe the correspondence between the PWM signal and the output logic.

Operation in Slow Decay Mode (forward/reverse ↔ brake)

Serial input				PWM input	Output				Mode
D4	D5	D6	D7	CLK2/PWM	OUT5	OUT6	OUT7	OUT8	
0	0			L	OFF	OFF			Standby mode
1	0				H	L			OUT5 → OUT6
0	1				L	H			OUT6 → OUT5
1	1				L	L			Brake mode
		0	0				OFF	OFF	Standby mode
		1	0				H	L	OUT7 → OUT8
		0	1				L	H	OUT8 → OUT7
		1	1				L	L	Brake mode
0	0			H	OFF	OFF			Standby mode
1	0				L	L			Brake mode
0	1				L	L			Brake mode
1	1				L	L			Brake mode
		0	0				OFF	OFF	Standby mode
		1	0				L	L	Brake mode
		0	1				L	L	Brake mode
		1	1				L	L	Brake mode

Operation in Fast Decay Mode (forward/reverse ↔ standby mode)

Serial input				PWM input	Output				Mode
D4	D5	D6	D7	CLK2/PWM	OUT5	OUT6	OUT7	OUT8	
0	0			L	OFF	OFF			Standby mode
1	0				H	L			OUT5 → OUT6
0	1				L	H			OUT6 → OUT5
1	1				L	L			Brake mode
		0	0				OFF	OFF	Standby mode
		1	0				H	L	OUT7 → OUT8
		0	1				L	H	OUT8 → OUT7
		1	1				L	L	Brake mode
0	0			H	OFF	OFF			Standby mode
1	0				OFF	OFF			Standby mode
0	1				OFF	OFF			Standby mode
1	1				L	L			Brake mode
		0	0				OFF	OFF	Standby mode
		1	0				OFF	OFF	Standby mode
		0	1				OFF	OFF	Standby mode
		1	1				L	L	Brake mode

Constant Voltage Control Setup Procedure for Channels 1 to 4

The constant voltage set value for channels 1 to 4 can be set separately for channels 1 and 2 and for channels 3 and 4. (See subsections, Serial Logic Table 3, and, Serial Logic Table 4, in section, Truth Tables, for a detailed description of this data.)

The reference voltage used as the basis for operation can be selected to be either the internal reference voltage (0.88V) or the external input voltage (the voltage applied to the VC pin).
The reference voltage selected as described above is voltage divided by the ratio set by the VC voltage divisor set by the serial data. The result of that voltage division operation is multiplied by five by the output constant voltage circuit and then output.
The following formulas can be used to calculate the output constant voltage for the individual cases.

When the internal reference voltage is used:
(output constant voltage) = (internal reference voltage (0.88 V)) × (VC voltage divisor) × 5

When the external reference voltage (VC input voltage) is used:
(output constant voltage) = (VC input voltage) × (VC voltage divisor) × 5

Voice Coil Motor and Stepping Motor Drive Methods (Channels 5 and 6)

When channel 5 or 6 is used to drive either a voice coil motor or stepping motor, the drive polarity can be set with either serial data or parallel data (the IN51, IN52, IN61, and IN62 input signals).
This section describes the procedures used for these settings.
(See subsection, Serial Logic Table 2, in section, Truth Tables, for a detailed description of this data.)

Setting Procedure Using Serial Data

A: Channel 5
1. Set the IN51 and IN52 pins to the low level. (Alternative, they may be left open.)
2. Set the drive polarity with the serial data

B: Channel 6
1. Set the IN61 and IN62 pins to the low level. (Alternative, they may be left open.)
2. Set the drive polarity with the serial data

Setting Procedure Using Parallel Data

The IN51 and IN52 pins are used to set the channel 5 drive polarity and the IN61 and IN62 pins are used to set the channel 6 drive polarity.

The truth table for this function is shown below.

Parallel inputs				Outputs				Mode	
IN51	IN52	IN61	IN62	OUT9	OUT10	OUT11	OUT12		
L	L			L	L			Standby mode	Serial priority
L	H			L	H			OUT10 → OUT9	Parallel priority
H	L			H	L			OUT9 → OUT10	
H	H			L	L			Brake	
		L	L			L	L	Standby mode	Serial priority
		L	H			L	H	OUT12 → OUT11	Parallel priority
		H	L			H	L	OUT11 → OUT12	
		H	H			L	L	Brake	

Constant Current Control Settings (channels 5 and 6)

The constant current settings for channels 5 and 6 are set individually for each channel.
(See subsection, Serial Logic Table 5, in section, Truth Tables, for a detailed description of this data.)

The output constant current is set by the constant current reference voltage set with the serial data and the resistor (RF) connected between the RF1 and RF2 pins.
The following formula can be used to calculate the output constant current.

(output constant current) = (constant current reference voltage) / (value of the resistor RF)

PI Output Drive Method

When the PI output is used to drive a photosensor, the drive on/off state is set from the serial data.
(See subsection, Serial Logic Table 5, in section, Truth Tables, for a detailed description of this data.)

Schmitt Buffer Hysteresis Setting

The presence or absence of hysteresis in the BO1, BO2, and BO3 Schmitt buffer outputs can be set individually with the serial data.
(See subsection, Serial Logic Table 5, in section, Truth Tables, for a detailed description of this data.)

Truth Tables

Serial Logic Table 1

Input								Setting mode	Content set	Notes	Channels set						PI	Serial data activation timing		
D0	D1	D2	D3	D4	D5	D6	D7				1ch	2ch	3ch	4ch	5ch	6ch		CLK1	CLK2	STB
0	0	0	0	*	*	*	*	AF Excitation Direction	CW (clockwise)		○	○						○		
			1	*	*	*	*		CCW (counterclockwise)											
			*	0	*	*	*	AF Excitation mode	2-phase excitation											
			*	1	*	*	*		1-2 phase excitation											
			*	*	0	*	*	AF Step/Hold	Clear											○
			*	*	1	*	*		Hold											
			*	*	*	0	*	AF Counter Reset	Reset											
			*	*	*	1	*		Clear											
			*	*	*	*	0	AF Output Enable	Output Off											
			*	*	*	*	1		Output On											
1	0	0	0	*	*	*	*	Zoom Excitation Direction	CW (clockwise)				○	○					○	
			1	*	*	*	*		CCW (counterclockwise)											
			*	0	*	*	*	Zoom Excitation Mode	2-phase excitation											
			*	1	*	*	*		1-2 phase excitation											
			*	*	0	*	*	Zoom Step/Hold	Clear											○
			*	*	1	*	*		Hold											
			*	*	*	0	*	Zoom Counter Reset	Reset											
			*	*	*	1	*		Clear											
			*	*	*	*	0	Zoom Output Enable	Output Off											
			*	*	*	*	1		Output On											

Serial Logic Table 2

Input								Setting mode	Content set	Notes	Channels set						PI	Serial data activation timing		
D0	D1	D2	D3	D4	D5	D6	D7				1ch	2ch	3ch	4ch	5ch	6ch		CLK1	CLK2	STB
0	1	0	0	0	0	*	*	OUT5-6 drive polarity (3ch)	OFF				○							○
				1	0	*	*		OUT5 → OUT6	*1										
				0	1	*	*		OUT6 → OUT5											
				1	1	*	*		Brake											
				*	*	0	0	OUT7-8 drive polarity (4ch)	OFF					○						
				*	*	1	0		OUT7 → OUT8	*1										
				*	*	0	1		OUT8 → OUT7											
				*	*	1	1		Brake											
			1	0	0	*	*	OU9-10 drive polarity (5ch)	OFF	*2					○					
				1	0	*	*		OUT9 → OUT10											
				0	1	*	*		OUT10 → OUT9											
				1	1	*	*		Brake											
				*	*	0	0	OUT11-12 drive polarity (6ch)	OFF	*3						○				
				*	*	1	0		OUT11 → OUT12											
				*	*	0	1		OUT12 → OUT11											
				*	*	1	1		Brake											
1	1	0	0	*	*	*	*	CLK2/PWM selection	CLK2 signal input	*4			○	○						○
			1	*	*	*	*		PWM signal input											
			*	0	*	*	*	PWM mode	Slow Decay (Forward/reverse ↔ brake)	*5										
			*	1	*	*	*		Fast Decay (Forward/reverse ↔ standby mode)	*6										
			*	*	0	0	*	PWM signal allocation	OFF											
			*	*	1	0	*		Channel 3 only											
			*	*	0	1	*		Channel 4 only											
			*	*	1	1	*		Both channels 3 and 4											
			*	*	*	*	0	(Dummy data)												
			*	*	*	*	1													

Serial Logic Table 3

Input								Setting mode	Content set	Notes	Channels set						PI	Serial data activation timing		
D0	D1	D2	D3	D4	D5	D6	D7				1ch	2ch	3ch	4ch	5ch	6ch		CLK1	CLK2	STB
0	0	1	0	0	0	0	*	VC voltage divisor (The values in parentheses indicate the output voltage value when the internal reference voltage (0.88V) is used.)	100% (4.4V)	*7	○	○								○
			1	0	0	0	*		97.7% (4.3V)											
			0	1	0	0	*		95.5% (4.2V)											
			1	1	0	0	*		93.2% (4.1V)											
			0	0	1	0	*		90.9% (4.0V)											
			1	0	1	0	*		88.6% (3.9V)											
			0	1	1	0	*		86.4% (3.8V)											
			1	1	1	0	*		84.1% (3.7V)											
			0	0	0	1	*		81.8% (3.6V)											
			1	0	0	1	*		79.5% (3.5V)											
			0	1	0	1	*		77.3% (3.4V)											
			1	1	0	1	*		75.0% (3.3V)											
			0	0	1	1	*		72.7% (3.2V)											
			1	0	1	1	*		70.5% (3.1V)											
			0	1	1	1	*		68.2% (3.0V)											
			1	1	1	1	*		65.9% (2.9V)											
			*	*	*	*	0	VC voltage selection	Internal reference voltage (0.88V)											
			*	*	*	*	1		VC input voltage											

Serial Logic Table 4

Input								Setting mode	Content set	Notes	Channels set						PI	Serial data activation timing		
D0	D1	D2	D3	D4	D5	D6	D7				1ch	2ch	3ch	4ch	5ch	6ch		CLK1	CLK2	STB
1	0	1	0	0	0	0	*	VC voltage Divisor (The values in parentheses indicate the output voltage value when the internal reference voltage (0.88V) is used.)	100% (4.4V)	*7			○	○						○
			1	0	0	0	*		97.7% (4.3V)											
			0	1	0	0	*		95.5% (4.2V)											
			1	1	0	0	*		93.2% (4.1V)											
			0	0	1	0	*		90.9% (4.0V)											
			1	0	1	0	*		88.6% (3.9V)											
			0	1	1	0	*		86.4% (3.8V)											
			1	1	1	0	*		84.1% (3.7V)											
			0	0	0	1	*		81.8% (3.6V)											
			1	0	0	1	*		79.5% (3.5V)											
			0	1	0	1	*		77.3% (3.4V)											
			1	1	0	1	*		75.0% (3.3V)											
			0	0	1	1	*		72.7% (3.2V)											
			1	0	1	1	*		70.5% (3.1V)											
			0	1	1	1	*		68.2% (3.0V)											
			1	1	1	1	*		65.9% (2.9V)											
			*	*	*	*	0	VC voltage selection	Internal reference voltage (0.88V)											
			*	*	*	*	1		VC input voltage											

Serial Logic Table 5

Input								Setting mode	Content set	Notes	Channels set						PI	Serial data activation timing		
D0	D1	D2	D3	D4	D5	D6	D7				1ch	2ch	3ch	4ch	5ch	6ch		CLK1	CLK2	STB
0	1	1	0	0	0	0	*	Constant current reference voltage	0.200V						○	○				○
			1	0	0	0	*		0.170V											
			0	1	0	0	*		0.165V											
			1	1	0	0	*		0.160V											
			0	0	1	0	*		0.155V											
			1	0	1	0	*		0.150V											
			0	1	1	0	*		0.145V											
			1	1	1	0	*		0.140V											
			0	0	0	1	*		0.135V											
			1	0	0	1	*		0.130V											
			0	1	0	1	*		0.125V											
			1	1	0	1	*		0.120V											
			0	0	1	1	*		0.115V											
			1	0	1	1	*		0.110V											
			0	1	1	1	*		0.105V											
			1	1	1	1	*		0.100V											
			*	*	*	*	0	Channel selection	OUT9-10 (5ch)											
			*	*	*	*	1		OUT11-12 (6ch)											
1	1	1	0	*	*	*	*	Photosensor drive	OFF								○			○
			1	*	*	*	*		ON											
			*	0	*	*	*	Buffer output hysteresis (BI1/BO1)	Absent											
			*	1	*	*	*		Present											
			*	*	0	*	*	Buffer output hysteresis (BI2/BO2)	Absent											
			*	*	1	*	*		Present											
			*	*	*	0	*	Buffer output hysteresis (BI3/BO3)	Absent											
			*	*	*	1	*		Present											
			*	*	*	*	0	(Dummy data)												
			*	*	*	*	1													

Notes

*1. The operating mode can be switched between forward (or reverse) ↔ brake mode and forward (or reverse) ↔ standby mode operation with the CLK2/PWM pin in combination with notes 5 and 6 below.

*2. These serial inputs are only accepted when the parallel inputs IN51 and IN52 are both at the low level. In all other states, the serial input will be ignored.

*3. These serial inputs are only accepted when the parallel inputs IN61 and IN62 are both at the low level. In all other states, the serial input will be ignored.

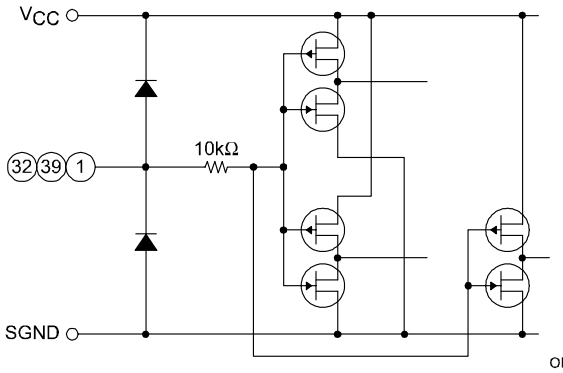
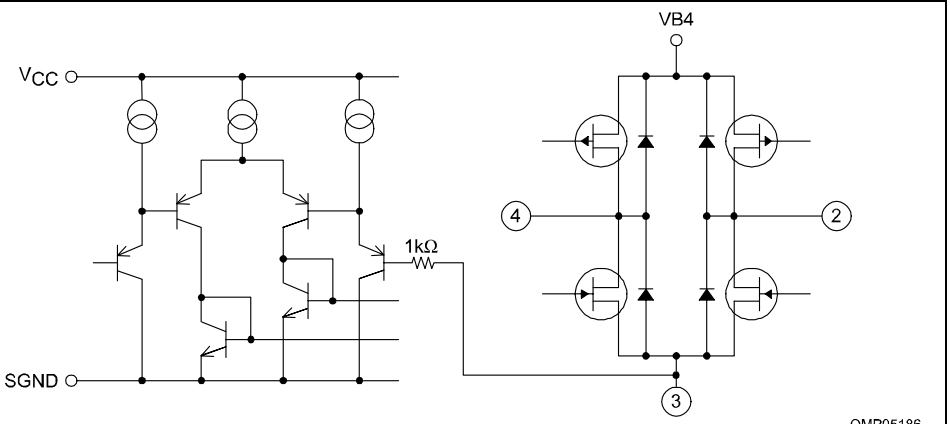
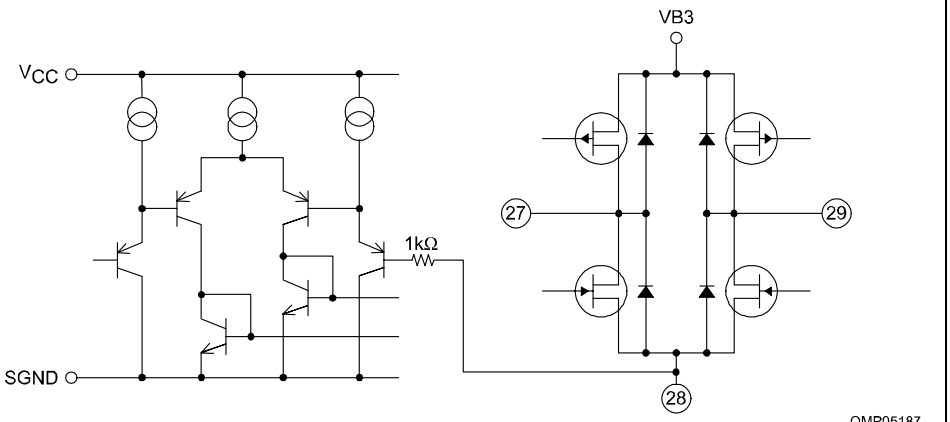
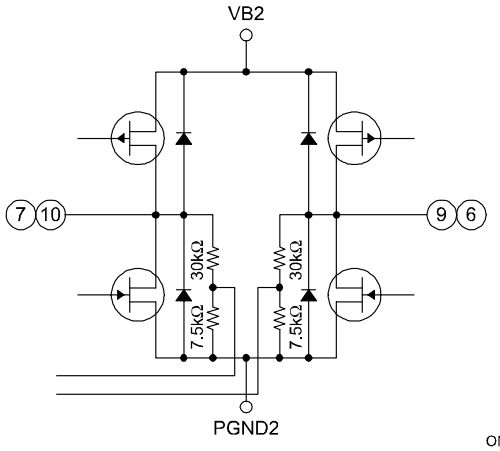
*4. Selects whether the CLK2/PWM input functions as a stepping motor clock (CLK2) or a DC motor PWM signal (PWM).

*5. Forcibly switches the logic of note 1 to brake mode when the CLK2/PWM input is high.

*6. Forcibly switches the logic of note 1 to standby mode when the CLK2/PWM input is high.

*7. Voltage divisor for the VC voltage divider circuit. After either the VC input voltage or the internal reference voltage is voltage divided by this ratio, the result of that division is multiplied by five by the output constant voltage circuit.

Pin Internal Equivalent Circuits

Pin No.	Symbol	Equivalent circuit
1 39 32	BI1 BI2 BI3	
4 2 3	OUT11 OUT12 RF2	
27 29 28	OUT9 OUT10 RF1	
10 9 7 6	OUT5 OUT6 OUT7 OUT8	

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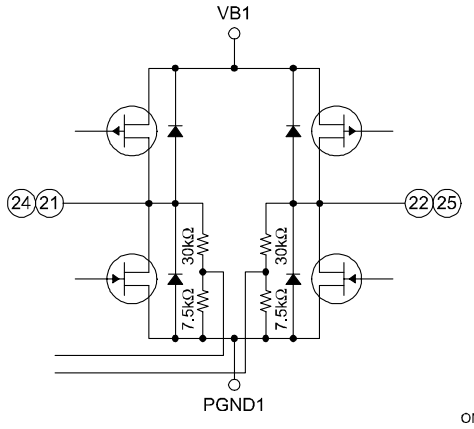
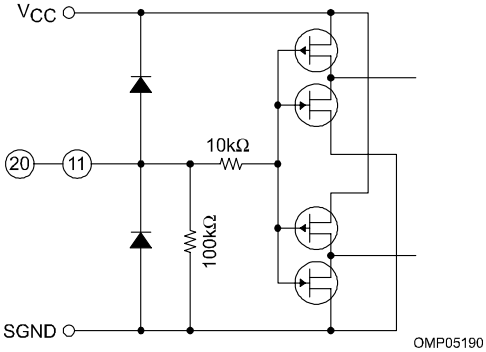
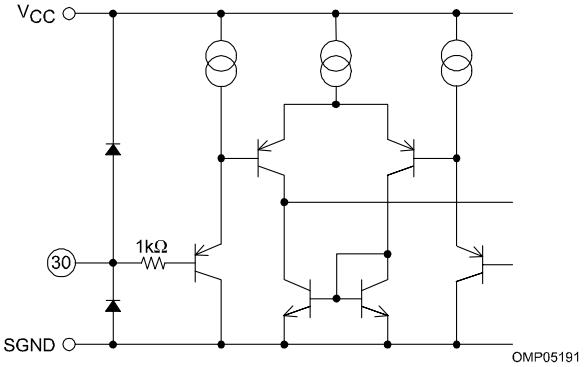
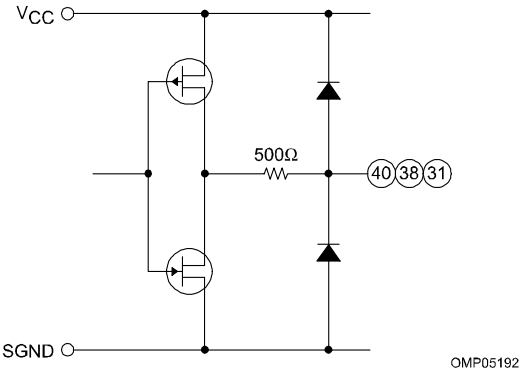
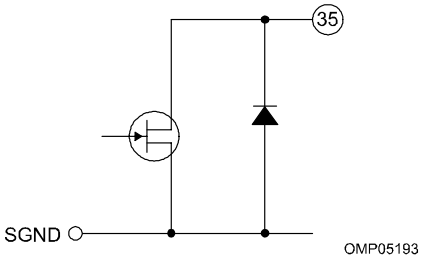
Pin No.	Symbol	Equivalent circuit
21 22 24 25	OUT1 OUT2 OUT3 OUT4	
11 12 13 14 15 16 17 18 19 20	ST CLK1 CLK2/PWM IN51 IN52 IN61 IN62 SCLK STB DATA	
30	VC	
40 38 31	BO1 BO2 BO3	
35	PI	

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