Ordering number : ENA1850

SANYO Semiconductors
DATA SHEET

LV8063TT — Bi-CMOS IC Fan Motor Driver Single-Phase Full-Wave Driver

Overview

The LV8063TT is the driver IC with BTL linear output for single-phase fan motor, and that drives at high efficiency, low power, and low noise by suppressing the reactive power.
The BTL output can be combined with the PWM control by an external signal, which is optimum for the note PC, the CPU cooler, etc. that requires low power dissipation and low noise.

Functions

- Single-phase full-wave operating by BTL output (BTL amplifier gain : +43dB)
- Speed control available by PWM pin
- Built-in Quick Start circuit
- Built-in thermal-shutdown (TSD) circuit
- Hall bias output pin (VHB = 1.05V typ)
- FG(rotation signal) output pin (Open drain output)
- Built-in lock protection and automatic return circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7	V
OUT pin output current	I_{OUT} max1	In regular mode	0.7	A
	I_{OUT} max2	In lock-detection mode	1	A
OUT pin output voltage handling	V_{OUT} max		7	V
FG output voltage handling	V_{FG} max		7	V
FG output current	I_{FG} max		5	mA
HB output current	I_{HB} max		10	mA
Allowable power dissipation	Pd max1	Independent IC	0.2	W
	Pd max2	IC on board *	0.4	W
Operating temperature	Topr		-30 to +95	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified substrate : 20mm × 10mm × 0.8mm, Paper phenol

Recommended Operating Conditions at Ta = 25°C

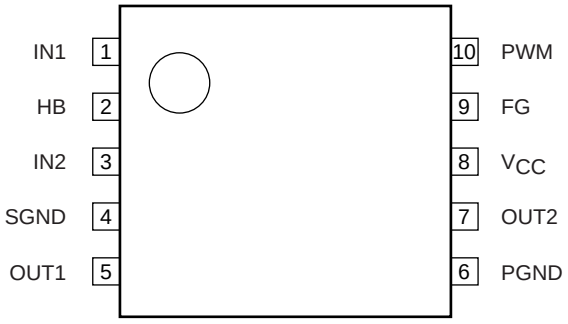
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} opg	Active at all circuit	2.5 to 6.0	V
	V_{CC} min	Start-up with PWM=H	2.2 to 6.0	V
Hall input common-mode input voltage range	VICM		0.3 to V_{CC}-1.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	I_{CC}	Active		1.5	3.0	mA
	I_{CCO}	Stand-by		200	300	μA
HB bias voltage	VHB	IHB = 5mA	0.9	1.05	1.2	V
Hall input bias current	IHIN				1	μA
Output On voltage	V_O	I_O = 250mA, source + sink		0.25	0.35	V
Hall amplifier output offset voltage	V_{IN}OFS		-6		6	mV
Hall amplifier voltage gain	GH		39	43	47	dB
PWM pin input Low level	VPWML		0		0.7	V
PWM pin input High level	VPWMH		2.5		V_{CC}	V
PWM input frequency	fPWM	Design guarantee *	20		50	kHz
PWM input smallest pulse width	TPWM	Design guarantee *		5		μs
FG output low-level voltag	V_{FG}	I_{FG} = 3mA			0.3	V
FG output leakage current	I_{FGL}	V_{FG} = 7V			10	μA
FG comparator hysteresis width	ΔV_{HYS}		±5	±15	±20	mV
Output on time in Lock-detection	TACT		0.45	0.6	0.75	sec
Output off time in Lock-detection	TDET		4.5	6	7.5	sec
Output on/off ratio in Lock-detection	TRTO	TRTO=TDET/TACT	8	10	11	
Thermal shutdown operating temperature	TSD	Design guarantee *		180		°C
Thermal shutdown hysteresis width	ΔTSD	Design guarantee *		40		°C

* Design guarantee: Indicates a design target value. These parameters are not tested in the independent IC.

Pin Assignment

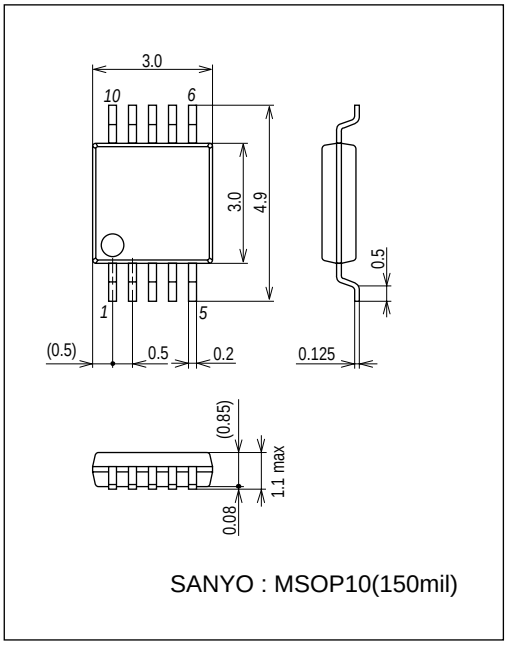


Top view

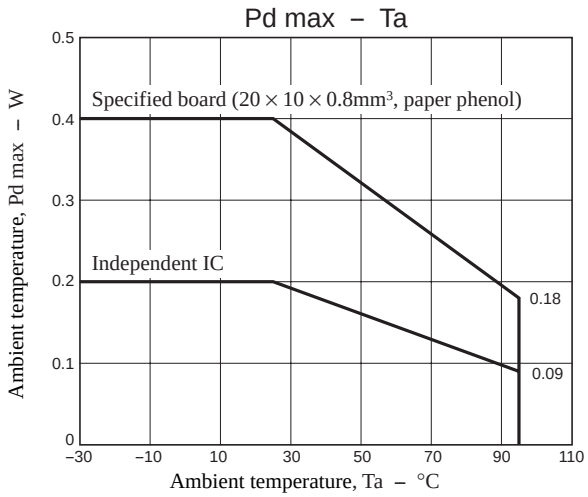
Package Dimensions

unit : mm (typ)

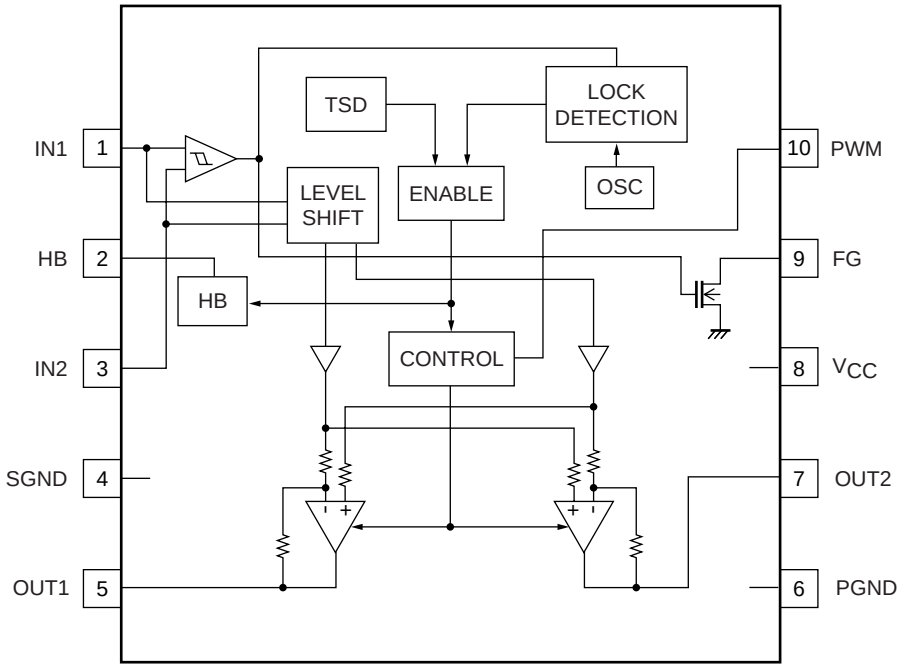
3297



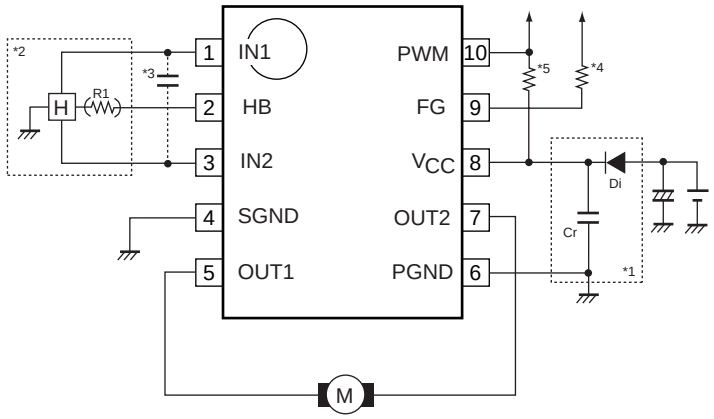
SANYO : MSOP10(150mil)



Block Diagram



Sample Application Circuit



*1 When the diode Di is used to prevent device destruction from reverse connection, the capacitor Cr must be inserted to assure a path for regenerative currents.
Similarly, if there no nearby capacitors on the fan power supply line, the capacitor Cr is also required to increase reliability.

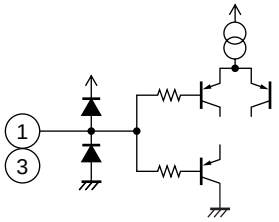
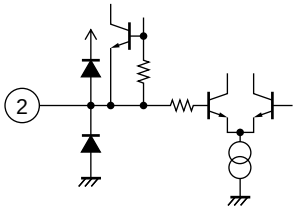
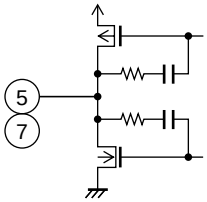
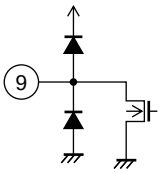
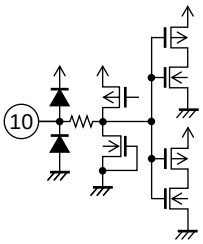
*2 The Hall element is biased at a constant voltage of approximately 1.05Vfrom the HB pin.
Thus LV8063TT provides a stable Hall output with excellent temperature characteristics.
If the Hall output is needed to adjust the amplitude, use the resistor R1 as shown in the figure.

*3 When the wiring from the Hall output to IC Hall input is long, noise may be carried through the wiring. In this case, insert the capacitor as shown in the figure.

*4 This pin must be left open if unused.

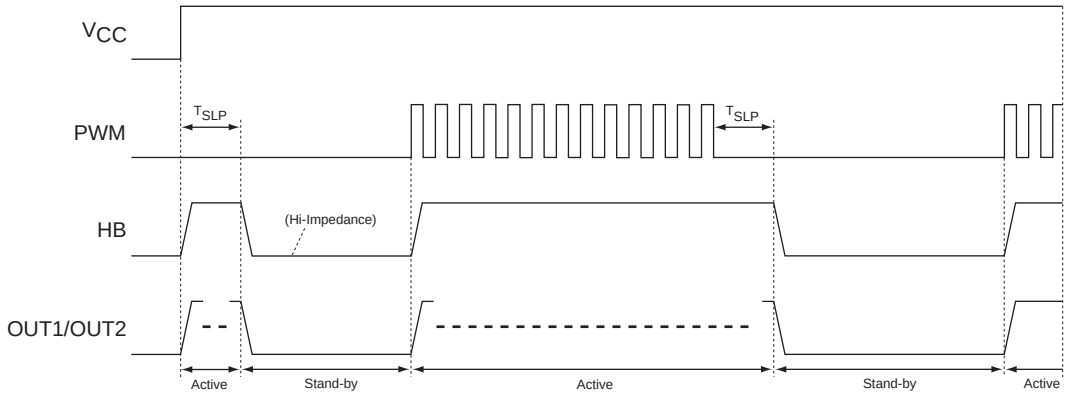
*5 When a PWM signal seems to be the open collector (a drain) output, please connect suitable pulling up resistance so that a H/L level is decided.

Pin Description

Pin No.	Pin name	Pin voltage	Description	Equivalent circuit
1	IN1	-	Hall input pin (+)	
3	IN2		Hall input pin (-)	
2	HB	1.05V (typ)	Hall bias output pin	
4	SGND	0V	Signal ground pin	
5	OUT1	-	Motor drive output pin	
7	OUT2			
6	PGND	0V	Power ground pin	
8	V_{CC}	2.5V to 6.0V	Voltage supply pin	
9	FG	-	FG pulse output pin	
10	PWM	-	PWM control input pin	

Timing Chart

Stand-by/Start-up

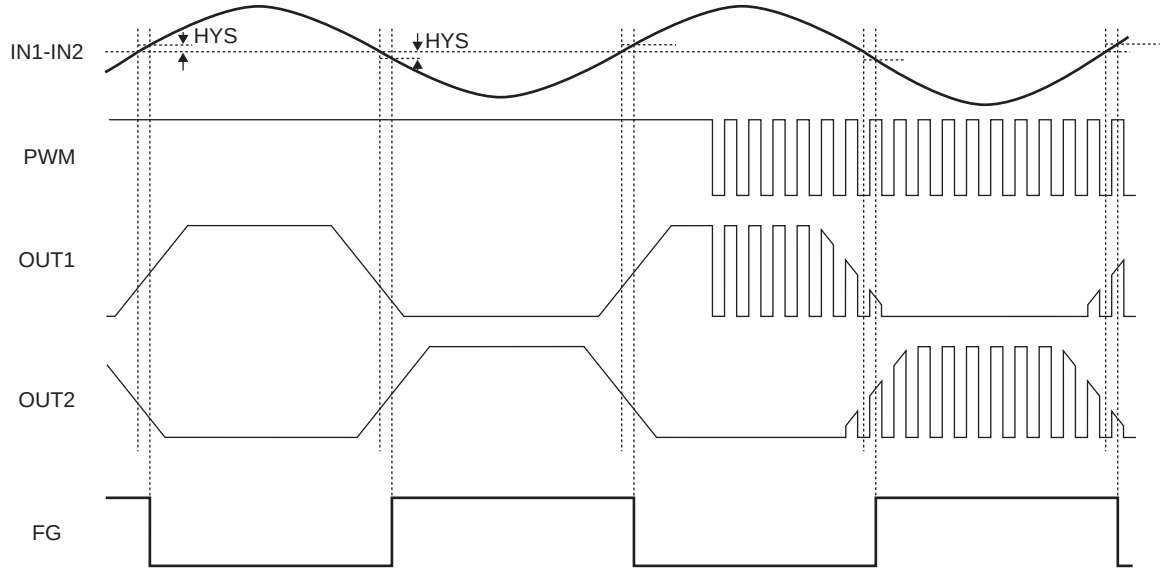


*T_{SLP}=800μs(typ)

*When PWM signal is input “L” level for continuousness TSLP, it becones the Stand-by mode by detecting above situation.

*When “H” level is input, it becomes the Active mode at once.

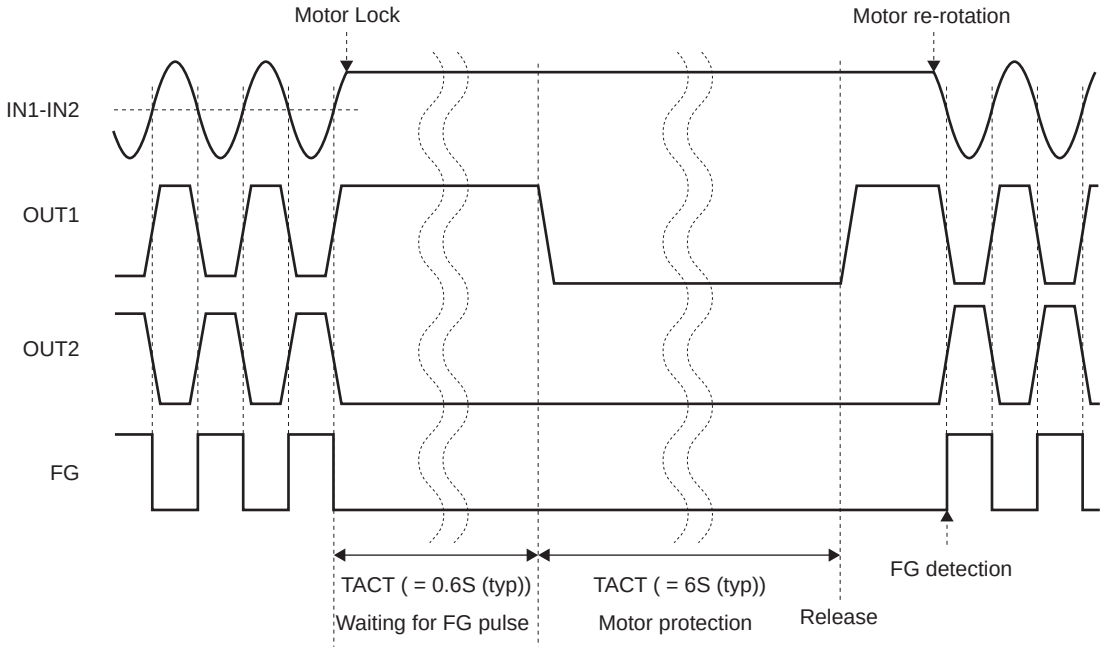
In Regular-Rotation



*Truth Table When Steady Rotation

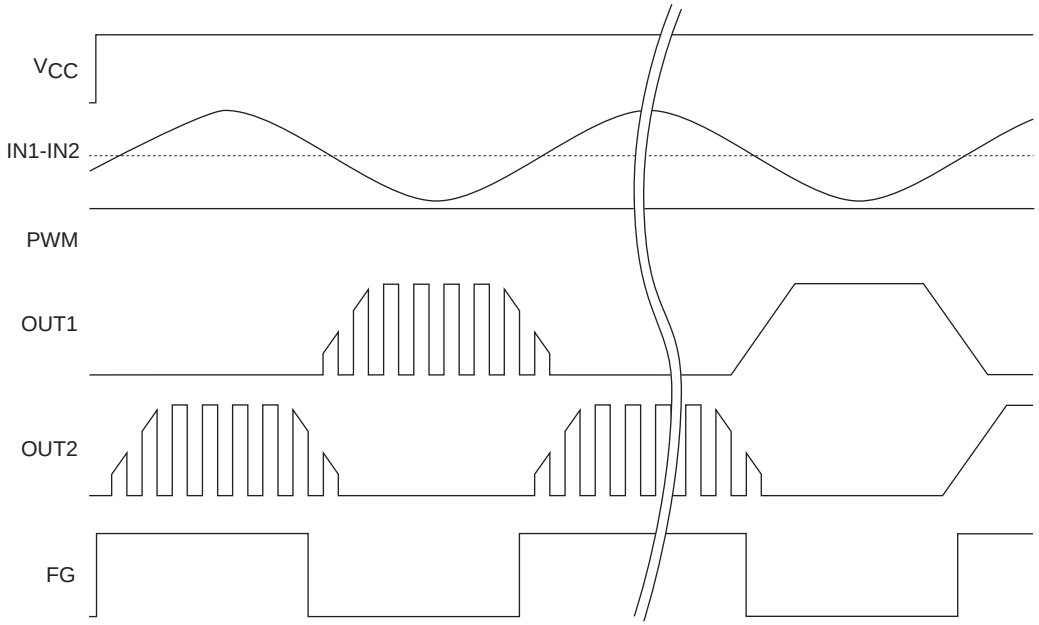
IN1	IN2	*PWM	OUT1	OUT2	FG	Mode
H	L	H	H	L	L	drive
		L	L	L		regeneration
L	H	H	L	H	OFF	drive
		L	L	L		regeneration

In Motor-Lock



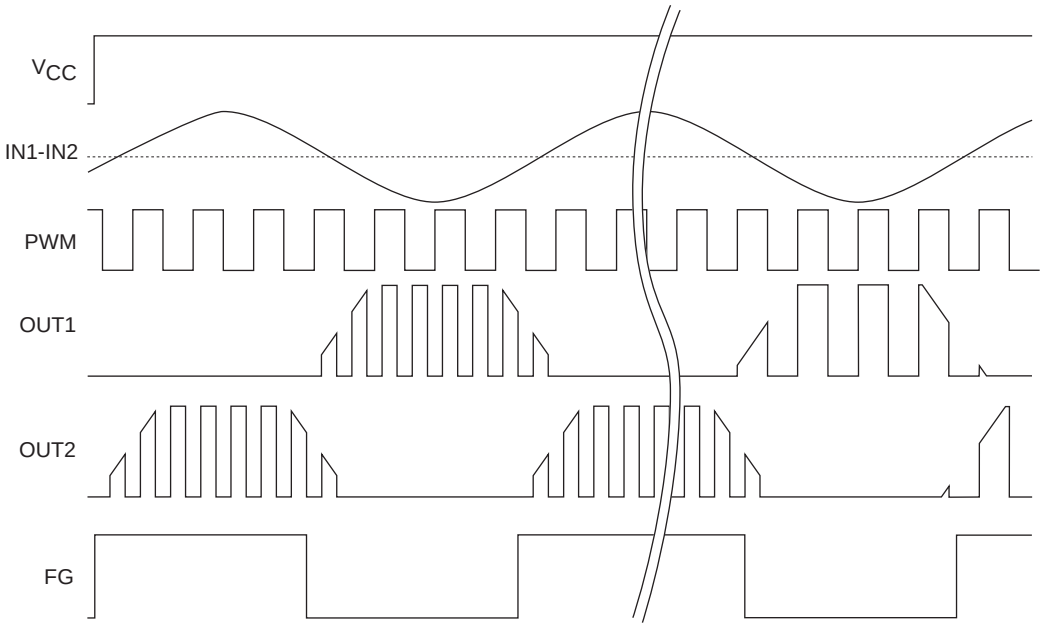
* When motor protection is activated, both OUT1 and OUT2 output low level.

When the circuit operates making amends starting (PWM pin = H)



When the power supply is turned on, the standby release (quick start), and the lock protection is released, the start amends operation is done.

When the circuit operates making amends starting (PWM pin = PWM signal input)



When the power supply is turned on, the standby release (quick start), and the lock protection is released, the start amends operation is done.