SANYO

SANYO Semiconductors
DATA SHEET

LV8092GQ — Bi-CMOS LSI
Piezo Actuator Driver IC

Overview

The LV8092GQ is a piezoelectric actuator driver IC. It internally generates drive waveforms and this makes it possible to control piezoelectric actuators with simple instructions.

Features

- Actuators using piezoelectric elements can be driven simply by I²C communication.
- The piezoelectric drive waveforms are set externally by serial input signals using the I²C interface.
- The rising and falling timings are determined with clock count.
- EN input that controls the startup/stop of the IC.
- The time for which the actuator is driven is determined with the drive frequency setting based on I²C communication.
- Provides a busy signal output during periods when the actuator is being driven by OUT pin output so that applications can be aware of the actuator operating/stopped state.
- Built-in thermal protection and undervoltage protection circuits

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		-0.5 to 6.0	V
Signal system supply voltage	V_{DD} max		-0.5 to 6.0	V
Output current	I_O max		300	mA
Input signal voltage	V_{IN} max		-0.5 to V_{DD}+0.5	V
Allowable power dissipation	Pd	*Mounted on a specified board.	700	mW
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified board : 50mm×40mm×0.8mm, 4-layer glass epoxy circuit board.

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Allowable Operating Conditions at Ta = 25°C, GND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.5 to 3.3	V
Signal system supply voltage	V_{DD}		1.6 to 3.3	V
Input signal voltage	V_{IN}		0 to V_{DD}	V
Maximum operating frequency	Ct max		Set STP count × 512	Times

Electrical Characteristics at Ta = 25°C, V_{CC} = 2.8V, GND = 0V, unless otherwise specified.

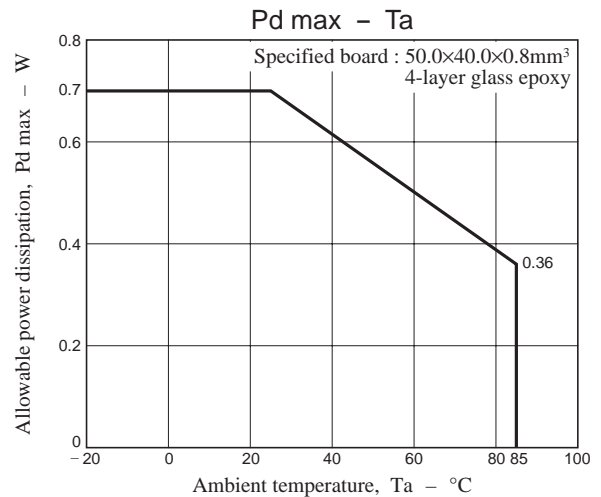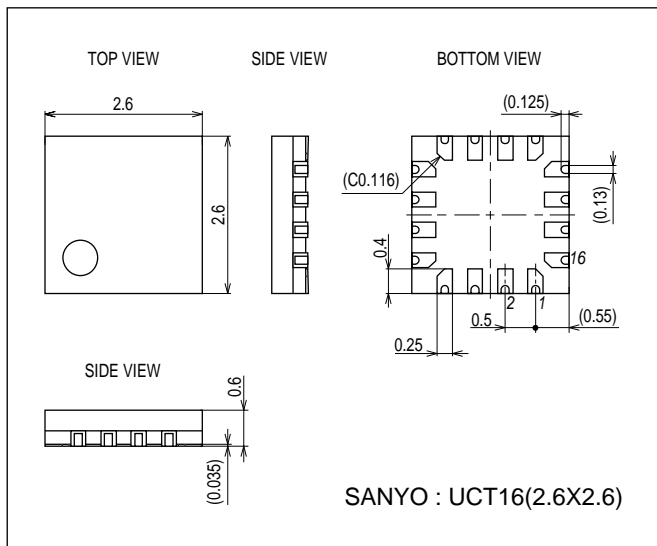| Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	$I_{CC}0$	No CLK input, When EN = L			1.0	μA
Operating mode current drain	$I_{CC}1$	CLK = 10MHz, When EN = H		0.7	1.5	mA
High-level input voltage	V_{IH}	1.6V ≤ V_{DD} ≤ 3.3V EN, SCL, SDA, RESET	0.8×V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}	1.6V ≤ V_{DD} ≤ 3.3V EN, SCL, SDA, RESET	0		0.2×V_{DD}	V
CLK, TEST pin high-level input voltage	$V_{IH}2$	CLK, TEST1/2	0.5×V_{CC}		V_{CC}	V
CLK, TEST pin low-level input voltage	$V_{IL}2$	CLK, TEST1/2	0		0.1×V_{DD}	V
Low voltage detection voltage	Vres	V_{CC} voltage	2.1	2.25	2.4	V
Thermal protection temperature	TSD	*1	150	180	210	°C
Output block upper-side on resistance	RonP			1.0	1.5	Ω
Output block lower-side on resistance	RonN			1.0	1.5	Ω
Turn on time	TPLH	With no load *2			0.2	μS
Turn off time	TPHL	With no load *2			0.2	μS

*1 : Design guaranteed value (no measurement is performed)

*2 : Rising time from 10 to 90% and falling time from 90 to 10% are specified with regard to the OUT pin voltage.
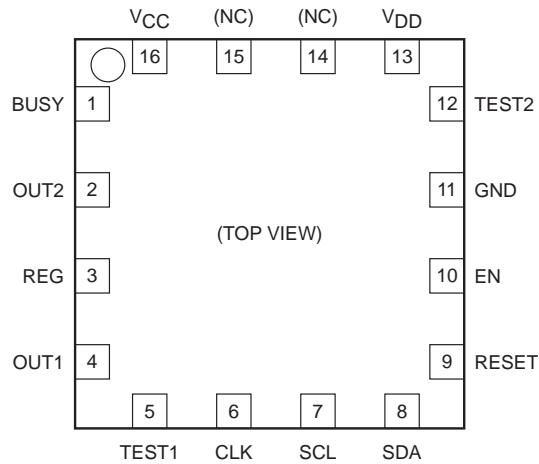
Package Dimensions

unit : mm (typ)

3341

SANYO : UCT16(2.6X2.6)

Pd max − Ta

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Pin Assignment

(TOP VIEW)

Pin	Label
16	V$_{CC}$
15	(NC)
14	(NC)
13	V$_{DD}$
1	BUSY
2	OUT2
3	REG
4	OUT1
12	TEST2
11	GND
10	EN
9	RESET
5	TEST1
6	CLK
7	SCL
8	SDA

Block Diagram
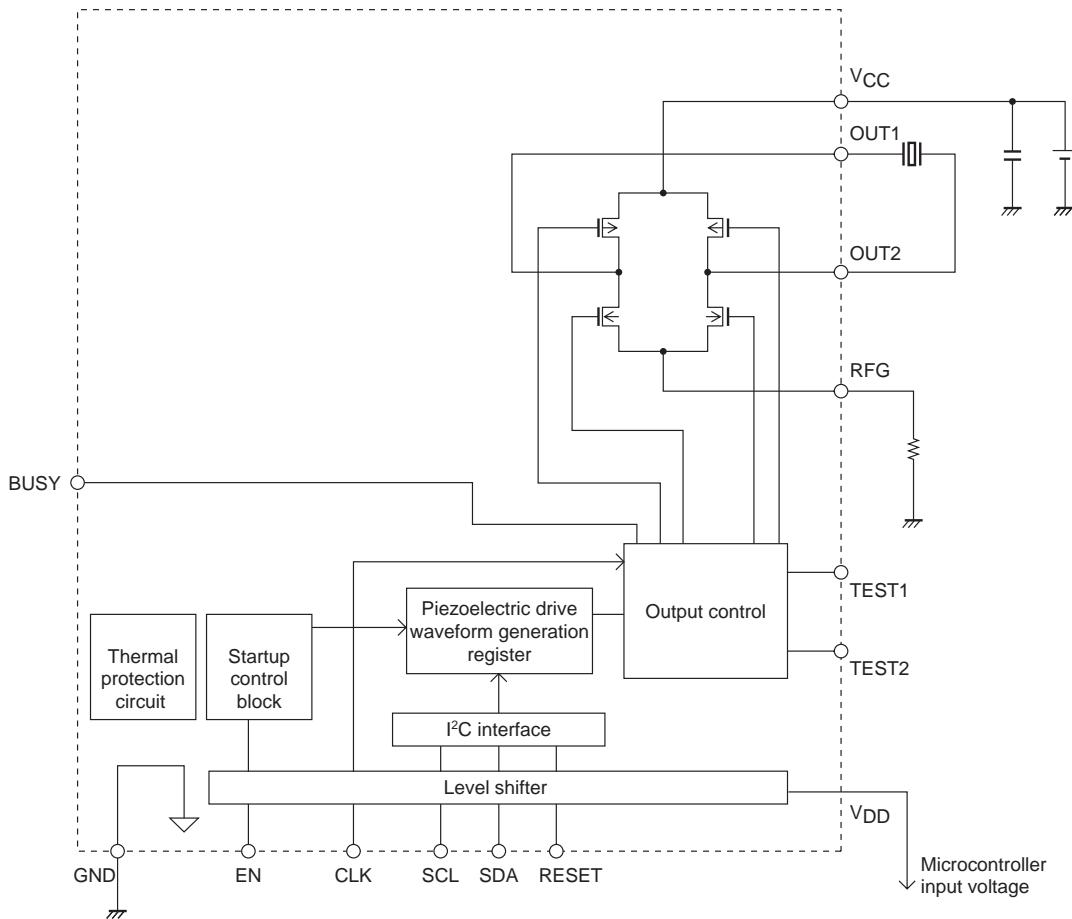
Value of the resistor connected to the RFG pin

    Inrush current flowing to the piezoelectric elements can be controlled in the LV8092GQ by inserting a resistor between the RFG pin and GND potential.

    Since the resistance affects the actuator operation, the constant must be determined in a range from 0 to 3.3Ω while monitoring the operation of the actuator.

Capacitor on the V$_{CC}$ line

    Piezoelectric actuators are capacitive loads in electrical terms, and they operate units by charging and discharging the charges. Since the charge between the capacitor on the V$_{CC}$ line and piezoelectric elements is transferred, the capacitor must be mounted near the V$_{CC}$ pin. The capacitance of the capacitor required is determined by the capacitance of the piezoelectric element. A capacitance within a range that does not affect operation must be selected.

LV8092GQ

高

Serial Bus Communication Specifications

I²C serial transfer timing conditions

Input waveform condition
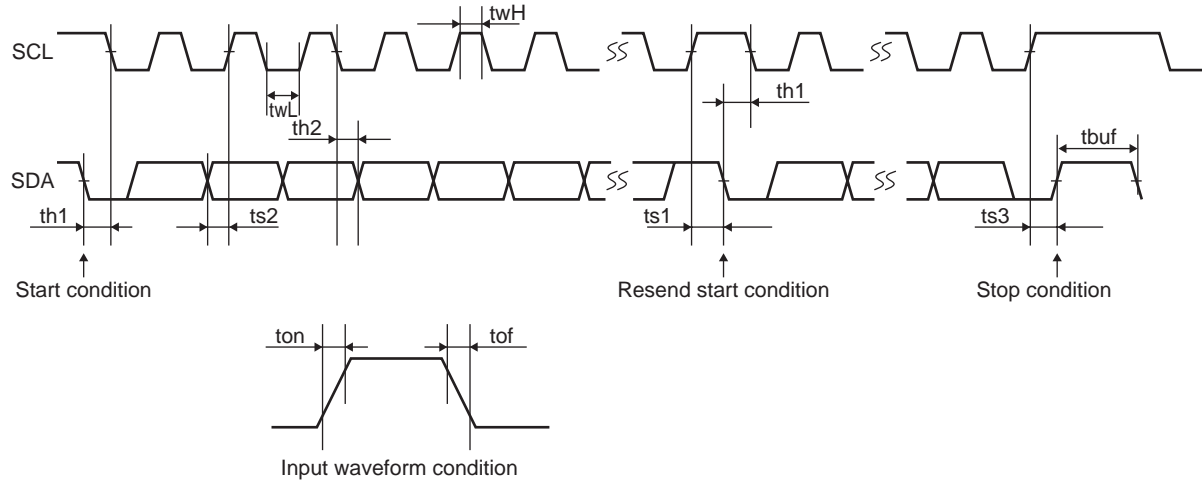
Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0	-	100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7	-	-	μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	250	-	-	ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0	-	-	μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	4.0	-	-	μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0	-	-	μs
Pulse width	twL	SCL low period pulse width	4.7	-	-	μs
	twH	SCL high period pulse width	4.0	-	-	μs
Input waveform conditions	ton	SCL/SDA (input) rising time	-	-	1000	ns
	tof	SCL/ SDA (input) falling time	-	-	300	ns
Bus free time	tbuf	Interval between stop condition and start condition	4.7	-	-	μs

High-speed mode

| Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	Clock frequency of SCL	0		400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	100			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6			μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	0.6			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			μs
Pulse width	twL	SCL low period pulse width	1.3			μs
	twH	SCL high period pulse width	0.6			μs
Input waveform conditions	ton	SCL/SDA (input) rise time			300	ns
	tof	SCL/SDA (input) fall time			300	ns
Bus free time	tbuf	Interval between the stop condition and the start condition	1.3			μs

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I²C bus transfer method

Start and stop conditions

The I²C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.
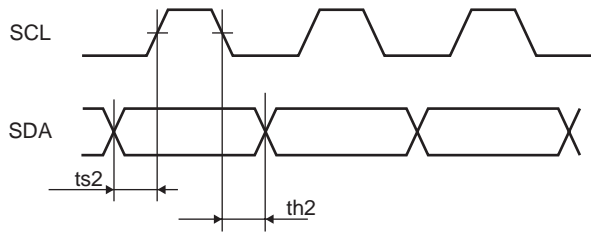
When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.

Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.
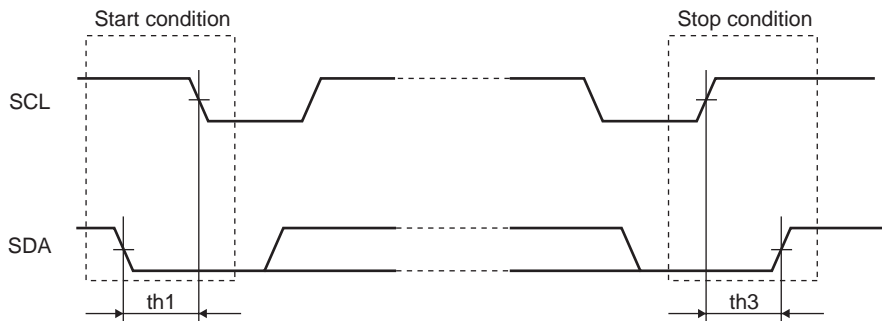
Data transfer and acknowledgement response

After the start condition is generated, data is transferred one byte (8 bits) at a time. Any number of data bytes can be transferred consecutively.

An ACK signal is sent to the sending side from the receiving side every time 8 bits of data are transferred. The transmission of an ACK signal is performed by setting the receiving side SDA to low after SDA at the sending side is released immediately after the clock pulse of SCL bit 8 in the data transferred has fallen low.

After the receiving side has sent the ACK signal, if the next byte transfer operation is to receive only the byte, the receiving side releases SDA on the falling edge of the 9th clock of SCL.

There are no CE signals in the I²C bus ; instead, a 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) which specifies the direction of subsequent data transfer.

The LB8092GQ is a drive IC with a dedicated write function and it does not have a read function.

The 7-bit address is transferred in sequence starting with MSB, and the eighth bit is set to low. The second and subsequent bytes are transferred in write mode.

In the LV8092GQ, the slave address is stipulated to be "1110010.".

LV8092GQ
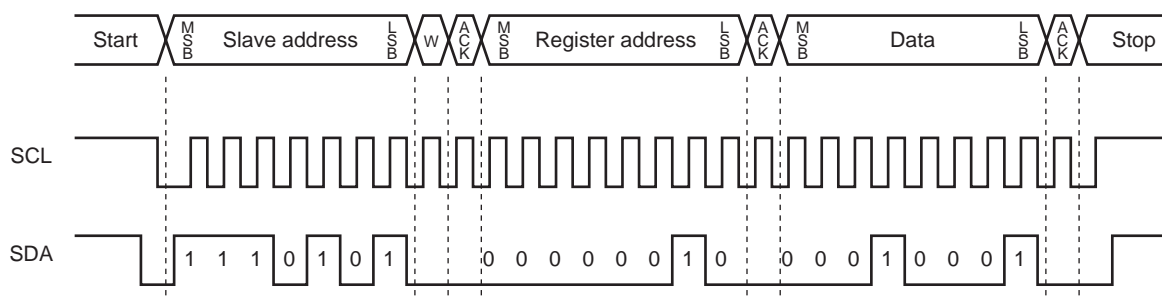
Serial Map

Register Address								Data							
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	M/I	DRVPULSE [6 : 0]						
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	GATE	×	×	CKSEL [1 : 0]		RET [1 : 0]		INIT
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	RST [7 : 0]							
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	GTAS [7 : 0]							
0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	GTBR [7 : 0]							
0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	1	GTBS [7 : 0]							
0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	0	STP [7 : 0]							
0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	1	×	×	×	×	INITMOV [7 : 4]			
0	0	0	0	0	0	0	0

(Rows numbered 0–7 at left; Upper : Register name, Lower : Default value)

Upper : Register name   Lower : Default value

Serial Mode Settings

0	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

D0 to D6: DRVPULSE [6 : 0]

Operation count setting register. Specify a number from 0 to 127.

The number of cyclic operations determined by <DRVPLUSE setting> × <STP setting> are performed.

Additional data can be input and data is added up to the equivalent of total of 512 pulses.

D7	M/I
0	∞
1	macro

Operation direction switching
*Default   Infinity distance direction
                         Macro direction

Operation direction switching register

The operation count setting register is reset when the register is switched. To stop the operation of the unit, switch the M/I register and set DRVPULSE to 0 for input. This register is also used to set the direction of operation when the initialization sequence is to be performed.

1	0	0	0	0	0	0	0	1	D7	0	0	D4	D3	D2	D1	D0

D0: Register for selecting whether the initialization sequence is to be performed when EN is set high.

D0	INIT
0	Initialization to be performed
1	Initialization not to be performed

Initialization to be performed/not to be performed setting
*Default

D0	D1	RET
0	0	2 times
0	1	1 time
1	0	3 times
1	1	4 times

Number of initialization sequence swing back
*Default

D4	D3	CKSEL
0	0	1/4
0	1	1/2
1	0	1
1	1	1

Input clock division ratio switching
*Default   1/4
                 1/2
                 1 (no frequency division)
                 1 (no frequency division)

D7	GATE
0	MODE1
1	MODE2

Gate mode operation
*Default   Forward/reverse/braking
                   Forward/reverse/standby

2	0	0	0	0	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0

RST7 to RST0 : Specifies the number of clocks per period (0 to 255). Default = 0
(Internally set to 115 when TEST = H and RESET = L.)

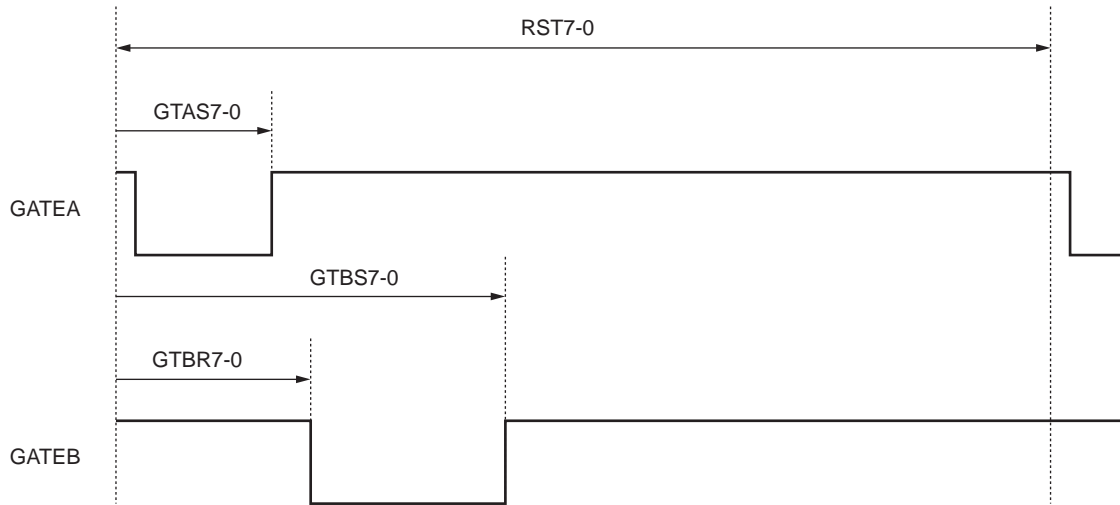| 3	0	0	0	0	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

GTAS7 to GTAS0 : Sets the GATE_A pulse set value (0 to 255). Default = 0
(Internally set to 21 when TEST = H and RESET = L.)

4	0	0	0	0	0	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0

GTBR7 to GTBR0 : Sets the GATE_B pulse reset value (0 to 255). Default = 0
(Internally set to 24 when TEST = H and RESET = L.)

| 5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

GTBS7 to GTBS0 : Sets the GATE_B pulse set value (0 to 255). Default = 0

(Internally set to 54 when TEST = H and RESET = L.)

| 6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

STP7 to STP0 : Specifies the number of output pulse steps with regard to DRIVE input (1 to 256). Default = 1

The setting value range is handled as the data value plus 1.

When data is input in 8-bit units (0 to 255), it is handled as an STP period of 1 to 256.

(Internally set to 139=140 periods when TEST = H and RESET = L.)

| 7 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | D3 | D2 | D1 | D0 |

INITMOV7 to INITMOV4 : Sets the number of swing back of the initialization sequence to be performed (16 to 256). Default = 16

(Internally set to 175 when TEST = H and RESET = L.)

D3	D2	D1	D0	INIT7 to 4	16 to 256
0	0	0	0	0	15
0	0	0	1	1	31
0	0	1	0	2	47
0	0	1	1	3	63
0	1	0	0	4	79
0	1	0	1	5	95
0	1	1	0	6	111
0	1	1	1	7	127
1	0	0	0	8	143
1	0	0	1	9	159
1	0	1	0	10	175
1	0	1	1	11	191
1	1	0	0	12	207
1	1	0	1	13	223
1	1	1	0	14	239
1	1	1	1	15	255

Functional Description

1 period :
One period of OUT waveform operation is equivalent to one output operation.
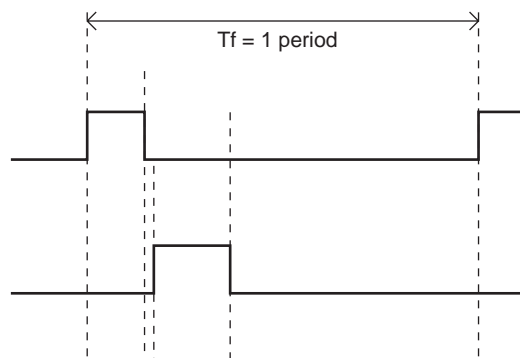
EN input :
A low-level EN input causes the IC to stop operation, placing the IC in the standby mode to save current consumption. A high-level EN input starts the IC. After performing the initialization sequence according to the predefined startup sequence, the IC starts operation due to DRVPULSE (when the initialization sequence is to be performed). The IC accepts I²C communication whether EN is high or low.

Initialization sequence (on or off and direction can be set by I²C) :
This is an internal sequence in which the actuator is moved to the initial position when the IC is started up. Setting EN from low to high initiates this initialization sequence.
The presence or absence of the initialization operation can be set using the initialization mode select register (INIT). If the initialization operation is specified, the direction of the initialization sequence can be set using the M/I register.
- M/I register = 0 : Initialization processing in infinity direction
  The IC performs the number of operations determined by STP setting period × INIT setting times in the infinite direction, then waits for the period equivalent to STP setting period × 4 times, and performs the number of swing back operations equal to STP setting period × RET setting times in the macro direction.
- M/I register = 1 : Auto macro operation in macro direction
  The IC performs the number of operations determined by STP setting period × INIT setting times in the macro direction, then waits for the period equivalent to STP setting periods × 4, and performs the number of swing back operations equal to STP period setting period × RET setting times in the infinity direction.

RESET input :
The input pin to reset the internal registers. When it is low, the counter is reset. When it is high the reset state is released. The reset input needs to be held high when I²C communication is in progress.

TEST1 pin :
This is a setting pin used when the IC is tested. It must be short-circuited to ground when the IC is used in a real application. When this pin is set high, a test counter value is loaded into the internal register, and it can no longer be set in I²C communication.

TEST2 pin :
This is a setting pin used when the IC is tested. It must be short-circuited to ground when the IC is used in a real application. When this pin is set high, the IC is ready for continuous output operation and continues operation in the infinity direction.

BUSY output :
This is an output signal pin that is held high (H = V_{DD} voltage) while the actuator is in operation and set low when the actuator is stopped.

V_{DD} :
This is a power voltage pin for the input pins. It supplies power to the EN, SCL, SDA, and RESET pins. Each input pin is provided with an internal level shifter circuit, so that it is not affected by potential difference from the V_{CC} voltage (the CLK and TEST pins accept input with respect to the V_{CC} voltage level).
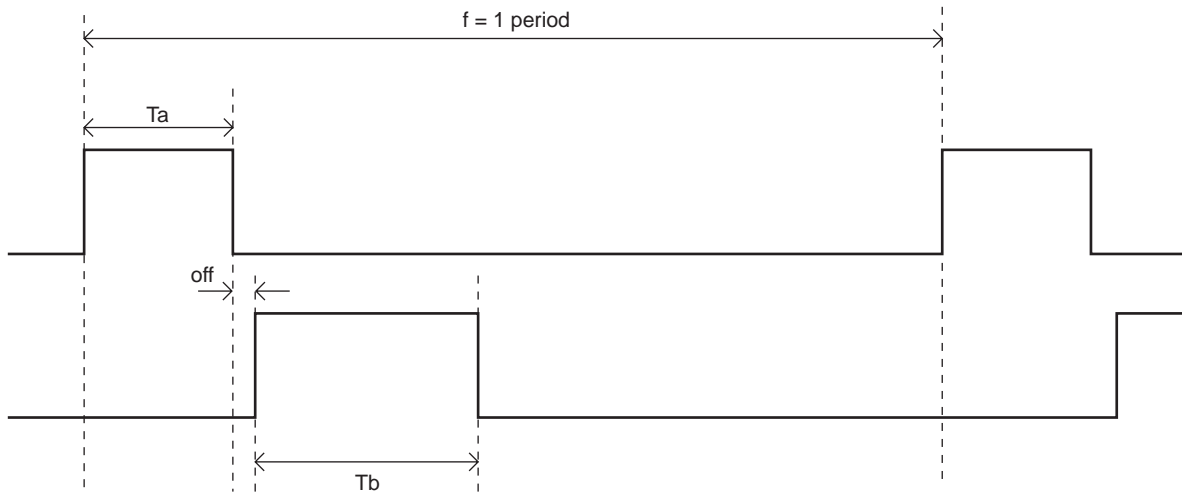
CLK input :
The pin for the external CLK input that provides the reference time for generating drive waveforms.
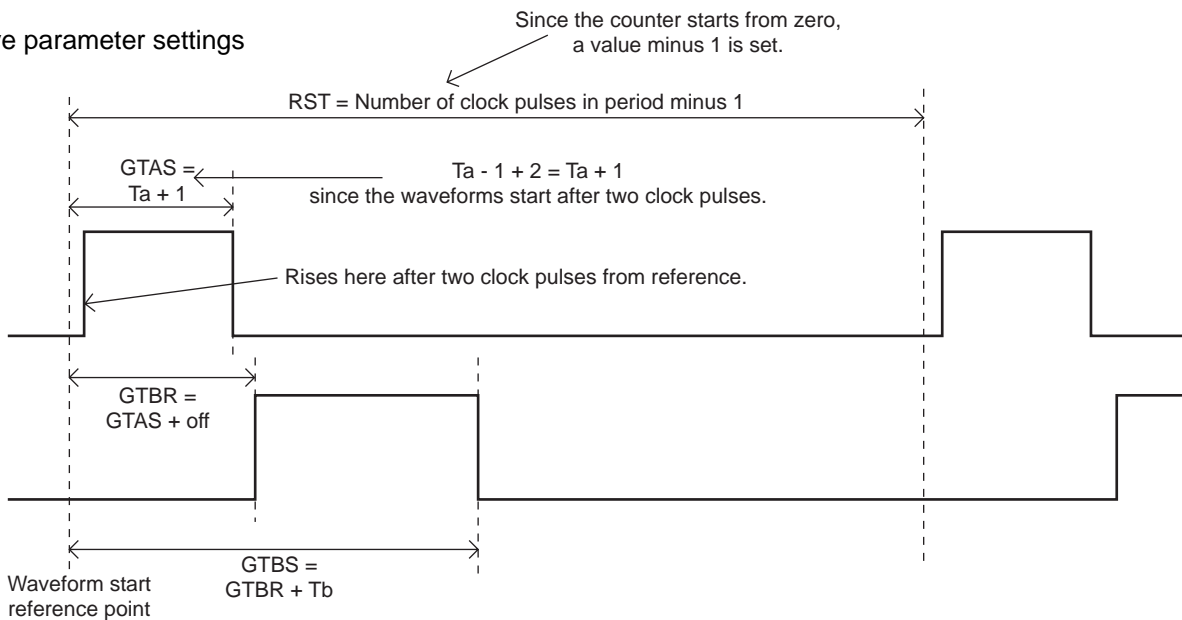The frequency division ratio for I²C communication can be selected from 1/4, 1/2, and 1/1. Drive waveforms are generated by counting this frequency-divided clk pulses as the basic count unit. The LV8092GQ supports frequency from 10MHz to 60MHz depending on the frequency division ratio and counter settings.

Actuator drive waveform settings :

Configuration of piezoelectric actuator drive waveform

f = 1 period

Ta

off

Tb

Drive parameter settings

Since the counter starts from zero,
a value minus 1 is set.

RST = Number of clock pulses in period minus 1

GTAS =
Ta + 1

Ta - 1 + 2 = Ta + 1
since the waveforms start after two clock pulses.

Rises here after two clock pulses from reference.

GTBR =
GTAS + off

GTBS =
GTBR + Tb

Waveform start
reference point

The drive waveforms are set using four parameters: RST, GTAS, GTBR and GTBS.

RST : Parameter determines the period, and sets the reference clock pulse count minus 1.

GTAS : Parameter determines the time taken for the gate signal A to the falling edge from the reference point.
Since the signal raises after two clock pulses from the reference, the Ta reference clock cycle count plus 1 is set.

GTBR : Parameter determines the time taken for the gate signal B to the rising edge from the reference point.
It sets the value obtained by adding the reference clock pulse count during the time from GTAS to "off."

GTBS : Parameter determines the time taken for the gate signal B to the falling ewdge from the reference point.
It sets the value obtained by adding the reference clock pulse count during the time from GTBR to "Tb."

[Example of settings] When setting reference clock to 10MHz, period to 13μs, Ta to 2.0μs, off to 0.3μs, and Tb to 3.0μs
Since the reference clock time is 0.1μs :

The period is 130 clks. → Specify 129 (RST value of 130 -1).
Ta is 20 clks. → Specify 21 (GTAS value of 20 + 1).
off is 3 clks. → Specify 24 (GTBR value of 21 + 3).
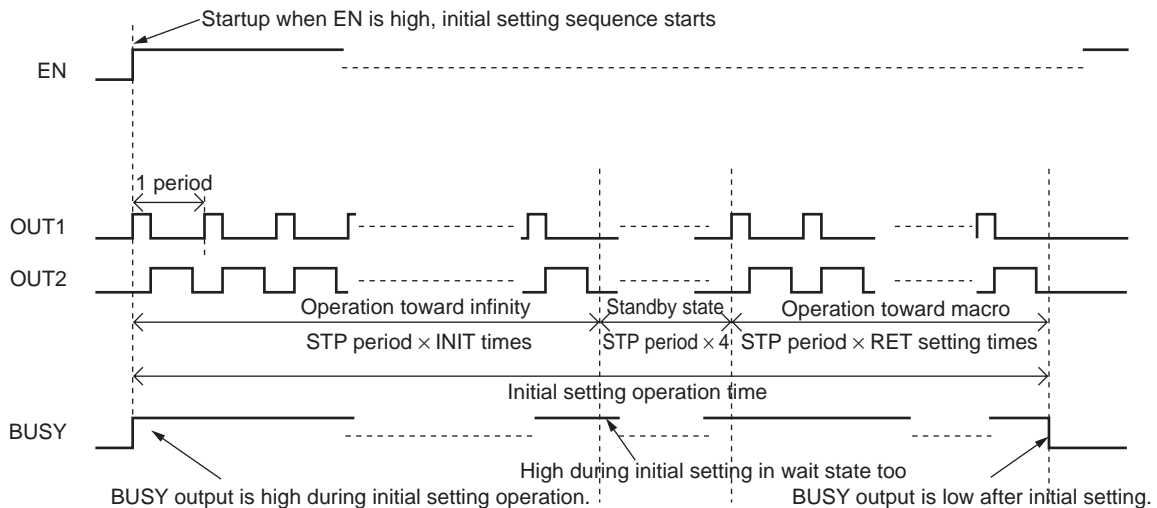Tb is 30 clks. → Specify 54 (GTBS value of 24 + 30).

Timing charts

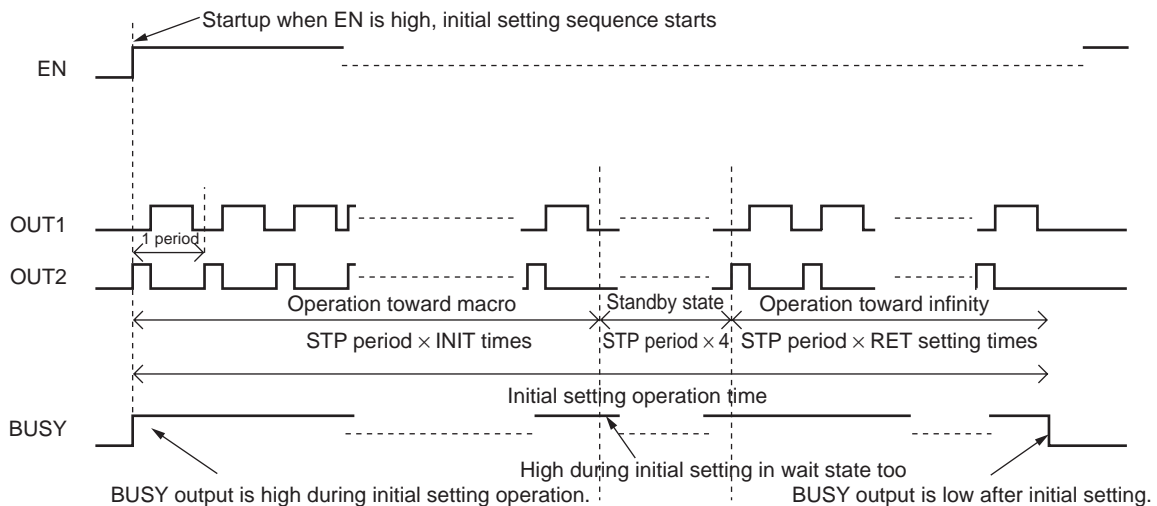Enlarged view of the sequence of output signals

Operation toward infinity

(RST setting + 1) × number of clock pulses
(GTAS setting - 1) × number of clock pulses
(GTAS setting - 1) × number of clock pulses

OUT1

(GTAS setting - 1) × number of clock pulses

OUT2

(GTBR setting -1) × number of clock pulses

Operation toward macro

(RST setting + 1) × number of clock pulses
(GTBR setting -1) × number of clock pulses

OUT1

(GTBS setting - 1) × number of clock pulses

OUT2

(GTAS setting - 1) × number of clock pulses
(GTAS setting - 1) × number of clock pulses

Sequence of initial setting operation ("on" or "off" can be set by the I²C settings.)
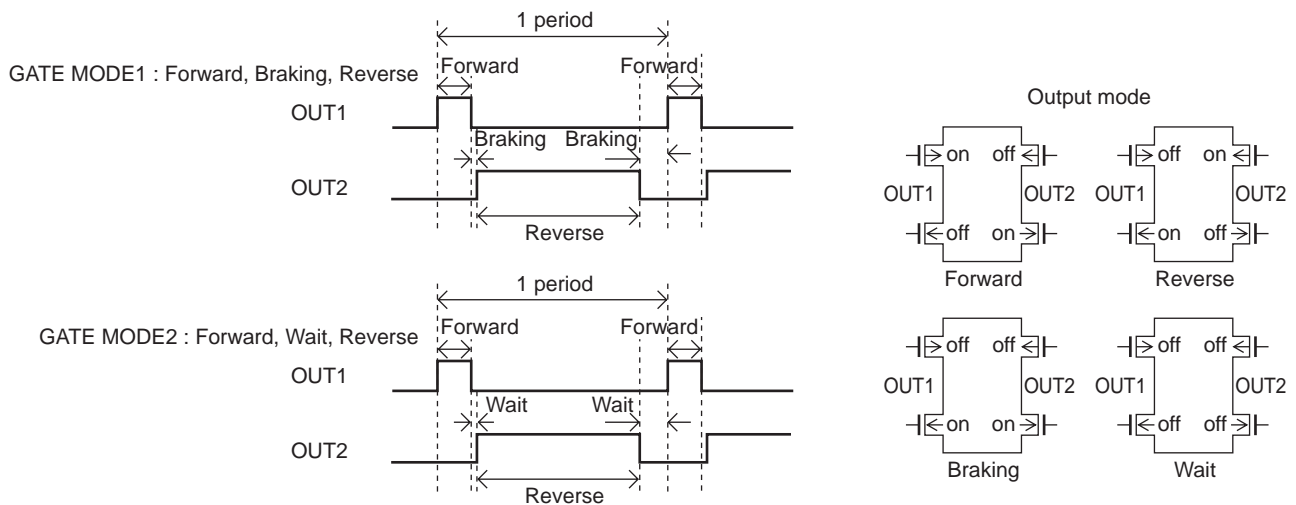When M/I register = 00 → Movement toward infinity position

Startup when EN is high, initial setting sequence starts

EN

1 period

OUT1

OUT2

Operation toward infinity

STP period × INIT times

Standby state

STP period × 4

Operation toward macro

STP period × RET setting times

Initial setting operation time

BUSY

BUSY output is high during initial setting operation.

High during initial setting in wait state too

BUSY output is low after initial setting.

When M/I register = 01 → Movement toward macro position

Startup when EN is high, initial setting sequence starts

EN

OUT1

1 period

OUT2

Operation toward macro

STP period × INIT times

Standby state

STP period × 4

Operation toward infinity

STP period × RET setting times

Initial setting operation time

BUSY

BUSY output is high during initial setting operation.

High during initial setting in wait state too

BUSY output is low after initial setting.

LV8092GQ

Sequence of operations triggered by DRVPULSE input

EN — Operation stops when EN input is low.

M/I register state — Infinity direction logic selection — Macro direction logic selection

DRVPULSE setting — I²C communication operation instruction completed 00000000_00000010 (operation 2 times toward infinity) — I²C communication operation instruction completed 00000000_10000010 (operation 2 times toward macro)

Equivalent to 2 pulses = STP setting period × operation for 2 times

1 period

OUT1 — Operation toward infinity (STP setting period × 2 times) — Operation toward macro

OUT2 — I²C communication Operation starts on completion of DRVPULSE input.

BUSY — Return to high when EN is set to low even before the completion of the operation.

BUSY output high, only during operation period

Gate setting output logic

GATE MODE1 : Forward, Braking, Reverse

1 period

Forward   Forward

OUT1

Braking   Braking

OUT2

Reverse

GATE MODE2 : Forward, Wait, Reverse

1 period

Forward   Forward

OUT1

Wait   Wait

OUT2

Reverse

Output mode

Forward

Reverse

Braking

Wait