Ordering number : ENA1515

SANYO Semiconductors
DATA SHEET

LV8098CS — Bi-CMOS IC For VCMs Constant-current Driver IC

Overview

The LV8098CS is a constant current driver IC for voice coil motors that supports I^2C control integrating a digital/analog converter (DAC). It uses an ultraminiature WLP package and includes a current detection resistor for constant current control, which makes the IC ideal for miniaturization of camera modules intended for use in camera-equipped mobile phones. The output transistor has a low on-resistance of 1Ω and the resistance of the built-in current detection resistor is 1Ω, which minimizes the voltage loss and helps withstand voltage drop in V_{CC}. The current consumption when the DAC is set to code 0 is 0 ($I_{CC} \approx 0$, $I_{OUT} \approx 0$) allowing reduction in current consumption.

Functions

- Constant current driver for voice coil motors.
- I^2C bus control supported.
- The current consumption is 0 when the DAC is set to code 0.
- Built-in thermal protection circuit.
- Built-in voltage drop protection circuit (V_{CC} = 2V output off).
- Low output block total-resistance of 2Ω helps withstand voltage drop in V_{CC}. (Current detection resistance + output transistor on-resistance).
- Built-in current detection resistor.
- Constant current control enabled by DAC (8 bits).
- Wide operating voltage range (2.2 to 5.0V).
- 6-pin WLP package used (1.27 × 0.87 × 0.5mm).

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		5.5	V
Output voltage	V_{OUT} max		V_{CC} + 0.5	V
Input voltage	V_{IN} max	SCL, SDA, ENA	5.5	V
Allowable power dissipation	Pd max	With specified substrate *	350	mW
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-40 to +150	°C

* Specified substrate : 40mm × 40mm × 1.6mm, Single layer glass epoxy substrate

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.2 to 5.0	V
Maximum preset output current	I_O		100	mA
High-level input voltage	V_{IH}	Applied to SCL, SDA, and ENA pins	1.3 to V_{CC}	V
Low-level input voltage	V_{IL}		-0.3 to 0.5	V

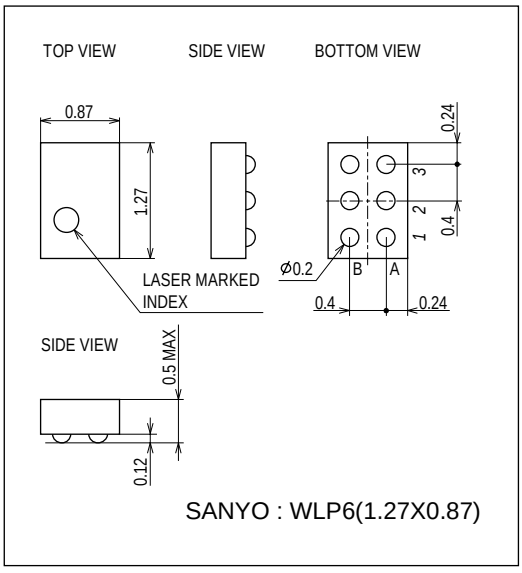
Electrical Characteristics at Ta = 25°C, V_{CC} = 2.8V

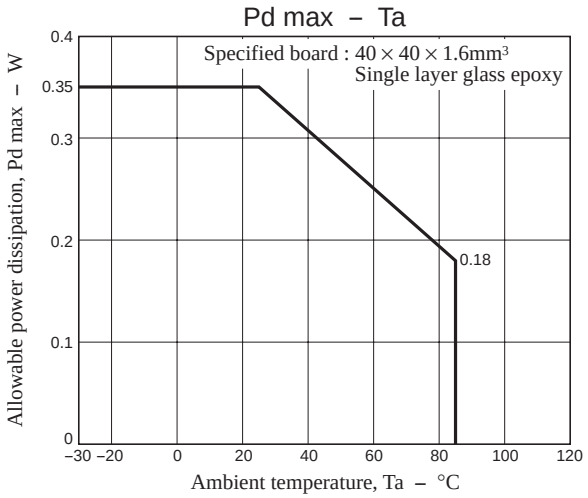
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I_{CCO}a	ENA = L			1	μA
	I_{CCO}b	ENA = H, PD = 1			1	μA
	I_{CCO}c	ENA = H, D0 to D7 = 0			1	μA
	I_{CC}1	ENA = H, D0 to D7 ≠ 0		0.5	3	mA
Input current	I_{IN}	SCL, SDA, ENA	-1	0	1	μA
Total resistance value of the output block (built-in resistor + transistor on-resistance)	RTTL	V_{CC} = 2.8V, I_{OUT} = 80mA		2	3	Ω
DAC block						
Resolution				8		bits
Relative accuracy	INL				±1	LSB
Differential linearity	DNL				±1	LSB
Full code current	Ifull	D0 to D7 = 1		100		mA
Error code current 0	Izero	D0 to D7 = 0			1	μA
Spark killer diode						
Reverse current	IS (leak)				1	μA
Forward voltage	VSF				1.3	V

Package Dimensions

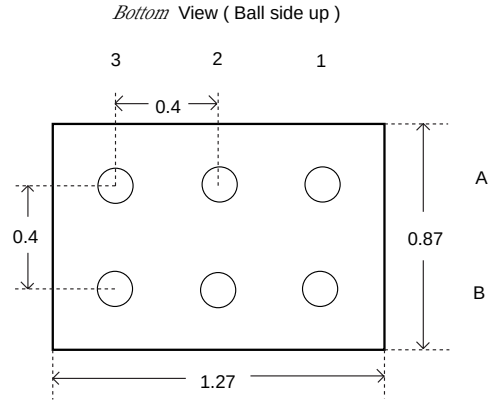
unit : mm (typ)

3380





Pin Assignment

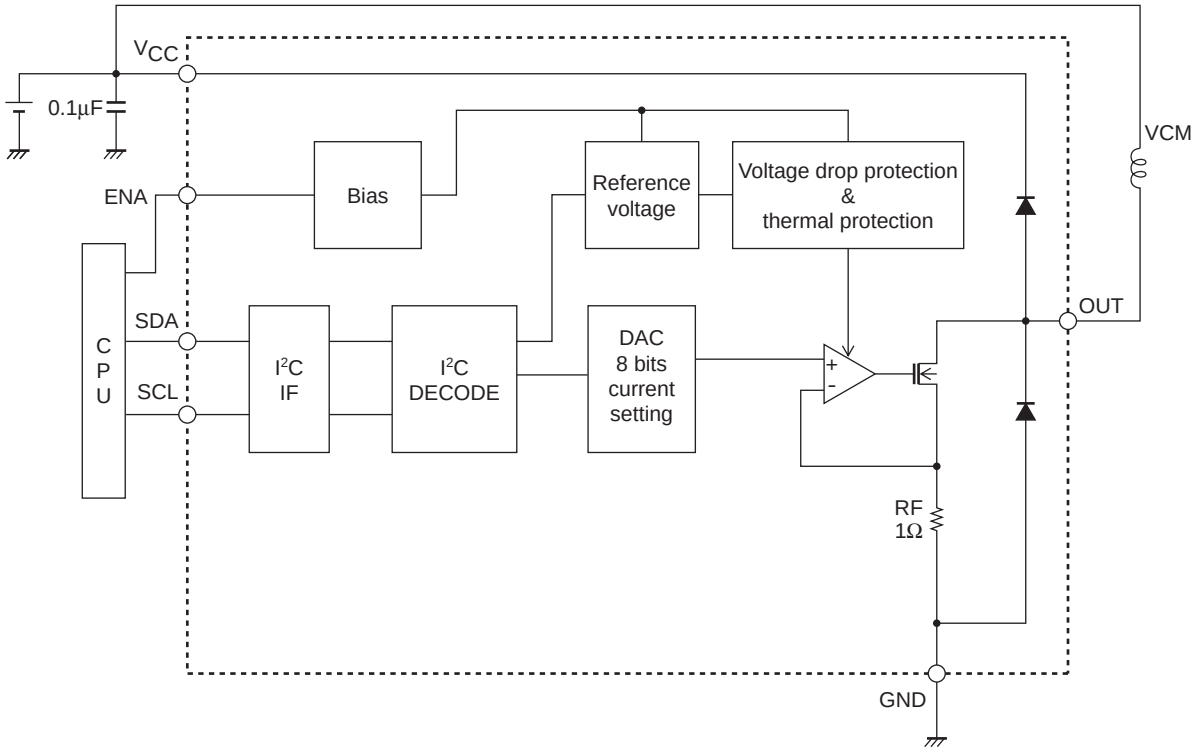


Pin No.	Pin Name	Pin Description
A1	SCL	I^2C SCL input pin
A2	ENA	Enable & reset *1, 2
A3	GND	Ground
B1	SDA	I^2C SDA input pin
B2	V_{CC}	Power supply pin
B3	OUT	Output pin

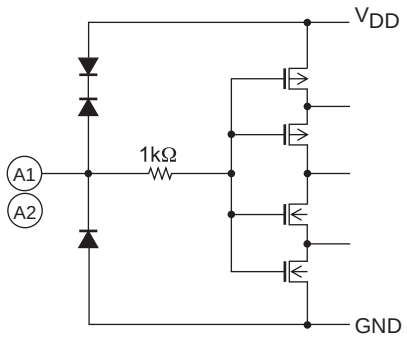
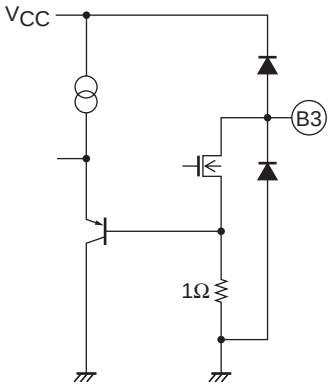
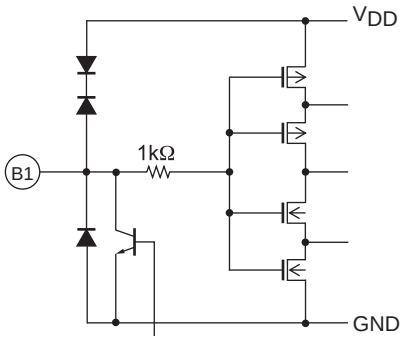
*1 : Setting the ENA pin to low powers down and resets the IC. It is necessary to power on the IC by setting the ENA pin to low and hold it high during normal operation.

*2 : When the ENA pin is to be used with pull_up, it is necessary to send code 0 in advance after power-on.

Block Diagram



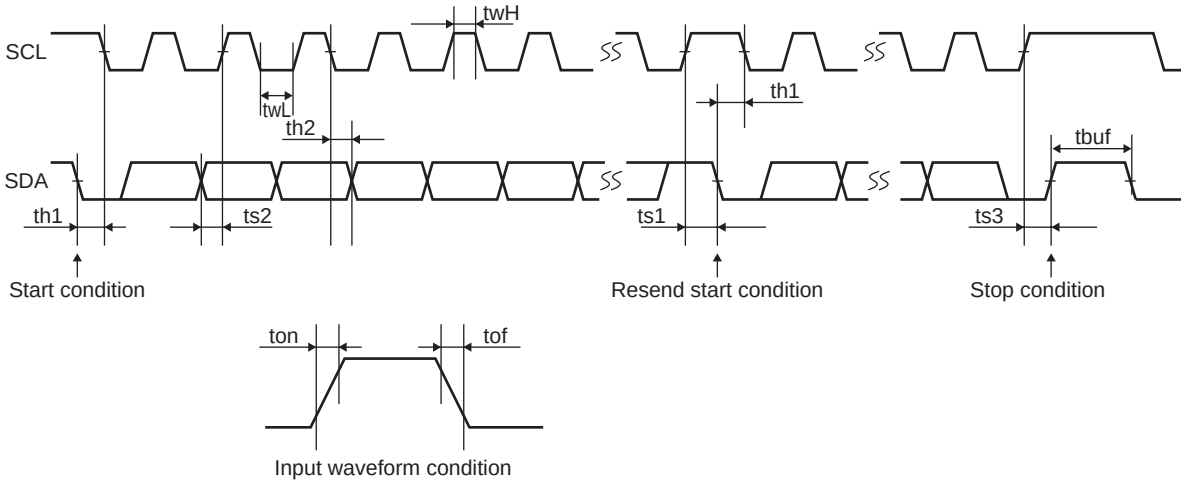
Pin Description

Pin No.	Pin name	Description	Equivalent circuit
A1 A2	SCL ENA	SCL I^2C serial clock input pin ENABLE When low, standby mode and reset is performed at the same time. This pin is held high for normal use. Input high level : 1.3V to 5.0V Input low level : -0.3V to 0.5V	
A3	GND	Ground pin.	
B3	OUT	OUT Output pin This is an NMOS open drain output, and the voice coil motor is connected between this pin and the V_{CC} pin for use.	
B2	V_{CC}	V_{CC} Power supply input pin	
B1	SDA	SDA I^2C serial data input pin Input high level : 1.3V to 5.0V Input low level : -0.3V to 0.5V	

Serial Bus Communication Specifications

I^2C serial transfer timing conditions

Standard mode



Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	250			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0			μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	4.0			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			μs
Pulse width	twL	SCL low period pulse width	4.7			μs
	twH	SCL high period pulse width	4.0			μs
Input waveform conditions	ton	SCL, SDA (input) rising time			1000	ns
	tof	SCL, SDA (input) falling time			300	ns
Bus free time	tbuf	Interval between stop condition and start condition	4.7			μs

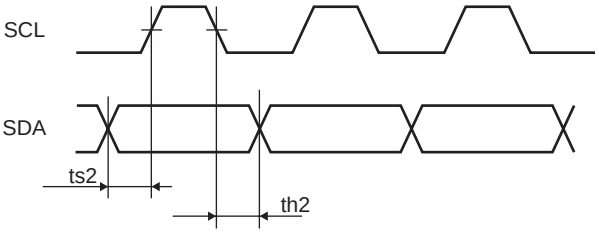
High-speed mode

Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	100			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6			μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	0.6			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			μs
Pulse width	twL	SCL low period pulse width	1.3			μs
	twH	SCL high period pulse width	0.6			μs
Input waveform conditions	ton	SCL, SDA (input) rising time			300	ns
	tof	SCL, SDA (input) falling time			300	ns
Bus free time	tbuf	Interval between stop condition and start condition	1.3			μs

I^{2}C bus transmission method

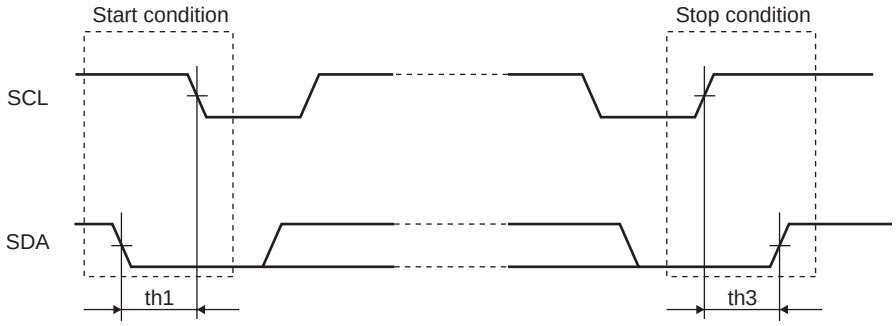
Start and stop conditions

The I^{2}C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.



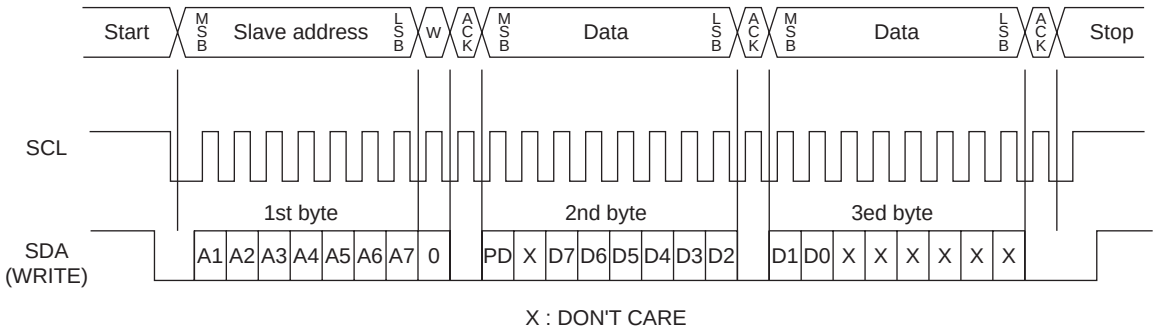
When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.

Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.



Data transfer and acknowledgement response

After the start condition has been generated, the data is transferred one byte (8 bits) at a time. Generally, in an I^{2}C bus, a unique 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) indicating the transfer direction of the subsequent data. However, this IC is provided with only a write mode for receiving the data. Every time 8 bits of data for each byte are transferred, the ACK signal is sent from the receiving end to the sending end. Immediately after the clock pulse of SCL bit 8 in the data transferred has fallen to low, SDA at the sending end is released, and SDA is set to low at the receiving end, causing the ACK signal to be sent. When, after the receiving end has sent the ACK signal, the transfer of the next byte remains in the receiving status, the receiving end releases SDA at the falling edge of the ninth SCL clock.



X : DON'T CARE

The standard data transfer to this device consists of three bytes : the slave address of the first byte and the data of the second and third bytes.

Slave address : 0110011(0)
PD : Power-down
D1-D7 : 8-bit data used to set output constant current ; MIN = 00000000, MAX = 11111111
The table below shows the format of the second and third bytes.

	2nd byte								3rd byte							
Serial data bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Function	PD	×	D7	D6	D5	D4	D3	D2	D1	D0	×	×	×	×	×	×

PD bit setting method PD = 1 → Power_down (standby mode) and reset

D0-D7 setting method

Current setting code	D7	D6	D5	D4	D3	D2	D1	Output setting (LSB)	Output current (mA) (design value)
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	0.392
2	0	0	0	0	0	1	0	2	0.784
254	1	1	1	1	1	1	0	254	99.608
255	1	1	1	1	1	1	1	255	100

Relationship between the ENA pin input, I^2C input data PD, and current setting 0 (code 0)

This IC supports the following three modes of setting up the standby mode :
1) Setting the ENA pin low.
2) Setting the PD bit to 1 (high) with I^2C input data.
3) Setting the output current to 0 with I^2C input data.

Execution of one of the steps 1) to 3) causes the output current to 0 and stops operation of the circuit.
When the ENA pin is set low, the I^2C data register is reset and the IC is reset to its default state (PD bit set to 0 and output current setting to code 0).
Since the IC starts operation in the data reset state at power-on time, it is necessary to start using the IC in the default state by setting the ENA pin low before turning on V_{CC} and then high after V_{CC} is established.

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