

SANYO Semiconductors DATA SHEET



Bi-CMOS IC LV8111V — For Polygon Mirror Motor **3-phase Brushless Motor Driver**

Overview

The LV8111V is a 3-phase brushless motor driver for polygon mirror motor driving of LBP. A circuit needed to drive of polygon mirror motor can be composed of a single-chip. Also, the output transistor is made DMOS by using BiDC process, and by adopting the synchronous rectification method, the lower power consumption (Heat generation) is achieved.

Features

- 3-phase bipolar drive
- Direct PWM drive + synchronous rectification
- IO max1 = 2.5A
- IO max1 = 3.0A (t ≤ 0.1 ms)
- Output current control circuit
- PLL speed control circuit
- Phase lock detection output (with mask function) Forward / Reverse switching circuit
- Compatible with Hall FG
- Provides a 5V regulator output

- Full complement of on-chip protection circuits, including lock protection, current limiter, under-voltage protection, and thermal shutdown protection circuits
- Circuit to switch slowing down method while stopped (Free run or Short-circuit brake)
- Constraint protection detection signal switching circuit (FG or LD)
- Hall bias pin (Bias current cut in a stopped state)
- SDCC (Speed Detection Current Control) function

Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC} max	V _{CC} pin	37	V
	VG max	VG pin	42	V
Output current	IO max1	*1	2.5	А
	I _O max2	t ≤ 0.1ms *1	3.0	А
Allowable Power dissipation	Pd max	Mounted on a specified board *2	1.7	W
Operation temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C
Junction temperature	Tj max		150	°C

*1. Tj max = 150°C must not be exceeded.

*2. Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

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Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	VCC		10 to 35	V
5V constant voltage output current	IREG		0 to -30	mA
LD pin applied voltage	V _{LD}		0 to 5	V
LD pin output current	I _{LD}		0 to 15	mA
FG pin applied voltage	V _{FG}		0 to 5	V
FG pin output current	I _{FG}		0 to 10	mA
HB pin applied voltage	V _{HB}		0 to 5	V
HB pin output current	I _{HB}		0 to -30	mA

Electrical Characteristics at $Ta = 25^{\circ}C$, $V_{CC} = 24V$

Parameter	Symbol	Conditions		Ratings	r	Unit
	Gymbol		min	typ	max	Onic
Current drain	I _{CC} 1			5.5	6.5	mA
	I _{CC} 2	In a stop state		1.0	1.5	mA
5V Constant Voltage Output						-
Output voltage	VREG		4.65	5.0	5.35	V
Line regulation	$\Delta VREG1$	V _{CC} = 10 to 35V		20	100	mV
Load regulation	$\Delta VREG2$	I _O = -5 to -20mA		25	60	mV
Temperature coefficient	∆VREG3	Design target value *		0		mV/°
Output Block						
Output ON resistance	R _{ON}	I_{O} = 1A , Sum of the lower and upper side outputs		1.5	1.9	Ω
Output leakage current	l _O leak	Design target value *			100	μA
Lower side Diode forward voltage	V _D 1	I _D = -1A		1.0	1.35	V
Upper side Diode forward voltage	V _D 2	I _D = 1A		1.0	1.35	V
Charge Pump Output (VG pin)						
Output voltage	VG _{OUT}			V _{CC} +4.9		V
CP1 pin	•				•	
Output ON resistance (High level)	V _{OH} (CP1)	I _{CP1} = -2mA		500	700	Ω
Output ON resistance (Low level)	V _{OL} (CP1)	I _{CP1} = 2mA		300	400	Ω
Hall Amplifier Block	1					
Input bias current	I _{HB} (HA)		-2	-0.5		μA
Common mode input voltage range	VICM		0.5		VREG-2.0	V
Hall input sensitivity			80			mVp-
Hysteresis	∆V _{IN} (HA)		15	24	42	mV
Input voltage $L \rightarrow H$	V _{SLH}			12		mV
Input voltage $H \rightarrow L$	V _{SHL}			-12		mV
Hall Bias (HB pin) P-channel Output	•				•	
Output voltage ON resistance	V _{OL} (HB)	I _{HB} = -20mA		20	30	Ω
Output leakage current	IL(HB)	V _O = 0V			10	μA
FG Amplifier Schmitt Block (IN1)	•				•	
Input amplifier gain	G _{FG}	Design target value *		5		times
Input hysteresis (H \rightarrow L)	V _{SHL} (FGS)	Input referred, Design target value *		0		mV
Input hysteresis (L \rightarrow H)	V _{SLH} (FGS)	Input referred, Design target value *		10		mV
hysteresis	VFGL	Input referred, Design target value *		10		mV
FGFIL pin						
High level output voltage	V _{OH} (FGFIL)		2.7	3.0	3.3	V
Low level output voltage	V _{OL} (FGFIL)		0.75	0.85	0.95	V
External capacitor charge current	ICHG ¹	V _{CHG} 1 = 1.5V	-5	-4	-3	μA
External capacitor discharge current	I _{CHG²}	V _{CHG} 2 = 1.5V	3	4	5	μA
Amplitude	V(FGFIL)	0.10	1.95	2.15	2.35	Vp-p

* Design target value, Do not measurement.

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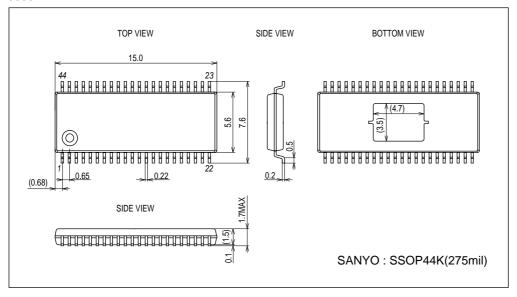
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Parameter	Symbol	Conditions		Ratings		Unit
FG Output			min	typ	max	
Output ON resistance	V _{OL} (FG)	I _{FG} = 7mA		20	30	Ω
Output leakage current	II (FG)	$V_{O} = 5V$		20	10	μA
PWM Oscillator	12(1 0)	0-30			10	μΛ
High level output voltage	V _{OH} (PWM)		2.95	3.2	3.45	V
Low level output voltage	V _{OL} (PWM)		1.3	1.5	1.7	V
External capacitor charge current	I _{CHG} (PWM)	V _{PWM} = 2V	-90	-70	-50	μA
Oscillation frequency	f(PWM)	C = 150pF	180	225	270	kHz
Amplitude	V(PWM)		1.5	1.7	1.9	Vp-p
Recommended operation frequency			1.5	1.7	300	kHz
range	[†] OPR		15		500	KI IZ
CSD Oscillation Circuit						
High level output voltage	V _{OH} (CSD)		2.7	3.0	3.3	V
Low level output voltage	V _{OL} (CSD)		0.8	1.0	1.2	V
Amplitude	V(CSD)		1.75	2.0	2.25	Vр-р
External capacitor charge current	I _{CHG} 1(CSD)	V _{CHG} 1 = 2.0V	-14	-10	-6	μA
External Capacitor Discharge Current	I _{CHG} 2(CSD)		8	11	14	μA
Oscillation frequency	f(CSD)	C = 0.068µF, Design target value *	30	40	50	Hz
Phase comparing output	·					
Output ON resistance (high level)	V _{PDH}	I _{OH} = -100μA		500	700	Ω
Output ON resistance (low level)	V _{PDL}	I _{OL} = 100μA		500	700	Ω
Phase Lock Detection Output						
Output ON resistance	V _{OL} (LD)	I _{LD} = 10mA		20	30	Ω
Output leakage current	I _I (LD)	$V_{O} = 5V$			10	μA
Error Amplifier Block	L	•				
Input offset voltage	V _{IO} (ER)	Design target value *	-10		+10	mV
Input bias current	I _B (ER)	5 5	-1		+1	μA
High level output voltage	V _{OH} (ER)	I _{OH} = -100μA	El+0.7	EI+0.85	El+1.0	V
Low level output voltage	V _{OL} (ER)	$I_{OL} = 100 \mu A$	EI-1.75	EI-1.6	EI-1.45	V
DC bias level	V _B (ER)		-5%	VREG/2	5%	V
Current Control Circuit	D()					
Drive gain	GDF	While phase locked	0.5	0.55	0.6	times
Current Limiter Circuit (pins RF and I						
Limiter voltage	V _{RF}		0.465	0.515	0.565	V
Under-voltage Protection	*KF		0.100	0.010	0.000	•
Operation voltage	VSD		8.3	8.7	9.1	V
Hyteresis			0.3	0.35	0.5	V
CLD Circuit			0.2	0.00	0.0	v
External capacitor charge current	I _{CLD}	$V_{CLD} = 0V$	-4.5	-3.0	-1.5	μA
Operation voltage	V _H (CLD)		3.25	3.5	3.75	μ Λ V
Thermal Shutdown Operation	· (, (, c, c, c))		0.20	5.5	0.10	v
Thermal shutdown operation	TSD	Design target value (Junction temperature)	150	175		°C.
temperature			100	175		0.
Hysteresis	∆TSD	Design target value (Junction temperature)		30		°C
CLK pin						
External input frequency	f _I (CLK)		0.1		10	kHz
High level input voltage	V _{IH} (CLK)		2.0		VREG	V
Low level input voltage	VIL(CLK)		0		1.0	V
Input open voltage	V _{IO} (CLK)		VREG-0.5		VREG	V
Hysteresis	V _{IS} (CLK)		0.2	0.3	0.4	V
High level input current	I _{IH} (CLK)	V _{CLK} = VREG	-10	0	+10	μA
Low level input current		V _{CLK} = 0V	-110	-85	-60	μΑ
Design target value, Do not measureme			110	00	00	μι

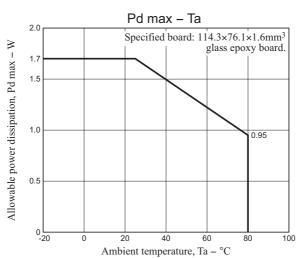
* Design target value, Do not measurement.

Deservation	Querra ha l			Ratings		1.1 14	
Parameter	Symbol	Conditions	min	typ	max	Unit	
CSDSEL pin							
High level input voltage	V _{IH} (CSD)		2.0		VREG	V	
Low level input voltage	V _{IL} (CSD)		0		1.0	V	
Input open voltage	V _{IO} (CSD)		VREG-0.5		VREG	V	
High level input current	I _{IH} (CSD)	V _{CSD} = VREG	-10	0	+10	μA	
Low level input current	I _{IL} (CSD)	$V_{CSD} = 0V$	-110	-85	-60	μΑ	
S/S pin							
High level input voltage	V _{IH} (SS)		2.0		VREG	V	
Low level input voltage	V _{IL} (SS)		0		1.0	V	
Input open voltage	V _{IO} (SS)		VREG-0.5		VREG	V	
Hysteresis	V _{IS} (SS)		0.2	0.3	0.4	V	
High level input current	I _{IH} (SS)	V _{S/S} = VREG	-10	0	+10	μA	
Low level input current	I _{IL} (SS)	V _{S/S} =0V	-110	-85	-60	μA	
BRSEL pin							
High level input voltage	V _{IH} (BRSEL)		2.0		VREG	V	
Low level input voltge	V _{IL} (BRSEL)		0		1.0	V	
Input open voltage	V _{IO} (BRSEL)		VREG-0.5		VREG	V	
High level input current	I _{IH} (BRSEL)	V _{BRSEL} = VREG	-10	0	+10	μA	
Low level input current	I _{IL} (BRSEL)	V _{BRSEL} = 0V	-110	-85	-60	μA	
F/R pin							
High level input voltage	V _{IH} (FR)		2.0		VREG	V	
Low level input voltage	V _{IL} (FR)		0		1.0	V	
Input open voltage	V _{IO} (FR)		VREG-0.5		VREG	V	
High level input current	I _{IH} (FR)	V _{F/R} = VREG	-10	0	+10	μΑ	
Low level input current	I _{IL} (FR)	$V_{F/R} = 0V$	-110	-85	-60	μA	

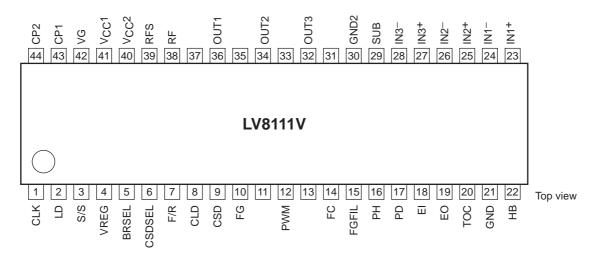
Package Dimensions

unit : mm (typ) 3333



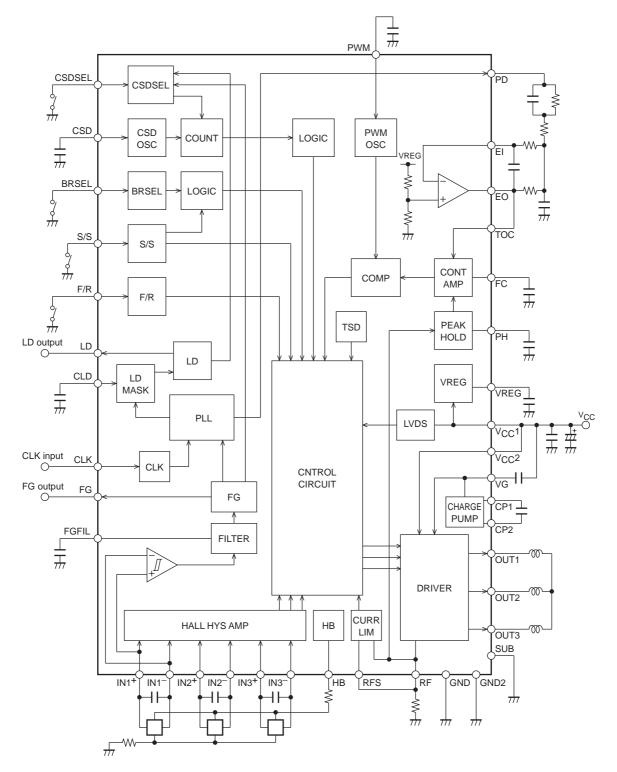


Pin Assignment



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Pin F	unctior	1	
Pin No.	Pin name	Function	Equivalent circuit
1	CLK	Clock input pin (10kHz maximum)	VREG
2	LD	Phase lock detection output pin. Goes ON during PLL-phase lock. Open drain output.	
3	S/S	Start/Stop input pin. START with a low-level input. STOP with a high-level input or open input	VREG 3 5kΩ 10kΩ 10kΩ 10kΩ 10kΩ 10kΩ 10kΩ 10kΩ 10kΩ 10kΩ
4	VREG	5V regulator output pin. (the control circuit power supply) Connect a capacitor between this pin and GND for stabilization.	
5	BRSEL	Brake selection pin. By low level, short-circuit braking when the S/S pin is in a stopped state. (Brake for the inspection process)	VREG 55kQ 55kQ 55kQ 55kQ 55kQ 55kQ 55kQ 55k
6	CSDSEL	Motor constraint protection detection signal selection pin. Select FG with low, and LD with high or in an open state.	VREG 55kΩ 55kΩ 55kΩ 56Ω 55kΩ 66 777

Continu	ed from pro	eceding page.	
Pin No.	Pin name	Function	Equivalent circuit
7	F/R	Pin to select Forward / Reverse. (Pin to select SDCC function)	VREG 55kΩ 5 55kΩ 7 77 77 77 77 77
8	CLD	Pin to set phase lock signal mask time. Connect a capacitor between this pin and GND. If there is no need for masking, this pin must be left open.	VREG 500Ω 500Ω 8 2kΩ 1 1 1 1 1 1 1 1 1 1 1 1 1
9	CSD	Pin for both the constraint protection circuit operation time and the initial reset pulse setting. Connect a capacitor between this pin and GND. If the motor constraint protection circuit is not used, a capacitor and a resistor must be connected in parallel between the CSD pin and GND.	
10	FG	FG Schmitt output pin. Open drain output.	
12	PWM	Pin to set the oscillation frequency of PWM. Connect a capacitor between this pin and GND.	VREG 2000 2000 12 12 12 177 777 777 777
14	FC	Frequency characteristics correction pin of the current limiter circuit. Connect a capacitor between this pin and GND.	VREG VREG () () () () () () () () () ()

Pin No.			
	Pin name	Function	Equivalent circuit
15	FGFIL	FG filter pin. When the noise of the FG signal is a problem, connect a capacitor between this pin and GND for stabilization.	VREG
16	PH	Pin to stabilize the RF waveform. Connect a capacitor between this pin and GND.	VREG
17	PD	Phase comparison output pin. The phase error is output by the duty changing of the pulse.	VREG 500Ω 17 17 777 777
18	EI	Error amplifier input pin.	VREG
19	EO	Error amplifier output pin.	VREG (19) 100kΩ 100kΩ 100kΩ
20	TOC	Torque command voltage input pin. Normally, this pin must be connected with the EO pin.	VREG 50002 200 117 117 117 117 117 117 117 1
21	GND	Ground pin of the control circuit block.	Continued on next page.

Continu	ed from pro	eceding page.			
Pin No.	Pin name	Function	Equivalent circuit		
22	НВ	Hall element bias current pin. Goes ON when the S/S pin is in a start state. Goes OFF when the S/S pin is in an stopped state.			
23 24 25 26 27 28	IN1+ IN1- IN2+ IN2- IN3+ IN3-	Hall amplifier input pin. A high level state of logic is recognized when IN ⁺ > IN ⁻ . In reverse case is a low-level state. The input amplitude of 100mVp-p or more (differential) is desirable in the Hall sensor inputs. If noise on the Hall inputs is a problem, that noise must be excluded by inserting capacitors across the inputs.	24/26/28 777 777 777 777 777 777 777 777 777 7		
29	SUB	Frame ground pin. This pin is connected with the GND2 pin.			
30	GND2	Ground pin of the output circuit block.			
32 34 36	OUT3 OUT2 OUT1	Output pin. As for PWM, Duty control is executed on the upper- side FET.			
38	RF	Source pin of output MOSFET (lower-side). Connect a low resistance (Rf) between this pin and GND.	38		
39	RFS	Output current detection pin. Connect to RF pin.	39 5KQ THEG 39 THEG THEG THE THE THE THE THE THE THE THE THE THE		
40	V _{CC} 2	Power supply pin. Connect a capacitor between this pin and GND for stabilization.			
41	V _{CC} 1	Power supply pin for control.			
42	VG	Charge pump output pin (Power supply for the upper side FET gate). Connect a capacitor between this pin and $V_{\mbox{CC}}$.			
43 44	CP1 CP2	Pin to connect a capacitor for charge pump. Connect a capacitor between CP1 and CP2.			

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3-phase Logic Truth Table	$(IN = "H" indicates the state where in IN^+ > IN^-)$
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	F/R = H			F/R = L			Output	
IN1	IN2	IN3	IN1	IN2	IN3	OUT1	OUT2	OUT3
Н	L	Н	L	Н	L	L	Н	М
Н	L	L	L	Н	Н	L	М	Н
Н	н	L	L	L	Н	М	L	Н
L	Н	L	Н	L	н	Н	L	М
L	Н	Н	Н	L	L	Н	М	L
L	L	Н	Н	Н	L	М	Н	L

S/S Pin

Input state	Mode
High or Open	Stop
Low	Start

CSDSEL Pin

Input state	Mode
High or Open	LD standard
Low	FG standard

BRSEL Pin

Input state	While stopped
High or Open	Free run
Low	Short-circuit brake

SDCC Select

Input state	Mode
F/R = High or Open	Function OFF
F/R = Low	Function ON

LV8111V Description

1. Speed Control Circuit

This IC can realize a high efficiency, low-jitter, a stable rotation by adopting the PLL speed control method. This the PLL circuit compares the phase difference of the edge between the CLK signal and the FG signal and controls by using the output of error. The FG servo frequency under control becomes congruent with the CLK frequency.

 f_{FG} (Servo) = f_{CLK}

2. Output Drive Circuit

This IC adopts the direct PWM drive method to reduce power loss in the output. The output transistor is always saturated while the transistor is on and adjusts the driving force of the motor by changing the duty that the output transistor is on.

The PWM switching of the output is performed by the upper-side output transistor.

Also, this IC has a parasitic diode of the output DMOS as a regeneration route when the PWM switching is off. But, this IC is cut down the fever than the diode regeneration by performing synchronous rectification.

3. Current Limiter Circuit

This IC limits the (peak) current at the value

 $I = V_{RF} / Rf (V_{RF} = 0.515V (typical), Rf : current detection resister)).$

The current limitation operation consists of reducing the PWM output on duty to suppress the current. To prevent malfunction of the current limitation operation when the reverse recovery current of diode is detected, the operation has a delay (approximately 300ns). In case of a coil resistance of motor is small or small inductance, since the current change at start-up is fast, there is a possibility that the current more than specified current is flowed by this delay.

It is necessary to set the current increases by the delay.

4. Power Saving Circuit

This IC becomes the power saving state of decreasing the consumption current in the stop state. The bias current of the majority circuits is cut in the power saving state. Also, 5V regulator output is output in the power saving state.

5. Reference Clock

Note that externally-applied clock signal has no noise of chattering. The input circuit has a hysteresis. But, if noise is a problem, that noise must be excluded by inserting capacitors across the inputs. If clock input goes to the no input state when the IC is in the start state, the drive is turned off after a few rotation of motor if the motor constrained protection circuit does operate. (Clock disconnection protection)

6. PWM Frequency

The PWM frequency is determined by using a capacitor C (F) connected to the PWM pin.

 $f_{PWM} \approx 1 / (29500 \times C) \cdots 150 pF$ or more $f_{PWM} \approx 1 / (32000 \times C) \cdots 100 pF$ or more, less than 150 pF

The frequency is oscillated at about 225kHz when a capacitor of 150pF is connected. The GND of a capacitor must be placed as close to the control block GND (GND pin) of the IC as possible to reduce influence of the output.

7. Hall Effect Sensor Input Signals

The signal input of the amplitude of hysteresis of 42mV max or more is required in the Hall effect sensor inputs. Also, an input amplitude of over 100mVp-p is desirable in the Hall effect sensor inputs in view of influence of noise. If the output waveform (when the phase changes) is distorted by noise, that noise must be excluded by inputting capacitors across the inputs.

8. FG Signals

The Hall signal of IN1 is used as the FG signal in the IC. If noise is a problem, the noise of the FG signal can be excluded by inserting a capacitor between the FGFIL pin and GND.

Note that normal operation becomes impossible if the value of the capacitor is overlarge. Also, note that the trouble of noise occurs easily when the position of GND of a capacitor is incorrect.

9. Constraint Protection Circuit

This IC has an on-chip constraint protection circuit to protect the IC and the motor in motor constraint mode. when the CSDSEL pin is set to the high level or open input, if the LD output remains high (unlocked statement) for a fixed period in the start state, this circuit operates. In the low level setting case, if the FG signal is not switched for a fixed period in the start state, this circuit is operates. Also, the upper-side output transistor is turned off while the constraint protection circuit is operating. This time is set by the capacitance of the capacitor attached to the CSD pin.

The set time (in seconds) is $102\times C~(\mu F)$

When a capacitor of $0.068\mu F$ is attached, the protection time becomes about 7.0 seconds.

The set time must be set well in advance for the motor start-up time. When the motor is decelerated by switching the clock frequency, this protection circuit is not operated. To clear the motor constrained state, the S/S pin is switched into a stop state or the power must be turned off and reapplied. Since the CSD pin also functions as the power-on reset pin, if the CSD pin were connected directly to ground, the logic circuit goes to the reset state and the speed cannot be controlled.

Therefore, if the motor constraint protection circuit is not used, a resistor of about $220k\Omega$ and a capacitor of about 4700pF must be connected in parallel between the CSD pin and GND.

10. Phase Lock Signals

(1) Phase lock range

This IC has no the speed system counter. The speed error range in the phase lock state is indeterminable only by the characteristics of the IC. (because the accelerations of the change in FG frequency influences.)

When it is necessary to specify for the speed error as a motor, the value obtained while the motor is actually operating must be measured. Since the speed error occurs easily when the accelerations of FG is large, the speed error will be the largest when the IC goes into the lock state during start-up or the unlocked state by switching the clock.

(2) Phase lock signal mask functions

When the IC goes into the lock state during start-up or the unlocked state by switching the clock, the low signal for a short-time by using the hunting when the IC goes into the locked state is masked. Therefore, the lock signal is output in stable state. But, the mask time duration causes the delay of the lock signal output. The mask time is set by the capacitance of the capacitor attached between the CLD pin and GND.

The mask time (seconds) is $1.8\times C~(\mu F)$

When a capacitor of $0.1\mu F$ is attached, the mask time becomes about 180ms. If the signals should be masked completely, the mask time must be set well in advance.

When there is no need for masking, the CLD pin must be left open.

11. Power Supply Stabilization

Since this IC is used in applications that draw large output currents and adopts the drive method by switching, the power-Supply line is subject to fluctuations. Therefore, capacitors with capacitances adequate to stabilize the power-supply voltage must be connected between the V_{CC} pin and GND. The ground-side a capacitor must be connected as close to the GND2 pin of power GND as possible. If it is impossible to connect a capacitor (electrolytic capacitor) near the pin, the ceramic capacitor of about 0.1μ F must be connected as close to the pin as possible. If diodes are inserted in the power-supply line to prevent IC destruction due to reverse power supply connection, Since this makes the power-supply voltage even more subject to fluctuations, even larger capacitors will be required.

12. VREG Stabilization

To stabilize the VREG voltage that is the power supply of the control circuit, connect a capacitor of 0.1μ F or more. GND of the capacitor must be attached as close to the control block GND (GND1 pin) of the IC as possible.

13. Error Amplifier

External components of the error amplifier block must be placed as close to the IC as possible to reduce influence of noise.

Also, these components must be placed as separate from the motor as possible.

14. IC Reverse Metal

To improve heat radiation, the metal part on the reverse of IC is stuck fast to the substrate by using highly-conduction solder.

15. SDCC (Speed Detection Current Control) function

The SDCC circuit controls the speed detection current. It limits the current to 75% of the specified current to reduce acceleration of the motor when the rotation of the motor exceeds 95% of its target speed. This enables stabilized phase lock pull-in and minimizes the variation in startup time.

The SDCC function is enabled by setting F/R low. It is disabled by setting F/R high or open.

Notes: If the selected state of SDCC does not match the rotational direction of the motor, it is necessary to solve the problem by changing the HALL bias.

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