Ordering number : ENN7812

SANYO Semiconductors

DATA SHEET

Bi-CDMOS IC

LV8223T — Motor driver system in CD and MD players

Overview

The LV8223T is a system driver IC that can implement, with a single chip, all the motor driver circuits required in CD and MD drives. The LV8223T provides three-phase PWM spindle, three-phase sled, focus, and tracking drivers. Since it integrates lifting drivers (three PWM H bridge channels) and one half-bridge channel on the same chip, it can contribute to further miniaturization, thinner form factors, and lower power in end products. The spindle motor driver adopts a direct PWM sensorless drive technique for highly efficient motor drive requiring a minimal number of external components.

Functions

- PWM H bridge motor drivers (3 channels)
- Three-phase stepping motor driver
- Half-bridge driver
- Direct PWM sensorless motor driver

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		5.0	V
Output block supply voltage	VS max		4.5	V
Predriver voltage (gate voltage)	VG max		6.5	V
Output current	I_O max		0.7	A
Allowable power dissipation 1	Pd max1	Independent IC	0.45	W
Allowable power dissipation 2	Pd max2	Mounted on a 50 × 50 × 1.6 mm glass epoxy PCB (reference value)	1.25	W
Operating temperature	Topr		–20 to +85	°C
Storage temperature	Tstg		–55 to +150	°C

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.1 to 4.0	V
Output block supply voltage	VS		0 to VG – 3.0 < V_{CC}	V
Predriver voltage (gate voltage)	VG		VS + 3 to 6.4	V

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Electrical Characteristics at Ta = 25°C, V_{CC} = 2.4 V

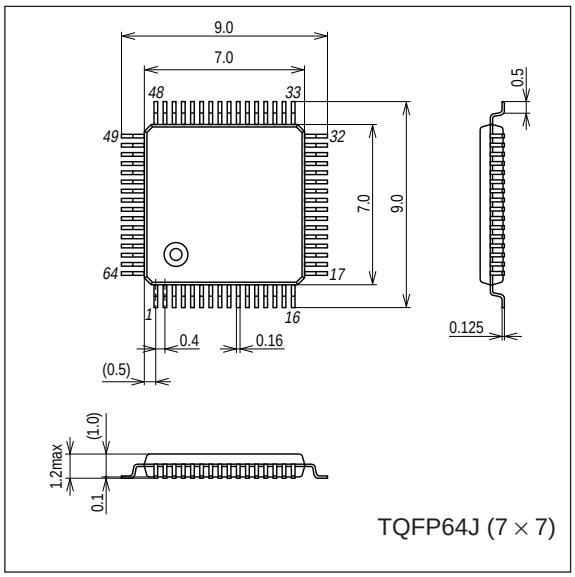
Parameter	Symbol	Conditions	Ratings			Unit	Test circuit diagram
			min	typ	max		
Current drain 1	$I_{CC}1$	S/S pin: high (operating mode)		1.5	2.0	mA	1
Current drain 2	$I_{CC}2$	S/S pin: low (standby mode)			20	μA	2
[Charge Pump Output]							
Output voltage	VG		5.6	6.1	6.4	V	1
Actuator Block (Focus, tracking, head up/down, and half bridge actuator drivers) [Actuator Input Pins]							
High-level input voltage range	V_{AIH}		V_{CC} – 0.5		V_{CC}	V	3
Low-level input voltage range	V_{AIL}		0		0.5	V	3
[Output Block]							
Output on-resistance	Ron1, 2, 3	I_O = 0.5 A, sum of the high and low sides		0.8	1.2	Ω	4
Output transmission delay time (H bridge)	T_{RISE}	Design target value *		0.05		μs	*
	T_{FALL}	Design target value *		0.05		μs	*
Minimum input pulse width	tmin	With the channel 1 and channel 2 pulse widths ≥ 2/3 tmin Design target value *		100		ns	*
[MUTE Pin]							
High-level input voltage range	VMUH	MUTE OFF	V_{CC} – 0.5		V_{CC}	V	5
Low-level input voltage range	VMUL	MUTE ON	0		0.5	V	5
Three-Phase Stepping Motor Block [Logic Input Pins]							
High-level input voltage range	VSL_{IH}		V_{CC} – 0.5		V_{CC}	V	3
Low-level input voltage range	VSL_{IL}		0		0.5	V	3
[Phase Detector Comparator Block]							
Input offset voltage	V_{SLOFS}		–9		+9	mV	6
Common-mode input voltage range	V_{SLCM}		0		V_{CC}	V	7
High-level output voltage	V_{SLCH}	I_O = –0.5 mA	V_{CC} – 0.5		V_{CC}	V	8
Low-level output voltage	V_{SLCL}	I_O = 0.5 mA			0.5	V	8
[Output Block]							
Output on-resistance	RonSL	I_O = 0.5 A, sum of the high and low sides		0.8	1.2	Ω	9
Spindle Motor Driver Block [Output Block On-Resistance]							
SOURCE1	Ron (H1)	I_O = 0.5 A, VS = 1.2 V, VG = 6 V Forward drive transistor		0.4	0.6	Ω	10
SOURCE2	Ron (H2)	I_O = 0.5 A, VS = 1.2 V, VG = 6 V Reverse drive transistor		0.4	0.6	Ω	10
SINK	Ron (L)	I_O = 0.5 A, VS = 1.2 V, VG = 6 V		0.4	0.6	Ω	10
SOURCE + SINK	Ron (H+L)	I_O = 0.5 A, VS = 1.2 V, VG = 6 V		0.8	1.2	Ω	10
[Position Detector Comparator]							
Input offset voltage	V_{SOFS}	Design target value	–9		+9	mV	*
[VCO Pin]							
VCO high-level voltage	V_{COH}		0.65	0.80	0.90	V	11
VCO low-level voltage	V_{COL}		0.35	0.50	0.60	V	11
[S/S Pin]							
High-level input voltage range	V_{SSH}	Start	V_{CC} – 0.5		V_{CC}	V	5
Low-level input voltage range	V_{SSL}	Stop	0		0.5	V	5
[BREAK Pin]							
High-level input voltage range	V_{BRH}	Brake off	V_{CC} – 0.5		V_{CC}	V	12
Low-level input voltage range	V_{BRL}	Brake on	0		0.5	V	12
[PWM Pin]							
High-level input voltage range	V_{PWMH}		V_{CC} – 0.5		V_{CC}	V	12
Low-level input voltage range	V_{PWML}		0		0.5	V	12
PWM input frequency	V_{PWMIN}				190	kHz	13
[CLK pin]							
High-level input voltage range	V_{CLKH}		V_{CC} – 0.5		V_{CC}	V	14
Low-level input voltage range	V_{CLKL}		0		0.5	V	14
[FG Output Pin]							
High-level output voltage	V_{FGH}	I_O = –0.5 mA	V_{CC} – 0.5		V_{CC}	V	8
Low-level output voltage	V_{FGL}	I_O = 0.5 mA	0		0.5	V	8

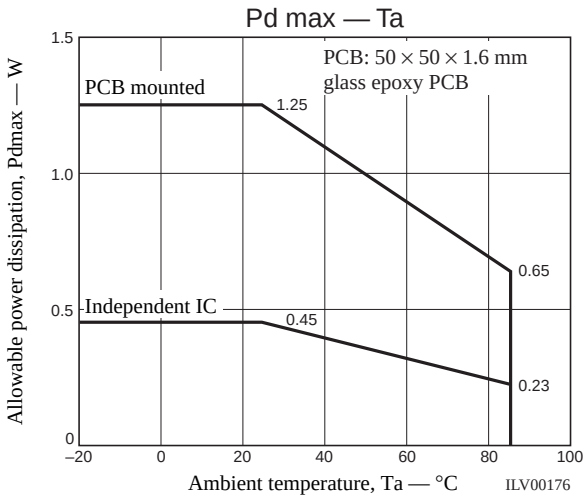
*: Design target value parameters are not tested.

Package Dimensions

unit : mm

3289





Actuator Truth Tables

Focus, Tracking, and Head Up/Down Driver Blocks

MUTE	IN1, 2F	IN1, 2R	OUT1, 2F	OUT1, 2R
H	L	L	L	L
H	H	L	H	L
H	L	H	L	H
H	H	H	L	L
L	×	×	Z	Z

MUTE2	IN3F	IN3R	OUT3F	OUT3R
H	L	L	L	L
H	H	L	H	L
H	L	H	L	H
H	H	H	L	L
L	×	×	Z	Z

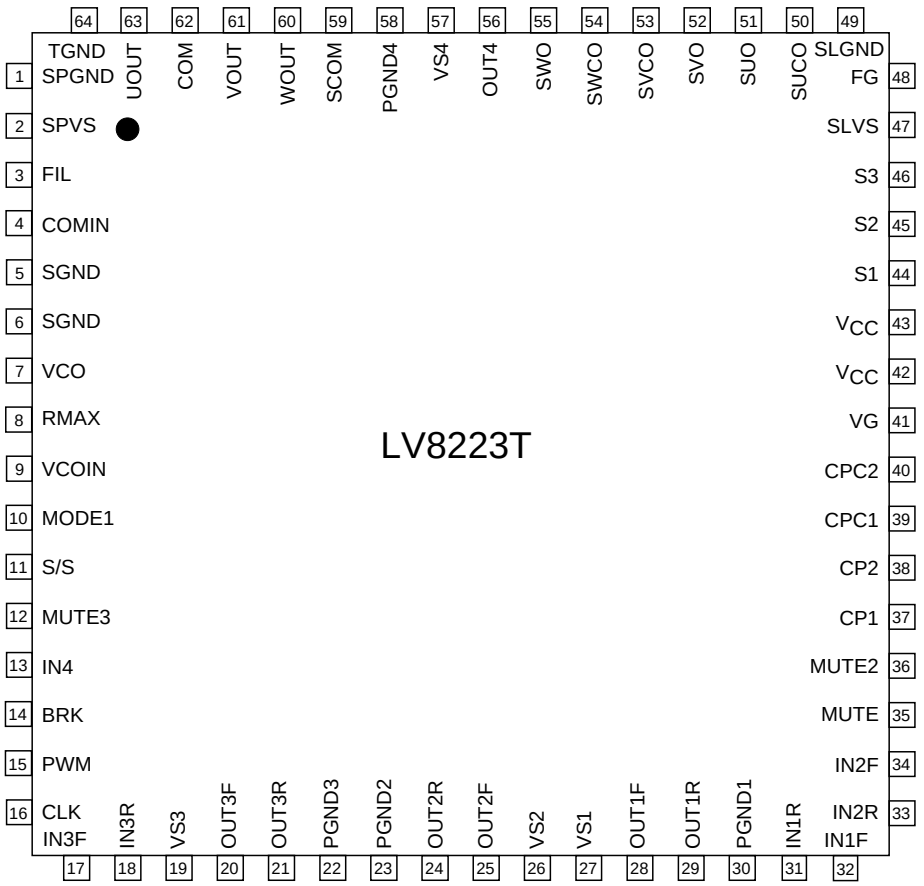
MUTE3	IN4	OUT4
H	L	L
H	H	H
L	×	Z

Sled Stepping Motor Driver Block

MUTE	S1	S2	S3	SUO	SVO	SWO
H	L	L	L	H	L	Z
H	H	L	L	H	Z	L
H	L	H	L	Z	H	L
H	H	H	L	L	H	Z
H	L	L	H	L	Z	H
H	H	L	H	Z	L	H
H	L	H	H	Z	Z	Z
H	H	H	H	Z	Z	Z
L	×	×	×	Z	Z	Z

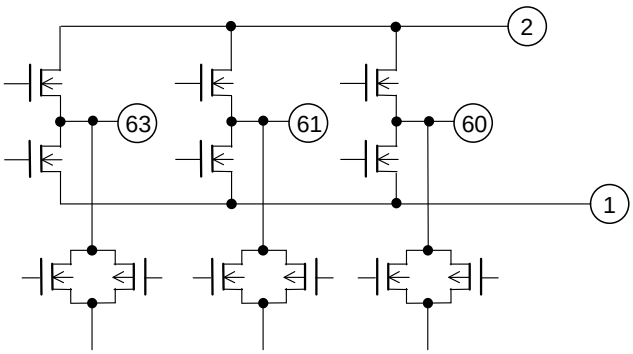
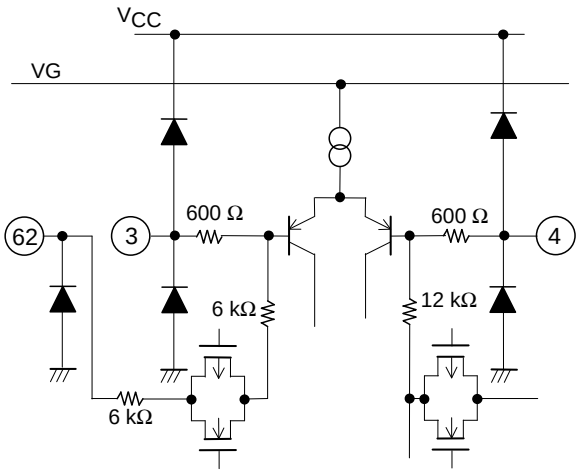
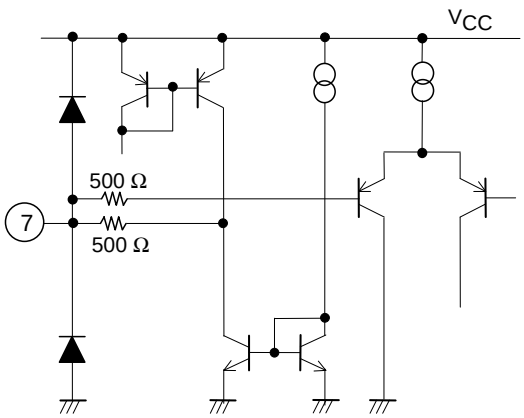
Z: Open

Pin Assignment



Top view

Pin Function

Pin No.	Pin Name	Pin Description	Equivalent circuit
1	SPGND	Spindle output block ground	
2	SPVS	Spindle motor driver power supply. Insert a capacitor between this pin and ground.	
63 61 60	UOUT VOUT WOUT	Outputs. Connect these pins to the spindle motor coils.	
62	COM	Spindle motor common point connection	
3	FIL	Spindle motor position detector comparator filter connection. Insert a capacitor between this pin and the COMIN pin (pin 4).	
4	COMIN	Spindle motor position detector comparator differential input. Insert a capacitor between this pin and the FIL pin (pin 3).	
5, 6 64	SGND TGND	Small signal system ground	
7	VCO	VCO oscillator connection. Insert a capacitor between this pin and ground. The VCO oscillator frequency follows the speed of the spindle motor.	

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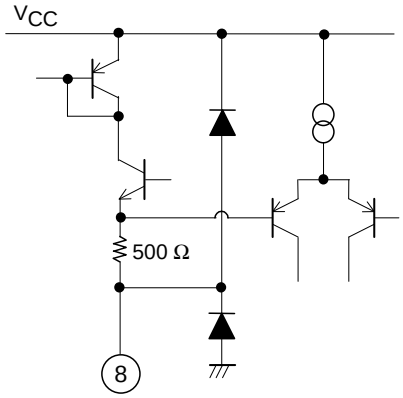
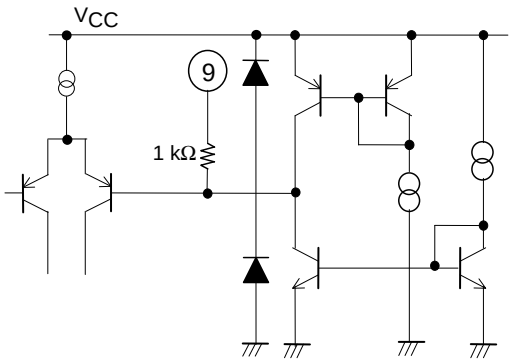
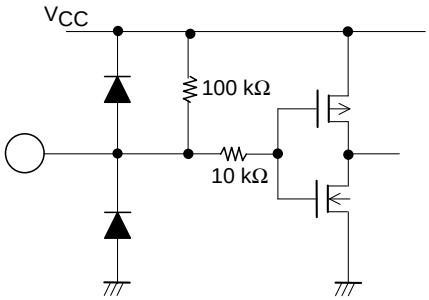
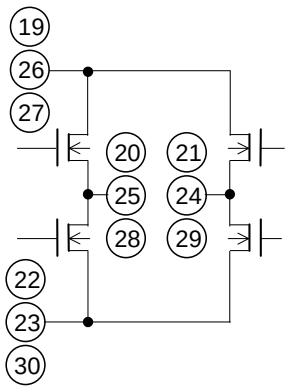
Pin No.	Pin Name	Pin Description	Equivalent circuit
8	RMAX	VCO maximum frequency setting. Insert a resistor between this pin and ground. Reducing the value of that resistor increases the maximum VCO frequency.	
9	VCOIN	VCO control voltage input. Insert a capacitor between this pin and ground. A control output proportional to the motor speed is generated by IC internal logic, and this is used to charge and discharge the capacitor. The voltage on this pin controls the VCO oscillator frequency.	
14	BRK	Spindle block brake function control. A low-level input to this pin switches the IC to reverse torque brake mode.	
44 45 46	S1 S2 S3	Sled block logic inputs	
19 26 27	VS3 VS2 VS1	H bridge circuit power supply. Insert capacitors between these pins and ground.	
22 23 30	PGND3 PGND2 PGND1	H bridge output block ground connections	
20, 21 25, 24 28, 29	OUT3F/R OUT2F/R OUT1F/R	H bridge circuit forward/reverse outputs. Connect these pins to the motor coils.	

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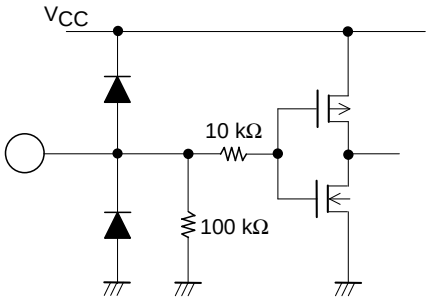
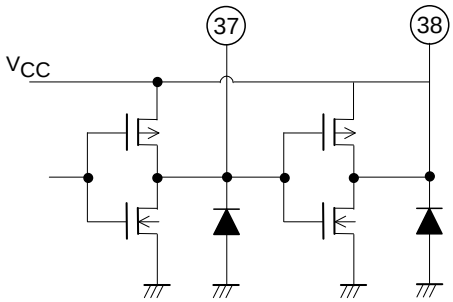
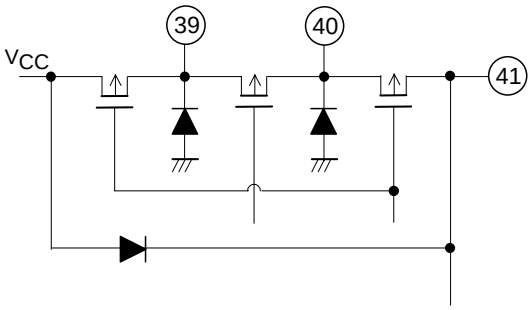
Pin No.	Pin Name	Pin Description	Equivalent circuit
10	MODE1	Spindle block PWM frequency switching. The CLK pin (pin 16) and PWM pin (pin 15) input frequencies have the relationship shown below. When a high level is input: fPWM = fCLK/32 When a low level is input: fPWM = fCLK/64	
11	S/S	Spindle motor block start/stop control. The circuit operates in start mode when a high level is input.	
12	MUTE3	Half bridge circuit muting control. The output pin (OUT4) goes to the high-impedance state (muted state) when a low level is input.	
13	IN4	Half bridge circuit control input	
15	PWM	Spindle block PWM signal input. The output transistor is turned on when a high level is input to this pin.	
16	CLK	Reference clock input used for logic operations. Input a spindle PWM signal with a frequency 32 or 64 times the frequency of this signal.	
17, 18 31, 32 33, 34	IN3F/R IN1F/R IN2F/R	Actuator H bridge block logic inputs	
35	MUTE	H bridge 1 and 2, and 3 phase sled muting control. The OUT1R/F, OUT2R/F, SUO, SVO, and SWO pins go to the high-impedance state (muted state) when a low level is input to this pin.	
36	MUTE2	H bridge 3 muting control. The OUT3R/F pin goes to the high-impedance state (muted state) when a low level is input to this pin.	
37	CP1	Charge pump step-up pulse output. Insert a capacitor between this pin and the CPC1 pin (pin 39). Leave this pin open if a voltage stepped up by a factor of 2 is to be used.	
38	CP2	Charge pump step-up pulse output. Insert a capacitor between this pin and the CPC2 pin (pin 40).	
39	CPC1	Charge pump step-up connection. Insert a capacitor between this pin and the CP1 pin (pin 37).	
40	CPC2	Charge pump step-up connection. Insert a capacitor between this pin and the CP2 pin (pin 38).	
41	VG	Charge pump step-up output. Insert a capacitor between this pin and ground.	
42, 43	V_{CC}	Power supply used for the small signal system. Insert a capacitor between these pins and ground.	

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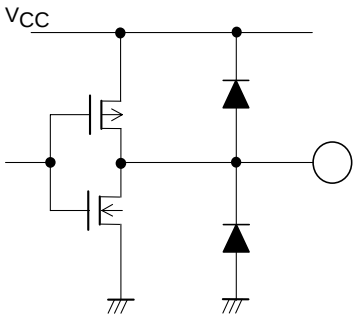
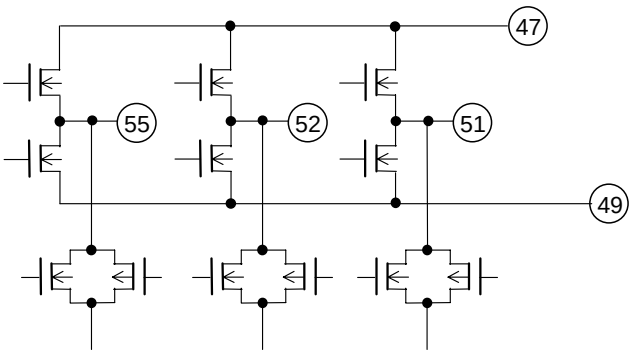
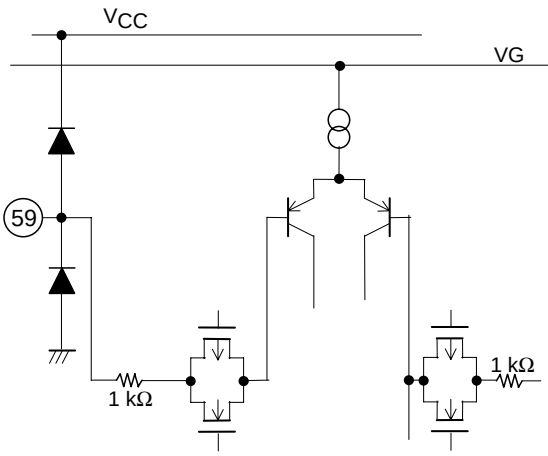
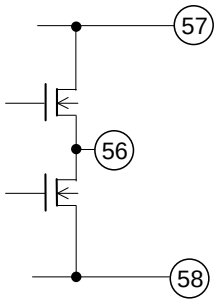
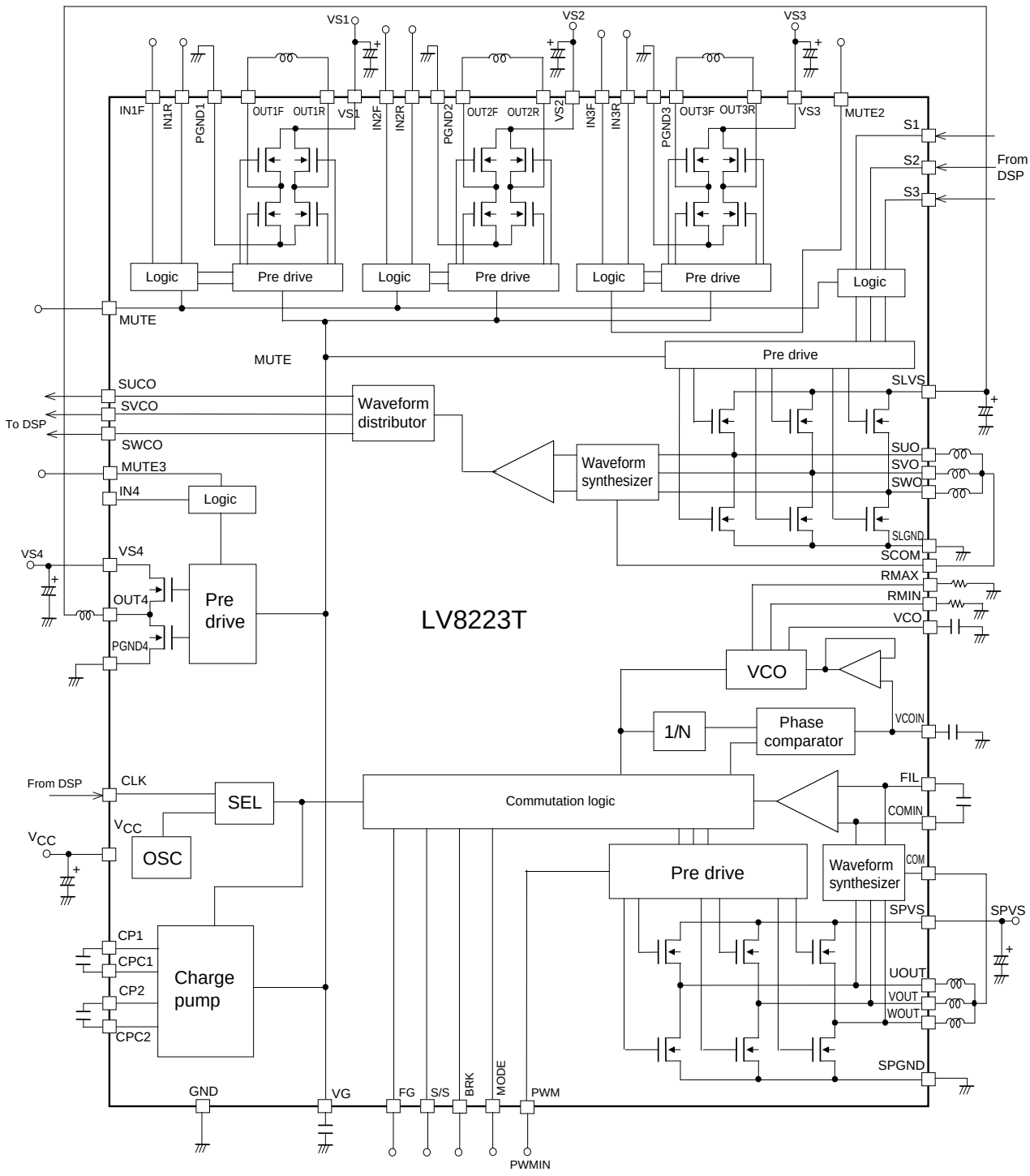
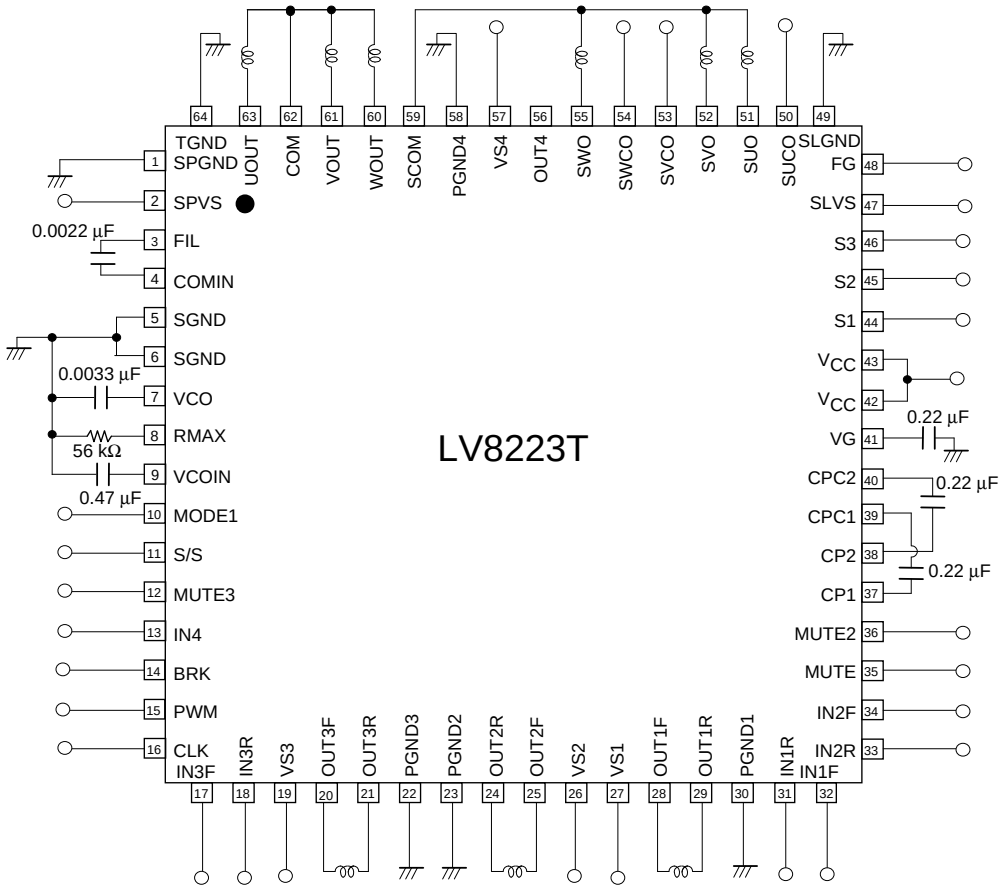
Pin No.	Pin Name	Pin Description	Equivalent circuit
48	FG	Spindle FG pulse signal output. This pin outputs a signal equivalent to the signal provided when 3 Hall sensors are used.	
50	SUCO	Sled block SUO output phase position detector comparator output	
53	SVCO	Sled block SVO output phase position detector comparator output	
54	SWCO	Sled block SWO output phase position detector comparator output	
49	SLGND	Sled output block ground	
47	SLVS	Sled motor drive power supply. Insert a capacitor between this pin and ground	
51 52 55	SUO SVO SWO	Outputs. Connect these pins to the sled motor coils.	
59	SCOM	Sled motor common point connection	
56	OUT4	Half bridge output. Connect this pin to the motor coil.	
57	VS4	Half bridge power supply. Insert a capacitor between this pin and ground.	
58	PGND4	Half bridge output block ground	

Block Diagram



Sample Application Circuit



* Capacitors must be inserted between each VS and PGND pair, and between each V_{CC} and SGND pair.

LV8223T Functional Description and Notes on External Components

The LV8223T is a system driver IC that implements, in a single chip, all the motor driver circuits required for CD and MD players. Since the LV8223T provides a spindle motor driver, a three-phase sled stepping motor driver, three H bridge drivers for the focus, tracking, and head up/down actuators, and a single half bridge motor driver channel, it can contribute to thinner form factors and further miniaturization in end products. Since the spindle motor driver uses a direct PWM sensorless drive technique, it achieves high-efficiency motor drive with a minimal number of external components.
Read the following notes before designing driver circuits using the LV8223T to design a system with fully satisfactory characteristics.

Output Drive Circuit and Speed Control Methods
The LV8223T adopts the synchronous commutation direct PWM drive method to minimize power loss in the output circuits. Low on-resistance DMOS devices (total high and low side on-resistance: 0.8 Ω, typical) are used as the output transistors.

The spindle motor driver speed is controlled by BRK and PWM signals provided by an external DSP. The PWM signal controls the sink side transistor. That transistor is switched according to the input duty of the signal input to the PWM pin (pin 15) to control the motor speed. (The sink side transistor is on when the PWM input is high, and off when the PWM input is low.)

Soft Switching Circuit
This IC uses variable duty soft switching to minimize motor drive noise. An excitation current on/off dual-sided soft switching technique is used for this soft switching.
Note that the LV8223T does not use soft switching drive, but instead uses hard switching drive, if it is not supplied with a CLK signal from the DSP. In this operating mode, the CLK signal is provided by an internal oscillator circuit.

VCO Circuit Constants
The LV8223T spindle block adopts a sensorless drive technique. Sensorless drive is implemented by detecting the back EMF signal generated by the motor and setting the commutation timing accordingly. Thus the timing control uses the VCO signal. We recommend using the following procedure to determine the values of the VCO circuit's external components.

1. Connect components with provisional values.
   Connect a 2.2 µF capacitor between the VCOIN pin (pin 9) and ground, connect a 68 kΩ resistor between the RMAX pin (pin 8) and ground, and connect a 3300 pF capacitor between the VCO pin (pin 7) and ground.
2. Determine the value of the VCO pin (pin 7) capacitor.
   Select a value such that the startup time to the target speed is the shortest and such that the variations in startup time are minimized. If the value of this capacitor is too large, the variations in the startup time will be excessive, and if too small, the motor may fail to turn. Since the optimal value of the VCO pin constant differs with the motor characteristics and the startup current, the value of this component must be verified again if the motor used or any circuit specifications are changed.
3. Determine the value of the RMAX (pin 8) resistor.
   Select a resistor value such that the VCOIN pin voltage is about V_{CC} − 1.0 V or lower with the motor operating at the target speed. If the value of this resistor is too large, the VCOIN pin voltage may rise excessively.
4. Determine the value of the VCOIN pin (pin 9) capacitor.
   If the FG output (pin 48) pulse signal becomes unstable at the lowest motor speed that will be used, increase the value of the VCOIN pin capacitor.
5. Determine the value of the resistor connected between the VCOIN pin (pin 9) and ground.
   When intermittent drive (free-running deceleration) using the S/S and MUTE pins is used to reduce system power consumption and the system locks up on restart, a large resistor (several MΩ) must be connected to discharge the capacitor connected to the VCOIN pin.
   Choose a value for this resistor such that the time for complete discharge is longer than the motor free-running deceleration time. Note that if an oscilloscope probe is attached to the VCOIN pin when determining the value of this constant, the discharge characteristics will differ due to the probe impedance. This issue requires care when testing in an actual system. (We recommend using an FET probe.)
   (Reason that a discharge resistor is required when the locked state occurs: Since the commutation timing in sensorless drive is determined by detecting the back EMF signal generated by the motor, the timing and other aspects are controlled based on the VCO signal. Therefore, the VCO control voltage is generated according to the speed of

the spindle motor. When a voltage independent of the spindle motor speed is applied to the VCOIN pin, the commutation timing will be disrupted and startup and drive operation will be adversely affected.)

S/S and MUTE Circuits

The S/S pin (pin 11) functions as the spindle motor driver start/stop pin; a high-level input specifies operation in the start state. The MUTE, MUTE2, and MUTE3 pins (pins 35, 36, and 12) control the drivers other than the spindle block; a low-level input to these pins applies muting to the corresponding block or blocks. When a low level is applied, the corresponding drivers (the H bridge blocks and the three-phase sled block) go to the high-impedance state for all outputs, regardless of the logic inputs. (The MUTE pin mutes the H bridge 1 and 2 blocks and the three-phase sled block, the MUTE2 pin mutes the H bridge 3 block, and the MUTE3 pin mutes the half bridge block.)

Since the S/S, MUTE, MUTE2, and MUTE3 pins operate independently, all of the S/S, MUTE, MUTE2, and MUTE3 pins must be set to the low level to set the IC to full standby mode (power saving mode).

Braking Circuit

The BRK pin (pin 14) switches the direction of the torque applied by the spindle motor driver; when a low level is applied to the BRK pin, the driver switches to reverse torque braking mode. When the motor decelerates to an adequately low speed in reverse torque braking mode, the driver switches to short-circuit braking mode to stop the motor. (Note: the IC cannot be set to low-power mode at this time.)

Note that when stopping the motor with the braking function, if this circuit switches to short-circuit braking too quickly and problems such as the motor remaining in motion occur, the value of the resistor connected to the RMAX pin (pin 8) must be reduced. If the motor moves back and forth without stopping and the IC does not switch to short-circuit braking when the speed approaches zero, insert a resistor with a value of a few kΩ at the COM pin. (Caution: Verify that insertion of this resistor does not degrade the startup characteristics.)

Notes on the CLK and PWM Signals

The LV8223T CLK pin (pin 16) is used as the sensorless logic reference clock, for step-up circuit pulse generation, and for other purposes. Therefore, if the CLK signal is supplied from the DSP, it must always be input in start mode. The CLK input signal must have a frequency that is either 32 to 64 times that of the PWM input signal. The MODE1 pin (pin 10) selects the relationship between the CLK and PWM frequencies. If the CLK signal is 32 times the PWM signal, the MODE1 pin must be set high, and if the CLK signal is 64 times the PWM signal, the MODE1 pin must be set low. We recommend that the CLK input frequency be less than 10 MHz.

As was mentioned previously in the section on soft switching, if the CLK signal is not supplied by the DSP (the CLK pin is left open or is shorted to ground), the internal oscillator circuit operates and supplies the CLK signal. Since the CLK signal and the PWM signal will be asynchronous in this case, the spindle motor drive operation will not be soft switching drive, but will be hard switching drive.

FG Output Circuit

The FG pin (pin 48) is the spindle block FG output. It outputs a pulse signal equivalent to a three Hall sensor FG output. This output has an MOS circuit structure.

Spindle Block Position Detector Comparator Circuit

The spindle block position detection comparator circuit is provided to detect the position of the rotor using the back EMF generated when the motor turns. The IC determines the timing with which the output block applies current to the motor based on the position information acquired by this circuit. Startup problems due to comparator input noise can be resolved by inserting a capacitor (about 1000 to 4700 pF) between the COMIN pin (pin 4) and the FIL pin (pin 3). Note that if this capacitor is too large, the output commutation timing may be delayed at higher speeds and efficiency may be reduced.

Charge Pump Circuit

The LV8223T n-channel DMOS output structure allows it to provide a charge pump based voltage step-up circuit. A voltage 3 times the V_{CC} voltage (or about 6.5 V) can be acquired by inserting a capacitor (recommended value: 0.22 μF or larger) between the CP2 and CPC2 pins. We recommend using this circuit with values such that the voltage relationship between the stepped-up voltage (VG) and the motor supply voltage (VS) is VG – VS ≥ 3.0 V. Note that this circuit is designed so that the stepped-up voltage (VG) is clamped at about 6.5 VDC. A larger capacitor must be used on the VG pin if the ripple on the stepped-up voltage (VG) results in VGmax exceeding 6.8 V.

Observe the following points if the VG voltage is supplied from external circuits.

- The VG voltage supplied from the external circuits must not exceed the absolute maximum rating VGmax.
- The capacitor between the CP and CPC pins (pin 37 and 40) is not required.

- The VG voltage must be applied in the correct order. The VG voltage must be applied after the V_{CC} level is applied, and must be cut before the V_{CC} power supply is turned off.
- There is an IC-internal diode between the V_{CC} and VG pins. Therefore, supply voltages such that V_{CC} > VG must never be applied to this IC.

Three-Phase Sled Driver Circuit

This circuit is used as the sled motor driver circuit. The SUC0 to SWC0 pins (pin 50, 53, and 54) are the sled driver position detector comparator output pins. They have an MOS output structure. These pins are used to feed back the sled motor speed and position information to the DSP or microcontroller. The S1 to S3 pins (pins 44, 45, and 46) are the sled driver logic inputs, and are connected to the DSP. These pins have built-in pull-up resistors.

Actuator Block

The LV8223T provides three H bridge channels for use as focus and tracking actuator drivers. The actuator block logic input pins have built-in pull-down resistors. PWM is used for control, and the block supports synchronous commutation.

Notes on PCB Pattern Design

The LV8223T is a system driver IC implemented in a Bi-DMOS process; the IC chip includes bipolar circuits, MOS logic circuits, and MOS drive circuits integrated on the same chip. As a result, extreme care is required with respect to the pattern layout when designing application circuits.

- Ground and V_{CC}/VS wiring layout
  The LV8223T ground and power supply pins are classified as follows.
  Small-signal system ground pins → SGND (pins 5 and 6), TGND (pin 64)
  Large-signal system ground pins → SPGND (pin 1), PGND1 (pin 27), PGND2 (pin 23), PGND3 (pin 22), SLGND (pin 49)
  Small-signal system power supply pins → V_{CC} (pins 42 and 43)
  Large-signal system power supply pins → SPVS (pin 2), SLVS (pin 47), VS1 (pin 30), VS2 (pin 26), VS3 (pin 19), VS4 (pin 57)
  Capacitors must be inserted, as close as possible to the IC, between each of the small-signal system power supply pins (pins 42 and 43) and the ground pins (pins 5 and 6).
  The large-signal system ground pins (the PGND system) must be connected with the shortest possible lines, and furthermore in a manner such that there is no shared impedance with the small-signal system ground lines. Capacitors must also be inserted, as close as possible to the IC, between the large-signal system power supply (VS system) pins and the large-signal system ground pins.

- Positioning the small-signal system external components
  The small-signal system external components that are connected to ground must be connected to the small-signal system ground with lines that are as short as possible.