


SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV8415CB

Bi-CMOS integrated circuit
 Blurring correction driver IC for DSC
 H bridge × 2ch driver

Overview

LV8415CB is blurring correction driver IC for DSC.

Functions

- Actuator driver (saturation drive H bridge) × 2ch
- Constant current hall bias circuit × 2ch
- With built-in for PWM signal generation logic circuit × 2ch
- 8bitDAC for hall amplifier offset adjustment × 2ch
- Two systems in power supply (V_M : for actuator, V_{CC})
- With built-in low voltage malfunction prevention circuit
- Hall Amplifier × 2ch
- General-purpose amplifier × 2ch
- 8bitDAC for hall bias × 2ch
- Three line serial input
- With built-in thermal protection circuit

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_M max		6	V
Supply voltage 2	V_{CC} max		6	V
Output peak current	I_O peak	OUT1 to 2 ($t \leq 10\text{msec}$, duty $\leq 20\%$)	600	mA
Output current	I_O max	OUT1 to 2	350	mA
Hall bias current	I_{HB} max		5	mA
Allowable power dissipation	P_d max	On a specified board *	1	W
Operating temperature	T_{opr}		-20 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* Specified board: 40.0mm×50.0mm×0.8mm, Four layers fiberglass epoxy circuit board.

Allowable Operating Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	V_M		2.7 to 5.5	V
Supply voltage range 2	V_{CC}		2.7 to 5.5	V
Logic input voltage	V_{IN}		0 to $V_{CC}+0.3$	V

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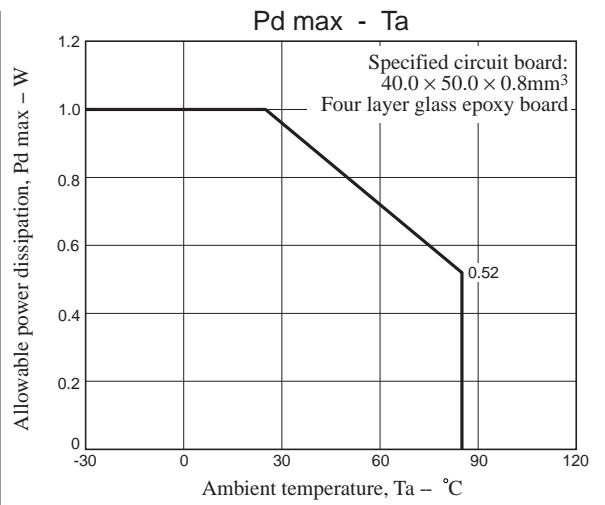
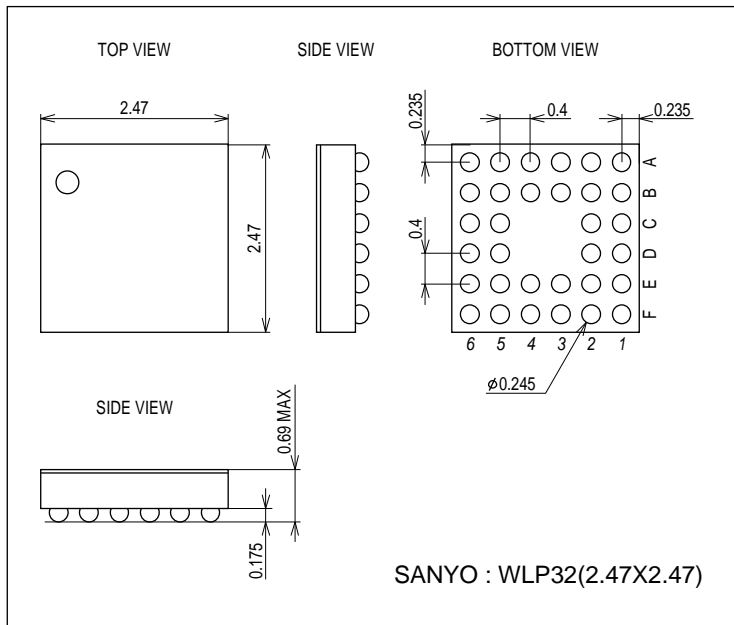
Electrical Characteristics at Ta = 25°C, VCC = 3.3V, VM = 5.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current consumption when standing by	I _{CCO}	ST = "L"			1.0	μA
VM current consumption	I _M	V _M = 5.0V, ST = "H", no load			10	μA
V _{CC} current consumption	I _{CC}	ST = "H", no load		2	3.2	mA
V _{CC} low voltage cutting voltage	V _{THVCC}		2.1	2.4	2.6	V
Low voltage hysteresis voltage	V _{THHYS}		100	150	200	mV
Thermal shutdown temperature	TSD	Design guarantee	155	175	195	°C
Thermal hysteresis width	ΔTSD	Design guarantee	15	35	55	°C
H bridge output (OUT1-2)						
Output on resistance	R _{onU}	I _O = 100mA, Upper-side on resistance		0.7	0.98	Ω
	R _{onD}	I _O = 100mA, Under-side on resistance		0.5	0.7	Ω
Output leakage current	I _{O leak}				1	μA
Diode forward voltage	V _D	I _D = -100mA		0.7		V
Operational amplifier (OP-AMP1-4)						
Input offset voltage	OP_VIO			±1	±5	mV
Input offset current	OP_IIO			±5	±50	nA
Input bias current	OP_IB			30	250	nA
Equal phase input voltage range	VICM		0		V _{CC}	V
Equal phase signal removal ratio	CMR		60	80		dB
Large amplitude voltage range	VG	R _L = 20kΩ, V _{IN} = 1mV(open loop gain)	1	10		V/mV
Output voltage range	V _{OH}	R _L = 20kΩ	V _{CC} -0.2			V
	V _{OL}	R _L = 20kΩ			0.2	V
Power supply change removal ratio	SVR		65	85		dB
Output current (sink/source)	OP_IO		1	2		mA
Hall bias (HB1-2)						
Output current	I _{HB}	R _{HG} = 1kΩ, V _{HBIN} = 1.0V	0.95	1.00	1.05	mA
Output saturation voltage	V _{SATHB}	I _{HB} = 1mA	V _{CC} -0.2			V
Standard voltage						
Standard voltage	V _{REF}		1.60	1.65	1.70	V
Standard voltage load characteristic	V _{Rref}	I _{REF} = 100μA	1.60	1.65	1.70	V
Internal CLK frequency for PWM drive						
CLK frequency	F _{clk}		13.5	15	17.25	MHz
Control pin (ST, SCLK, DATA, STB)						
Built-in pull-down resistance	R _{in}		50	100	200	kΩ
Input current	I _{INL}	V _{IN} = 0V			1.0	μA
	I _{INH}	V _{IN} = 3.3V	20	33	50	μA
Input "L" level voltage	V _{INL}				1.0	V
Input "H" level voltage	V _{INH}		2.5			V

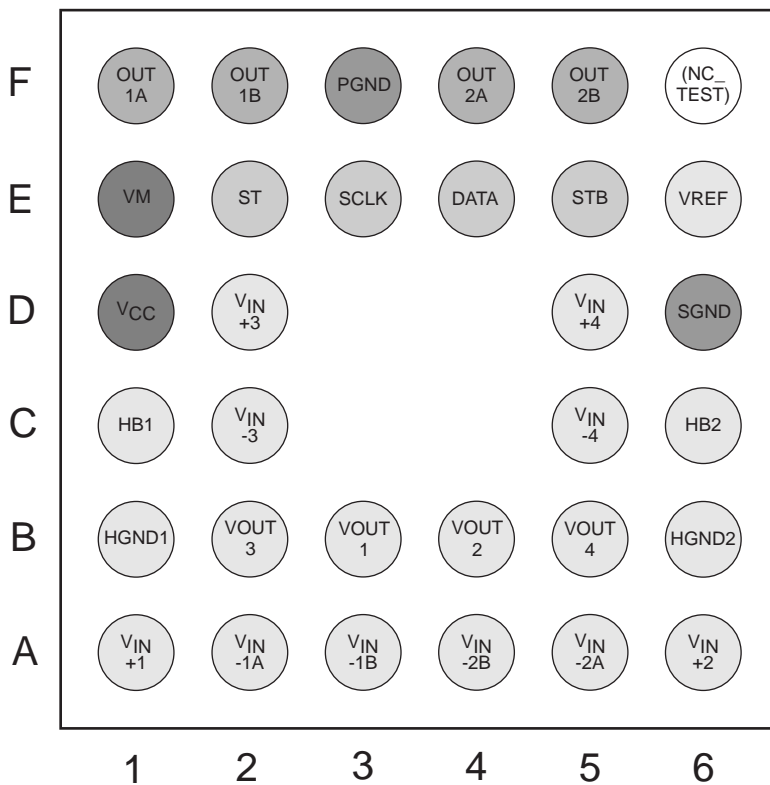
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Package Dimensions

unit : mm (typ)
3397



Pin Assignment



(NC_TEST) is pin only for the test. Please NC_TEST pin connect GND line.

- Power supply pin
- GND pin
- Output pin
- Logic control pin
- Analog control pin

Ball side view

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Pin function

Pin No.	Pin name	Pin function	Equivalent Circuit
E2 E3 E4 E5	ST SCLK DATA STB	Input pin. High level 2V to ($V_{CC} = 3.3V$) Low level 0 to 0.5V ($V_{CC} = 3.3V$)	
F1 F2 F4 F5 E1 F3	OUT1A OUT1B OUT2A OUT2B VM PGND	Output pin. (PWM output) VM : POWER – Power supply pin. PGND : POWER – GND pin.	
D1 D6	VCC SGND	Signal system power supply pin Signal system GND pin	
C1 B1 C6 B6	HB1 HGND1 HB2 HGND2	HB1, 2 pin Hall bias source pin HGND1, 2 pin Hall bias current setting pin	
A1 A2 A3 A6 A5 A4	V _{IN+1} V _{IN-1A} V _{IN-1B} V _{IN+2} V _{IN-2A} V _{IN-2B}	Hall amplifier input pin V _{IN+} Hall amplifier+ input pin V _{IN-A} Hall amplifier- input pin V _{IN-B} LPF formation pin (The filter is formed for the noise removal.)	
B3 B4	VOUT1 VOUT2	Hall amplifier output pin. VOUT1 : Hall amplifier 1ch output pin. VOUT2 : Hall amplifier 2ch output pin.	

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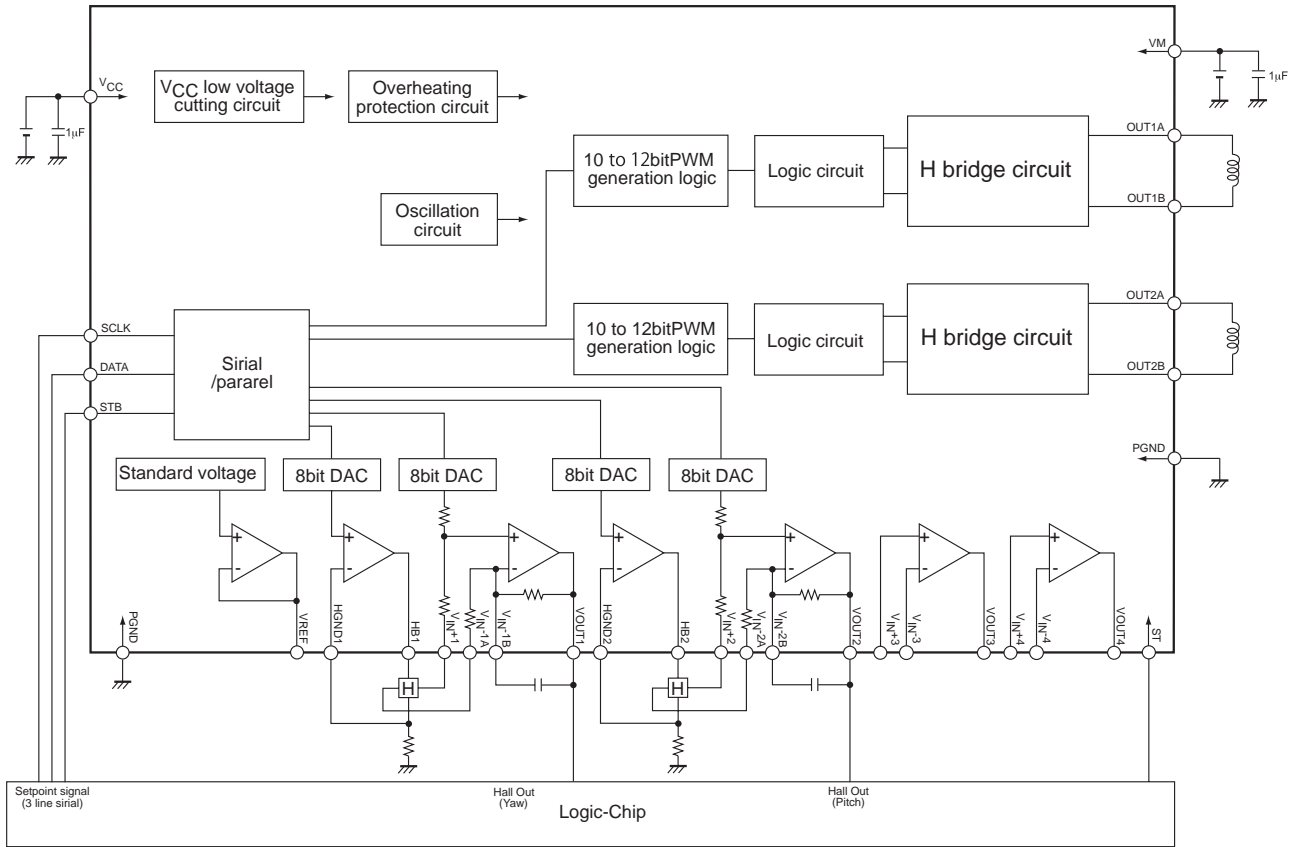
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Pin No.	Pin name	Pin function	Equivalent Circuit
D2 C2 D5 C5	V_{IN+3} V_{IN-3} V_{IN+4} V_{IN-4}	General purpose amplifier input pin. V_{IN+3} : 3ch general purpose amplifier+ input pin V_{IN-3} : 3ch general purpose amplifier- input pin V_{IN+4} : 4ch general purpose amplifier+ input pin V_{IN-4} : 4ch general purpose amplifier- input pin	
B2 B5	V_{OUT3} V_{OUT4}	General purpose amplifier output pin. V_{OUT3} : 3ch general purpose amplifier output pin V_{OUT4} : 4ch general purpose amplifier output pin	
E6	V_{REF}	Internal standard voltage pin $V_{CC}/2$ output	
F6	NC-TEST	N.C. pin TEST pin Please NC_TEST pin connect GND line.	

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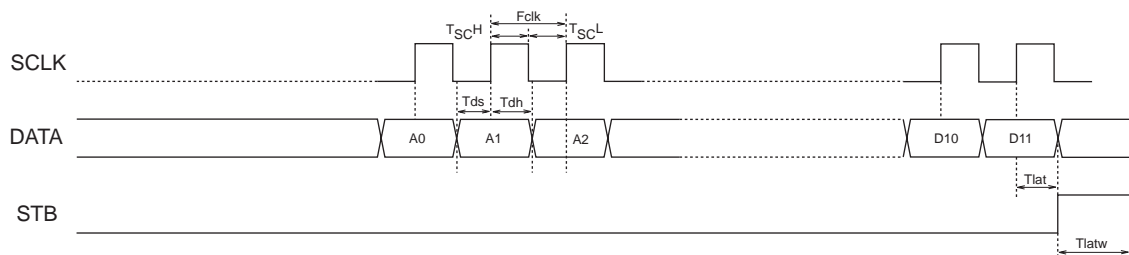
Block Diagram



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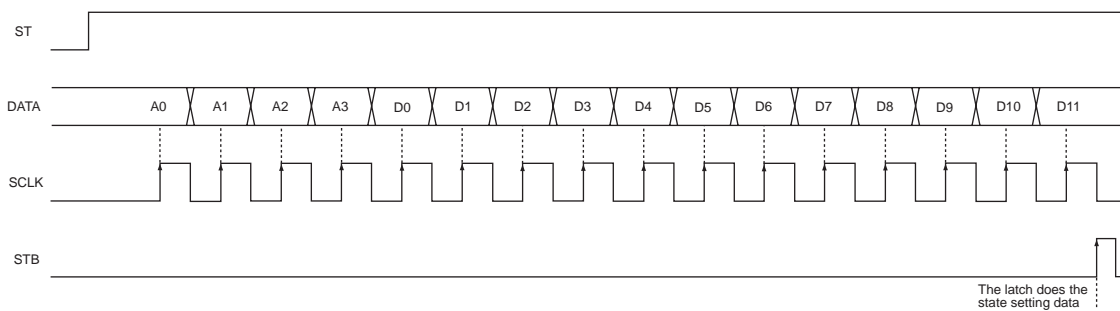
3 line serial communication electrical Characteristics at Ta = 25°C, VCC = 3.3V, VM = 5.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Serial data forwarding pin						
Logic pin input current	I _{INL}	V _{IN} =0V(SCLK, DATA, STB)			1.0	μA
	I _{INH}	V _{IN} =3.3V(SCLK, DATA, STB)		33	50	V
Input "H" level voltage	V _{INH}	SCLK, DATA, STB	2.5			V
Input "L" level voltage	V _{INL}	SCLK, DATA, STB			1.0	μS
Minimum SCLK "H" pulse width	T _{SC_H}		0.1			μS
Minimum SCLK "L" pulse width	T _{SC_L}		0.1			μS
STB regulation time	T _{lat}		0.1			μS
Minimum STB pulse width	T _{latw}		0.1			μS
Data set-up time	T _{ds}		0.1			μS
Data hold time	T _{dh}		0.1			μS
maximum CLK frequency	F _{clk}				4	MHz



Serial data timing condition

Serial data input timing chart



It inputs it from A0 in order of D11. The data transfer is done by the rising edge, and after all data transfers, the latch does all data to SCLK by the STB signal standing up. The STB signal accepts and the internal logic of IC doesn't accept the SCLK signal during "H".

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Serial logic map

PWMh - bridge relation serial map

				Input												Setting mode	Set content	Remarks			
A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11						
0	0	0	0	*	*	0	0	0	0	0	0	0	0	0	0	0	1ch PWM Duty set	100%	Reverse		
				*	*	1	0	0	0	0	0	0	0	0	0	0		0		511/512 × 100%	
				*	*	0	1	0	0	0	0	0	0	0	0	0		0		510/512 × 100%	
				*	*	0	1	1	1	1	1	1	1	1	1	1		0		...	2/512 × 100%
				*	*	1	1	1	1	1	1	1	1	1	1	1		0		1/512 × 100%	
				*	*	0	0	0	0	0	0	0	0	0	0	0		1		0%	Middle point
				*	*	1	0	0	0	0	0	0	0	0	0	0		1	1/512 × 100%	Normal rotation	
				*	*	0	1	0	0	0	0	0	0	0	0	0		1	2/512 × 100%		
				*	*	1	0	1	1	1	1	1	1	1	1	1		1	...		509/512 × 100%
				*	*	0	1	1	1	1	1	1	1	1	1	1		1	510/512 × 100%		
				*	*	1	1	1	1	1	1	1	1	1	1	1		1	511/512 × 100%		
				*	*	1	1	1	1	1	1	1	1	1	1	1		1	511/512 × 100%		
1	0	0	0	*	*	0	0	0	0	0	0	0	0	0	0	2ch PWM Duty set	100%	Reverse			
				*	*	1	0	0	0	0	0	0	0	0	0		0		511/512 × 100%		
				*	*	0	1	0	0	0	0	0	0	0	0		0		510/512 × 100%		
				*	*	0	1	1	1	1	1	1	1	1	1		0		...	2/512 × 100%	
				*	*	1	1	1	1	1	1	1	1	1	1		0		1/512 × 100%		
				*	*	0	0	0	0	0	0	0	0	0	0		1		0%	Middle point	
				*	*	1	0	0	0	0	0	0	0	0	0		1	1/512 × 100%	Normal rotation		
				*	*	0	1	0	0	0	0	0	0	0	0		1	2/512 × 100%			
				*	*	1	0	1	1	1	1	1	1	1	1		1	...		509/512 × 100%	
				*	*	0	1	1	1	1	1	1	1	1	1		1	510/512 × 100%			
				*	*	1	1	1	1	1	1	1	1	1	1		1	511/512 × 100%			
				*	*	1	1	1	1	1	1	1	1	1	1		1	511/512 × 100%			
0	1	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*	1ch hall bias set (8bit DAC)	0V			
				1	0	0	0	0	0	0	0	0	*	*	*	*		1/255 × VREF			
				0	1	0	0	0	0	0	0	0	*	*	*	*		2/255 × VREF			
				*	*	*	*	*	*	*	*	*	*	*	*	*		...			
				1	0	1	1	1	1	1	1	1	*	*	*	*		253/255 × VREF			
				0	1	1	1	1	1	1	1	1	*	*	*	*		254/255 × VREF			
				1	1	1	1	1	1	1	1	1	*	*	*	*		VREF			
1	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*	2ch hall bias set (8bit DAC)	0V				
				1	0	0	0	0	0	0	0	*	*	*	*		1/255 × VREF				
				0	1	0	0	0	0	0	0	0	*	*	*		*	2/255 × VREF			
				*	*	*	*	*	*	*	*	*	*	*	*		*	...			
				1	0	1	1	1	1	1	1	1	*	*	*		*	253/255 × VREF			
				0	1	1	1	1	1	1	1	1	*	*	*		*	254/255 × VREF			
				1	1	1	1	1	1	1	1	1	*	*	*		*	VREF			
0	0	1	0	0	0	0	0	0	0	0	0	*	*	*	*	1ch hall amplifier offset adjustment (8bit DAC)	0V				
				1	0	0	0	0	0	0	0	*	*	*	*		1/255 × V _{CC}				
				0	1	0	0	0	0	0	0	0	*	*	*		*	2/255 × V _{CC}			
				*	*	*	*	*	*	*	*	*	*	*	*		*	...			
				1	0	1	1	1	1	1	1	1	*	*	*		*	253/255 × V _{CC}			
				0	1	1	1	1	1	1	1	1	*	*	*		*	254/255 × V _{CC}			
				1	1	1	1	1	1	1	1	1	*	*	*		*	V _{CC}			
1	0	1	0	0	0	0	0	0	0	0	0	*	*	*	*	2ch hall amplifier offset adjustment (8bit DAC)	0V				
				1	0	0	0	0	0	0	0	*	*	*	*		1/255 × V _{CC}				
				0	1	0	0	0	0	0	0	0	*	*	*		*	2/255 × V _{CC}			
				*	*	*	*	*	*	*	*	*	*	*	*		*	...			
				1	0	1	1	1	1	1	1	1	*	*	*		*	253/255 × V _{CC}			
				0	1	1	1	1	1	1	1	1	*	*	*		*	254/255 × V _{CC}			
				1	1	1	1	1	1	1	1	1	*	*	*		*	V _{CC}			

The PWMh-bridge driver's ON/OFF operation is done with the ST pin.

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Hall amplifier gain setting range

Hall amplifier relation serial map

Input								Setting mode	Hall amplifier magnification (Inside: Resistance)
A0	A1	A2	A3	D0	D1	D2	D3		
0	0	0	1	0	0	0	0	1ch hall amplifier gain setting (“3” Resistance ÷ “2” Resistance)	10 (36k//3.6k)
				1	0	0	0		20 (72k//3.6k)
				0	1	0	0		40 (144k//3.6k)
				1	1	0	0		50 (180k//3.6k)
				0	0	1	0		60 (216k//3.6k)
				1	0	1	0		70 (252k//3.6k)
				0	1	1	0		90 (324k//3.6k)
				1	1	1	0		100 (360k//3.6k)
				0	0	0	1		110 (396k//3.6k)
				1	0	0	1		120 (432k//3.6K)
				0	1	0	1		140 (504k//3.6k)
				1	1	0	1		150 (540k//3.6k)
				0	0	1	1		160 (570k//3.6k)
				1	0	1	1		170 (612k//3.6k)
				0	1	1	1		190 (684k//3.6k)
				1	1	1	1		200 (720k//3.6k)
1	0	0	1	0	0	0	0	2ch hall amplifier gain setting (“3” Resistance ÷ “2” Resistance)	10 (36k//3.6k)
				1	0	0	0		20 (72k//3.6k)
				0	1	0	0		40 (144k//3.6k)
				1	1	0	0		50 (180k//3.6k)
				0	0	1	0		60 (216k//3.6k)
				1	0	1	0		70 (252k//3.6k)
				0	1	1	0		90 (324k//3.6k)
				1	1	1	0		100 (360k//3.6k)
				0	0	0	1		110 (396k//3.6k)
				1	0	0	1		120 (432k//3.6K)
				0	1	0	1		140 (504k//3.6k)
				1	1	0	1		150 (540k//3.6k)
				0	0	1	1		160 (570k//3.6k)
				1	0	1	1		170 (612k//3.6k)
				0	1	1	1		190 (684k//3.6k)
				1	1	1	1		200 (720k//3.6k)
0	1	0	1	0	0	0	0	1ch hall amplifier offset resistance / input resistance (“1” Resistance ÷ “2” Resistance)	10 (36k//3.6k)
				1	0	0	0		20 (72k//3.6k)
				0	1	0	0		40 (144k//3.6k)
				1	1	0	0		50 (180k//3.6k)
				0	0	1	0		60 (216k//3.6k)
				1	0	1	0		70 (252k//3.6k)
				0	1	1	0		90 (324k//3.6k)
				1	1	1	0		100 (360k//3.6k)
				0	0	0	1		110 (396k//3.6k)
				1	0	0	1		120 (432k//3.6K)
				0	1	0	1		140 (504k//3.6k)
				1	1	0	1		150 (540k//3.6k)
				0	0	1	1		160 (570k//3.6k)
				1	0	1	1		170 (612k//3.6k)
				0	1	1	1		190 (684k//3.6k)
				1	1	1	1		200 (720k//3.6k)
1	1	0	1	0	0	0	0	2ch hall amplifier offset resistance / input resistance (“1” Resistance ÷ “2” Resistance)	10 (36k//3.6k)
				1	0	0	0		20 (72k//3.6k)
				0	1	0	0		40 (144k//3.6k)
				1	1	0	0		50 (180k//3.6k)
				0	0	1	0		60 (216k//3.6k)
				1	0	1	0		70 (252k//3.6k)
				0	1	1	0		90 (324k//3.6k)
				1	1	1	0		100 (360k//3.6k)
				0	0	0	1		110 (396k//3.6k)
				1	0	0	1		120 (432k//3.6K)
				0	1	0	1		140 (504k//3.6k)
				1	1	0	1		150 (540k//3.6k)
				0	0	1	1		160 (570k//3.6k)
				1	0	1	1		170 (612k//3.6k)
				0	1	1	1		190 (684k//3.6k)
				1	1	1	1		200 (720k//3.6k)

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General-purpose amplifier ON/OFF setting

Input						Setting mode	Set content	Remarks
A0	A1	A2	A3	D0	D1			
0	0	1	1	0	*	General-purpose amplifier 1	Stand-by	
				1	*		Operate	
				*	0	General-purpose amplifier 2	Stand-by	
				*	1		Operate	

PWM circuit accuracy setting

Input						Setting mode	Set content	Remarks
A0	A1	A2	A3	D0	D1			
1	0	1	1	0	0	PWM accuracy setting	10bit resolution	Initial value
				0	1		11bit resolution	
				1	0		12bit resolution	
				*	*		-	

PWM pulse width of moving

1ch (X axis side)

Input [3:0]								Setting mode	Moving pulse number
A0	A1	A2	A3	D0	D1	D2	D3		
0	1	1	1	0	0	0	0	1ch (X axis) side width of moving	0 (Initialization)
				1	0	0	0		1
				0	1	0	0		2
				1	1	0	0		3
				0	0	1	0		4
				1	0	1	0		5
				0	1	1	0		6
				1	1	1	0		7
				0	0	0	1		8
				1	0	0	1		9
				0	1	0	1		10
				1	1	0	1		11
				0	0	1	1		12
				1	0	1	1		13
				0	1	1	1		14
1	1	1	1	15					

Note : 1 pulse = 1CLK

2ch (Y axis side)

Input [7:4]								Setting mode	Moving pulse number
A0	A1	A2	A3	D4	D5	D6	D7		
0	1	1	1	0	0	0	0	2ch (Y axis) side width of moving	0 (Initialization)
				1	0	0	0		1
				0	1	0	0		2
				1	1	0	0		3
				0	0	1	0		4
				1	0	1	0		5
				0	1	1	0		6
				1	1	1	0		7
				0	0	0	1		8
				1	0	0	1		9
				0	1	0	1		10
				1	1	0	1		11
				0	0	1	1		12
				1	0	1	1		13
				0	1	1	1		14
1	1	1	1	15					

Note : 1 pulse = 1CLK

The ON/OFF operation of the hall amplifier and the hall bias is done with the ST pin.

Note : An initial value of A0 to A3 = 1111 is a static test mode. Use it specifying data D0 for one.

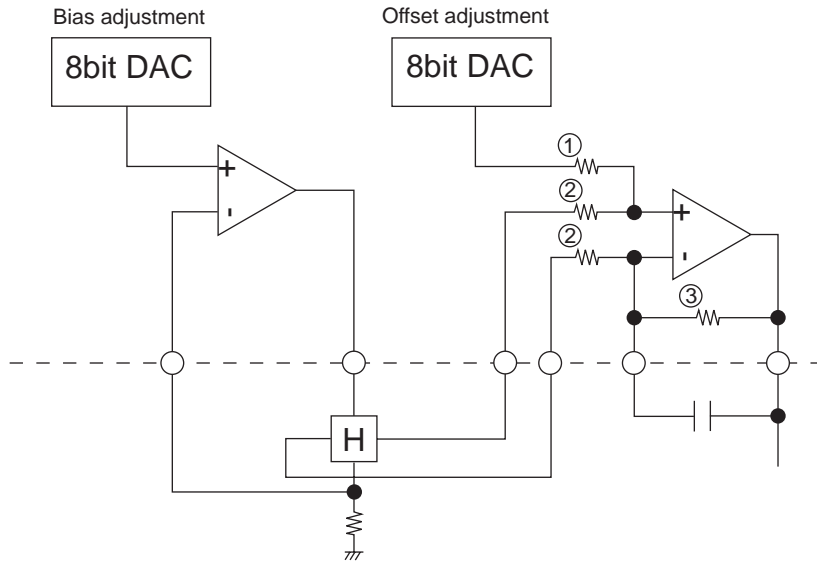
TEST mode setting

Input					Setting mode	Content	Remarks
A0	A1	A2	A3	D0			
1	1	1	1	0	NC pin _ TEST mode	External CLK	It uses it by the shipment inspection.
				1		Internal CLK	

Note : External CLK mode is for the shipment inspection. Use it with internal CLK. Use it after it internal CLK switches because default is external CLK mode.

LV8415CB

Hall bias, Offset adjustment circuit configuration



Hall amplifier, Hall bias equivalent circuit

About the gain adjustment

The resistance ratio of "2" and "3" is adjusted in figure and the gain is set. Refer to the setting to the cereal map. The magnification can be set from ten by 200.

About the Offset adjustment

The resistance ratio of "1" and "2" is adjusted in figure and the Offset is set. Refer to the setting to the cereal map. The magnification can be set from ten by 200.

Note in design

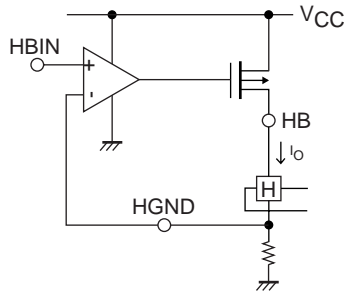
- Stand-by function

IC becomes a stand-by state at ST = "L", and IC enters the state of operation at ST = "H". Moreover, the register in IC is reset as for ST = "L" at times.

- Hall bias

The constant current output is built into for the hall element drive. The constant current value is set from detection resistance (RHG) connected from the HBIN pin impression voltage and the HGND pin between GND.

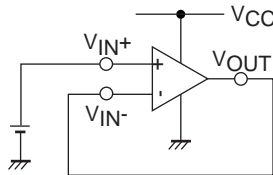
Constant current value (I_O) = HBIN voltage ÷ Detection resistance



Constant current value (I_O) becomes about 1mA when assuming HBIN pin impressed voltage = 1.0V and detection resistance = 1 k Ω from the above-mentioned calculation type. Moreover, the HGND pin must connect with the HB pin, and connect the detection resistance of a large value as much as possible when you do not use the hall bias circuit.

- Operation amplifier

Impress the bias to the V_{IN+} pin, and compose the buffer by the connection to the VOUT pin in the V_{IN-} pin in the operational amplifier not used.



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