SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV8481CS — Saturated Driver with 2 channels + Constant Current Driver

Overview

The LV8481CS is low-voltage motor driver with a saturated driver with 2 channels + constant current driver. Since it is in wafer level package, this IC is optimized for the stepping motor driver and shutter driver of various portable equipments including the mobile phones with camera.

Functions

- Saturated driver H bridge with 2 channels + Constant current driver.
- I^2C bus interface
- Built-in AF stepping motor sequence logic (enabling 2-phase excitation and 1-2 phase excitation)
- Built-in lens home position sequence logic
- Enabling power-saving by MOS process
- Built-in 4 bit DAC for constant current
- Built-in constant current detection resistance
- Wafer level package. WLP10 (0.97mm × 2.47mm × 0.5mmt)
- Built-in thermal shutdown circuit and LVS circuit.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}, VM max		5.0	V
Output applied voltage	V_{OUT} max	OUT1, OUT2, OUT3, OUT4, OUT5	5.0	V
Input applied voltage	V_{IN} max	ENA, SCL, SDA	-0.3 to +5.0	V
GND pin flow-out current	IGND	Per channel	400	mA
Allowable power dissipation	Pd max	With specified substrate *	550	mW
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-40 to +150	°C

* Specified substrate : 50.0mm × 50.0mm ×1.6mm, glass epoxy 1 layers printed circuit board

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LV8481CS

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.4 to 4.5	V
High level input voltage	V_{IH}	ENA, SCL and SDA	$0.4 \times V_{CC}$ to	V
Low level input voltage	V_{IL}		to $V_{CC} \times 0.13$	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 2.8V

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Supply current	I_{CCO}	EN = 0V		0.1	1	uA
	$I_{CCO}1$	EN = 3V		1.2	1.8	mA
Output ON resistance 1 (out1 to out3)	Ron11	V_{CC} = 3.0V (Sum of the upper and lower side outputs) EN = 3.0V, I_{OUT} = 100mA		2.7	3.3	Ω
	Ron12	V_{CC} = 4.5V (Sum of the upper and lower side outputs) EN = 3.0V, I_{OUT} = 100mA		2.1	2.6	Ω
Output ON resistance 2 (out4 to out5 + sence R)	Ron21	V_{CC} = 3.0V (Sum of the upper and lower side outputs + RF (0.5Ω)) EN = 3.0V, I_{OUT} = 100mA		2.7	3.2	Ω
	Ron22	V_{CC} = 4.5V (Sum of the upper and lower side outputs + RF (0.5Ω)) EN = 3.0V, I_{OUT} = 100mA		2.1	2.55	Ω
Output constant current DAC1	$I_{OUT}1$	D3-D0code : 0000		260		mA
Output constant current DAC2	$I_{OUT}2$	D3-D0code : 0001		250		mA
Output constant current DAC3	$I_{OUT}3$	D3-D0code : 0010		240		mA
Output constant current DAC4	$I_{OUT}4$	D3-D0code : 0011		230		mA
Output constant current DAC5	$I_{OUT}5$	D3-D0code : 0100		220		mA
Output constant current DAC6	$I_{OUT}6$	D3-D0code : 0101		210		mA
Output constant current DAC7	$I_{OUT}7$	D3-D0code : 0110		200		mA
Output constant current DAC8	$I_{OUT}8$	D3-D0code : 0111		190		mA
Output constant current DAC9	$I_{OUT}9$	D3-D0code : 1000		180		mA
Output constant current DAC10	$I_{OUT}10$	D3-D0code : 1001		170		mA
Output constant current DAC11	$I_{OUT}11$	D3-D0code : 1010		160		mA
Output constant current DAC12	$I_{OUT}12$	D3-D0code : 1011		150		mA
Output constant current DAC13	$I_{OUT}13$	D3-D0code : 1100		140		mA
Output constant current DAC14	$I_{OUT}14$	D3-D0code : 1101		130		mA
Output constant current DAC15	$I_{OUT}15$	D3-D0code : 1110		120		mA
Output constant current DAC16	$I_{OUT}16$	D3-D0code : 1111		110		mA
Output turn ON time	Traise	OUT1-OUT4		1	3	us
Output turn OFF time	Tfall	OUT1-OUT4		0.2	1	us
AF PLS period	Taf		1.8	2	2.2	ms
Input curren	I_{IN}	V_{IN} = 3V		0	1	uA
SDA pin low level output	V_{OL}	I_O = 300uA		0.2	0.3	V
Time of onset of movements after receiving I²C communication	TI²CSH	I²C comand SH operation			10	us
	TI²CAF	I²C comand AF sequence operation			1.2	ms
	TI²CDP	I²C comand Defaultposition sequence operation			6	ms
Thermal shut down operation temperature	TTSD	ENA = 3V Design target value		175		°C
Hysteresis	TΔTSD	ENA = 3V Design target value		35		°C

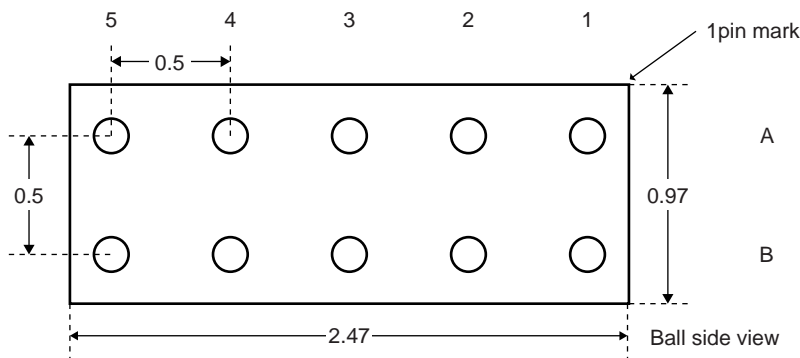(Assured design target) * : Design target value, not to be measured at production test.
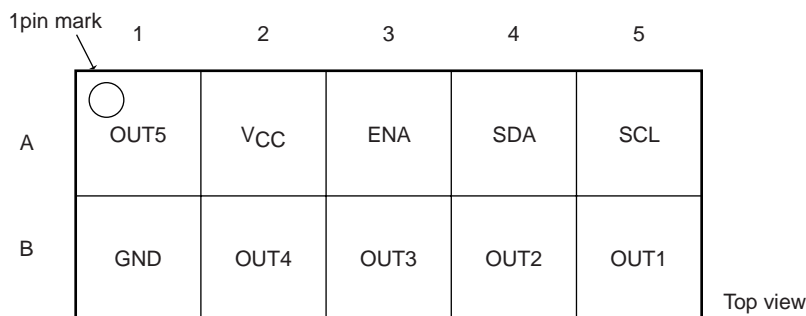
Package Dimensions

unit : mm (typ)

3362

TOP VIEW   SIDE VIEW   BOTTOM VIEW

2.47

0.97

0.235

5   4   3   2   1

Ø 0.27   0.5   0.235

0.5

SIDE VIEW

0.5 MAX

0.14

SANYO : WLP10(2.47X0.97)

Pd max – Ta

Specified board:$50.0 \times 50.0 \times 1.6mm^3$
glass epoxy

0.55

0.29

Allowable power dissipation, Pd max - W

Ambient temperature, Ta - °C

Pin Assignment

5   4   3   2   1   1pin mark

0.5

A

0.5

0.97

B

2.47   Ball side view

1pin mark

	1	2	3	4	5
A	OUT5	V_{CC}	ENA	SDA	SCL
B	GND	OUT4	OUT3	OUT2	OUT1

Top view
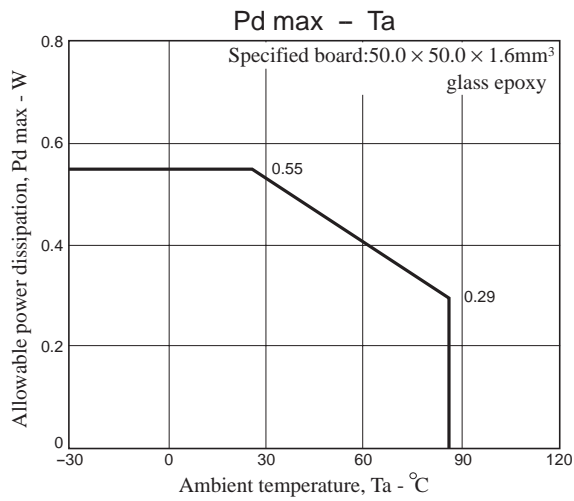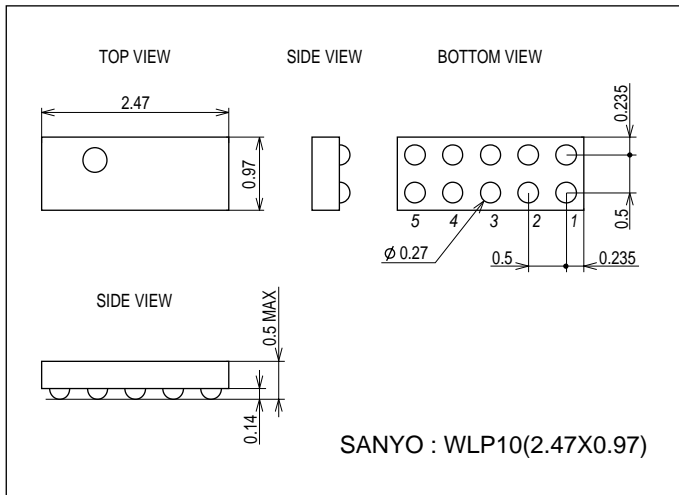
Pin No.	Pin Name
A1	OUT5
A2	V_{CC}
A3	ENA
A4	SDA
A5	SCL
B1	GND
B2	OUT4
B3	OUT3
B4	OUT2
B5	OUT1

Block Diagram
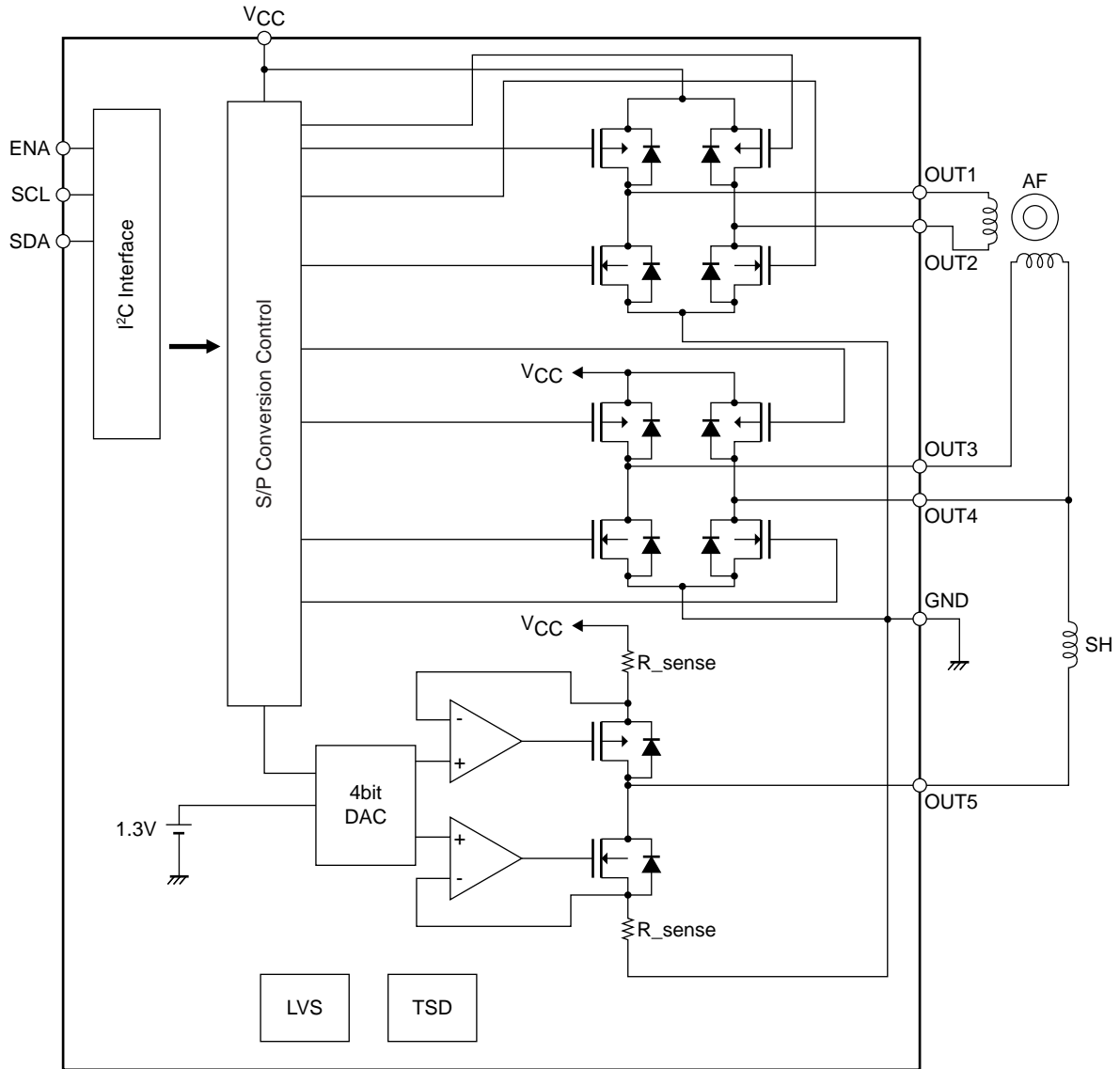
Serial Bus Communication Specifications

I^2C serial transfer timing conditions

Standard mode

Start condition   Resend start condition   Stop condition

Input waveform condition
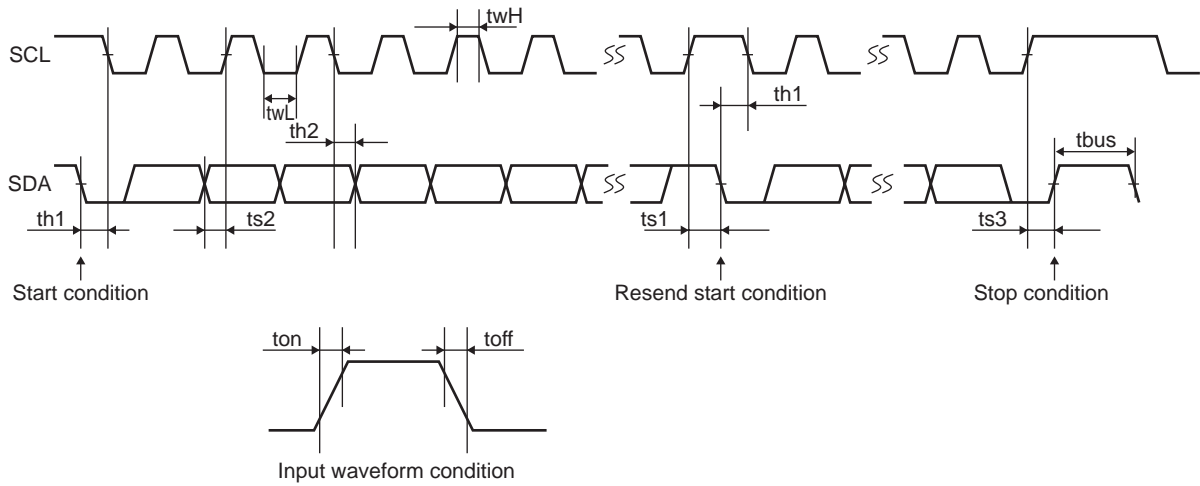
Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7			us
	ts2	Setup time of SDA with respect to the rising edge of SCL	250			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0			us
Data hold time	th1	Hold time of SDA with respect to the falling edge of SDA	4.0			us
	th2	Hold time of SDA with respect to the falling edge of SCL	0			us
Pulse width	twL	SCL low period pulse width	4.7			us
	twH	SCL high period pulse width	4.0			us
Input waveform conditions	ton	SCL, SDA (input) rising time			1000	ns
	toff	SCL, SDA (input) falling time			300	ns
Bus free time	tbus	Interval between stop condition and start condition	4.7			us

High-speed mode

| Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6			us
	ts2	Setup time of SDA with respect to the rising edge of SCL	100			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6			us
Data hold time	th1	Hold time of SDA with respect to the falling edge of SDA	0.6			us
	th2	Hold time of SDA with respect to the falling edge of SCL	0.08			us
Pulse width	twL	SCL low period pulse width	1.3			us
	twH	SCL high period pulse width	0.6			us
Input waveform conditions	ton	SCL, SDA (input) rising time			300	ns
	toff	SCL, SDA (input) falling time			300	ns
Bus free time	tbus	Interval between stop condition and start condition	1.3			us

I²C bus transmission method

Start and stop conditions

The I²C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.
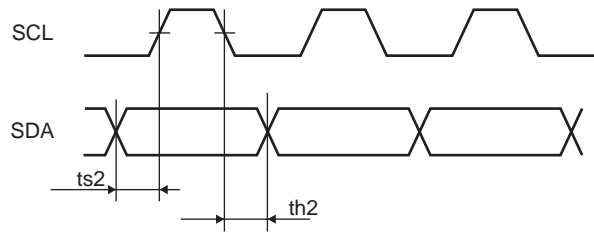
When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.

Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.
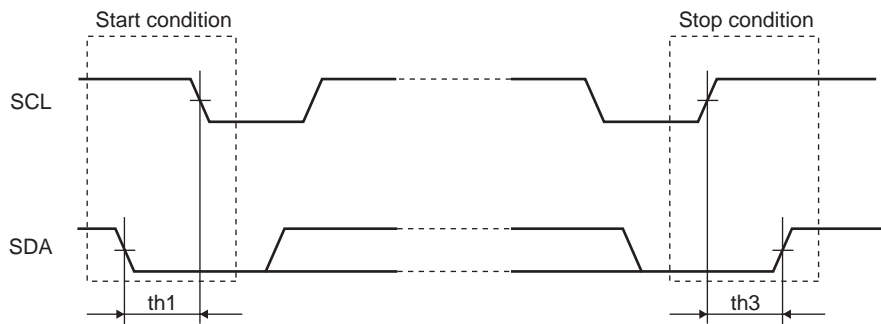

Data transfer and acknowledgement response

After the start condition has been generated, the data is transferred one byte (8 bits) at a time. Generally, in an I²C bus, a unique 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) indicating the transfer direction of the subsequent data.

Every time 8 bits of data for each byte are transferred, the ACK signal is sent from the receiving end to the sending end. Immediately after the clock pulse of SCL bit 8 in the data transferred has fallen to low, SDA at the sending end is released, and SDA is set to low at the receiving end, causing the ACK signal to be sent.

When, after the receiving end has sent the ACK signal, the transfer of the next byte remains in the receiving status, the receiving end releases SDA at the falling edge of the ninth SCL clock.
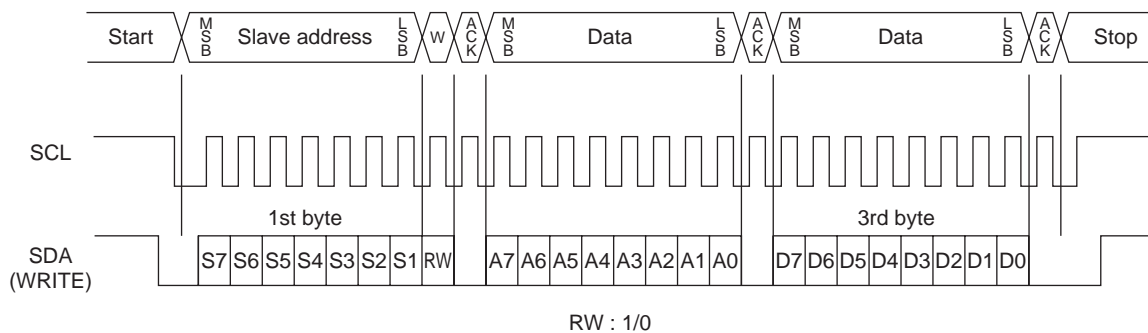
Number of Slave Address is 0110010. (S7→S1)

Serial Map

	Register Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	AFMODE [7 : 0]							
									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1	FL	×	AFMODE [5 : 3]			HOLD time set [2 : 0]		
									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	0	×	×	×	×	×	SHMODE [2 : 0]		
1									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	1	×	×	×	×	CURRENTMODE [3 : 0]			
									0	0	0	0	0	0	0	0

Upper : Register name   Lower : Default value

*Caution : address 00000111 is IC testmode. This address is out of use.

Serial Each Mode Settings

Rotational Direction Setting

0	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

D0	Rotational direction
0	CW
1	CCW

AF ON/OFF Setting

0	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

D1	ON/OFF
0	Standby mode
1	Operation mode

AF counter Reset

0	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

D2	Counter Reset
0	Reset on
1	Reset off

Step Number Setting

0	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7 (32P)	D6 (16P)	D5 (8P)	D4 (4P)	D3 (2P)	Number of steps
0	0	0	0	0	2step
0	0	0	0	1	4step
0	0	0	1	0	6step
0	0	0	1	1	8step
0	0	1	0	0	10step
0	0	1	0	1	12step
0	0	1	1	0	14step
0	0	1	1	1	16step
0	1	0	0	0	18step
0	1	0	0	1	20step
0	1	0	1	0	22step
0	1	0	1	1	24step
0	1	1	0	0	26step
0	1	1	0	1	28step
0	1	1	1	0	30step
0	1	1	1	1	32step
1	0	0	0	0	34step
1	0	0	0	1	36step
1	0	0	1	0	38step
1	0	0	1	1	40step
1	0	1	0	0	42step
1	0	1	0	1	44step
1	0	1	1	0	46step
1	0	1	1	1	48step
1	1	0	0	0	50step
1	1	0	0	1	52step
1	1	0	1	0	54step
1	1	0	1	1	56step
1	1	1	0	0	58step
1	1	1	0	1	60step
1	1	1	1	0	62step
1	1	1	1	1	64step

Note):

D3 : 2Pulse   on/off (2step) setting register
D4 : 4Pulse   on/off (4step) setting register
D5 : 8Pulse   on/off (8step) setting register
D6 : 16Pulse   on/off (16step) setting register
D7 : 32Pulse   on/off (32step) setting register

AF HOLDTIME Setting

0	0	0	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0

D2	D1	D0	HOLD PULSE Number 1 (at AF sequence)	HOLD PULSE Number (at Default position sequence)
0	0	0	1Puls (2msec/1msec)	1Puls (10msec/5msec)
0	0	1	2Puls (4msec/2msec)	2Puls (20msec/10msec)
0	1	0	4Puls (8msec/4msec)	4Puls (40msec/20msec)
0	1	1	5Puls (10msec/5msec)	5Puls (50msec/25msec)
1	0	0	8Puls (16msec/8msec)	8Puls (80msec/40msec)
1	0	1	16Puls (32msec/16msec)	16Puls (160msec/80msec)
1	1	0	32Puls (64msec/32msec)	32Puls (320msec/160msec)
1	1	1	1Puls (2msec/1msec)	1Puls (10msec/5msec)

Note) : HOLDTIME value make a written (2-phase excitation/1-2 phase excitation).

AF Excitation Setting

0	0	0	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0

D3	Excitation system
0	2-phase excitation
1	1-2 phase excitation

Default position sequence setting

0	0	0	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0

D4	ON/OFF
0	Off
1	Default position sequence ON

Default position and AF sequence + steps Setting

0	0	0	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0

D5	+64step (on/off)
0	Off
1	+64step

Further note : When the pulses of 64 steps or more in total are set in Default position sequence and AF sequence and the flag of D5 is "1", the pulse of the number of AFsteps + 64steps can be set.

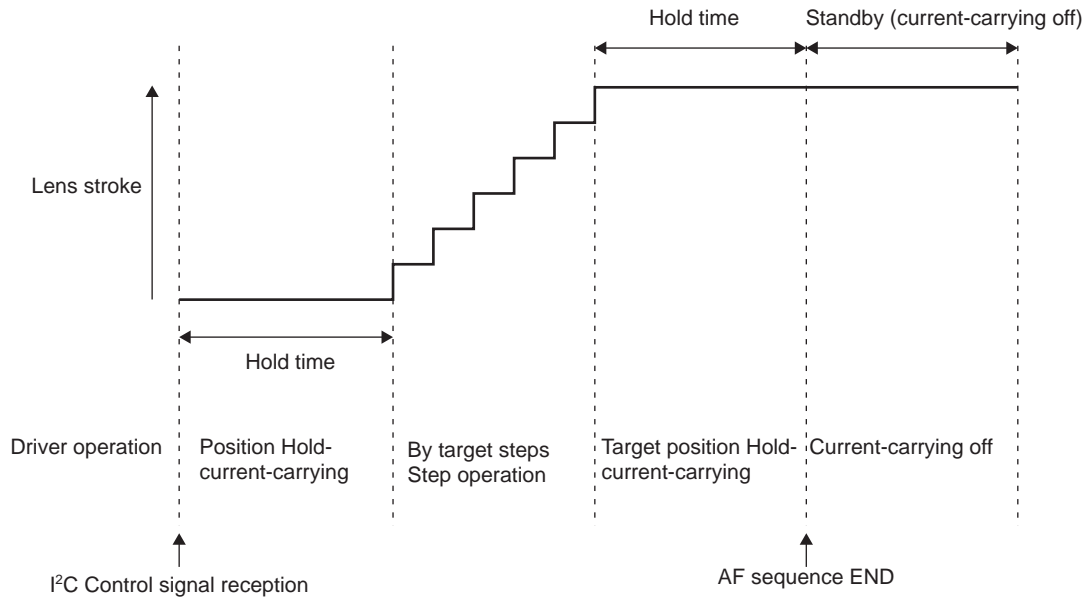## AF sequence and Default position sequence Flag

0	0	0	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0

The situation between Standby state and Under execution of the sequences AF and Default position can be confirmedin the state of "D7".

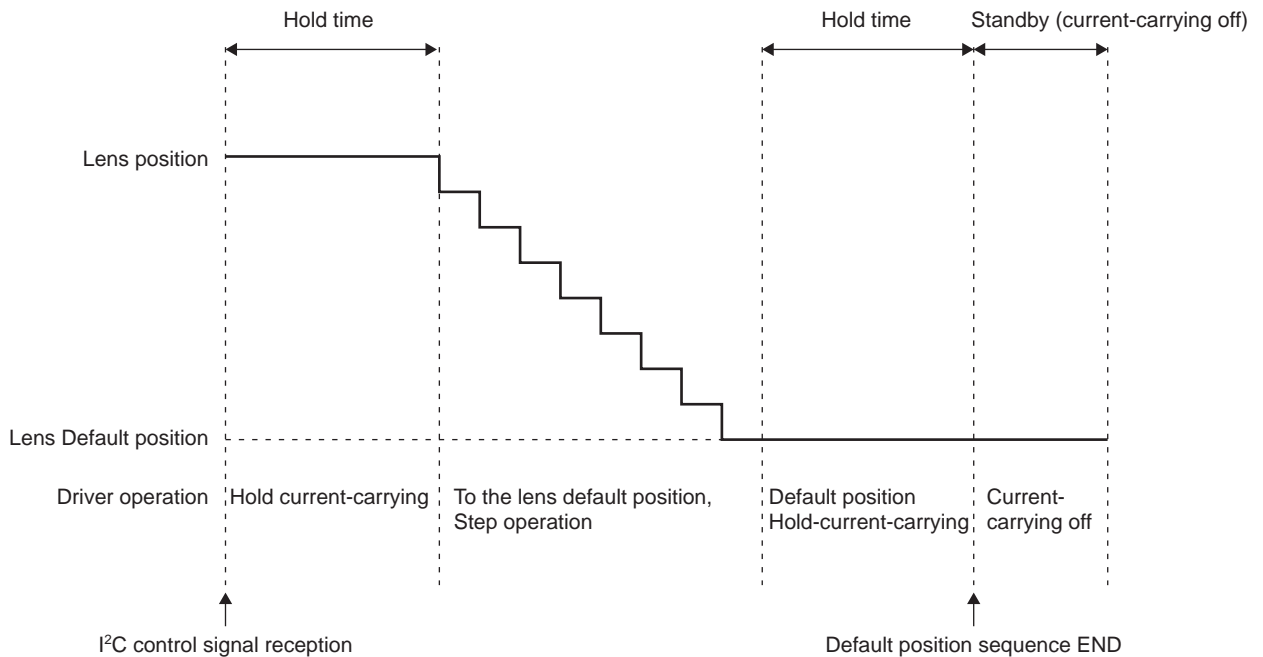| D7	FL
0	Standby state
1	Under execution

When the sequence ends, FL automatically becomes zero.

AF sequence diagram

(1) Set default value at OUT1 = H, OUT2 = L, OUT3 = H and OUT4 = L.
(2) STMspeed at the AF sequence becomes 500pps.
(3) The hold current-carrying time, it is the same time both front and rear times.

Default Position Sequence diagram

Further note : (1) When the flag of D4 in the address 00000001 of a default position sequence is "1", whether or not the total of a default position sequence is 65step or more is set by using a flag in D5.
The command is transmitted by the I²C communication after setting HOLD time.

(2) The number of step, the rotational direction and AFon/off are set in the address 00000000. And, a default position sequence is performed at the IC side when the data is transmitted by using I2C communication.

(3) STMspeed in a default position sequence becomes 100pps.

(4) Hold current-carrying time, it becomes congruent with the previous or nest time.

SH bridge, OUT4 to 5 Operation Setting

1	0	0	0	0	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0

D1	D0	OUT4	OUT5	Bridge state
0	0	Z	Z	Standby All channels OFF
0	1	H	L	Constant current between OUT4 and OUT5
1	0	L	H	Constant current between OUT5 and OUT4
1	1	L	L	Brake Logic

• Constant current is driven When applying current between channels OUT4 and OUT5.

SH bridge, on/off Setting

1	0	0	0	0	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0

D2	ON/OFF
0	Standby
1	Operation

Constant Current Setting

1	0	0	0	0	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

D3	D2	D1	D0	Constant current value
0	0	0	0	260mA
0	0	0	1	250mA
0	0	1	0	240mA
0	0	1	1	230mA
0	1	0	0	220mA
0	1	0	1	210mA
0	1	1	0	200mA
0	1	1	1	190mA
1	0	0	0	180mA
1	0	0	1	170mA
1	0	1	0	160mA
1	0	1	1	150mA
1	1	0	0	140mA
1	1	0	1	130mA
1	1	1	0	120mA
1	1	1	1	110mA

AF sequence (2-phase excitation drive) (1 cycle = 4CLK)

AF sequence a→b→c→d→a (Clockwise direction)
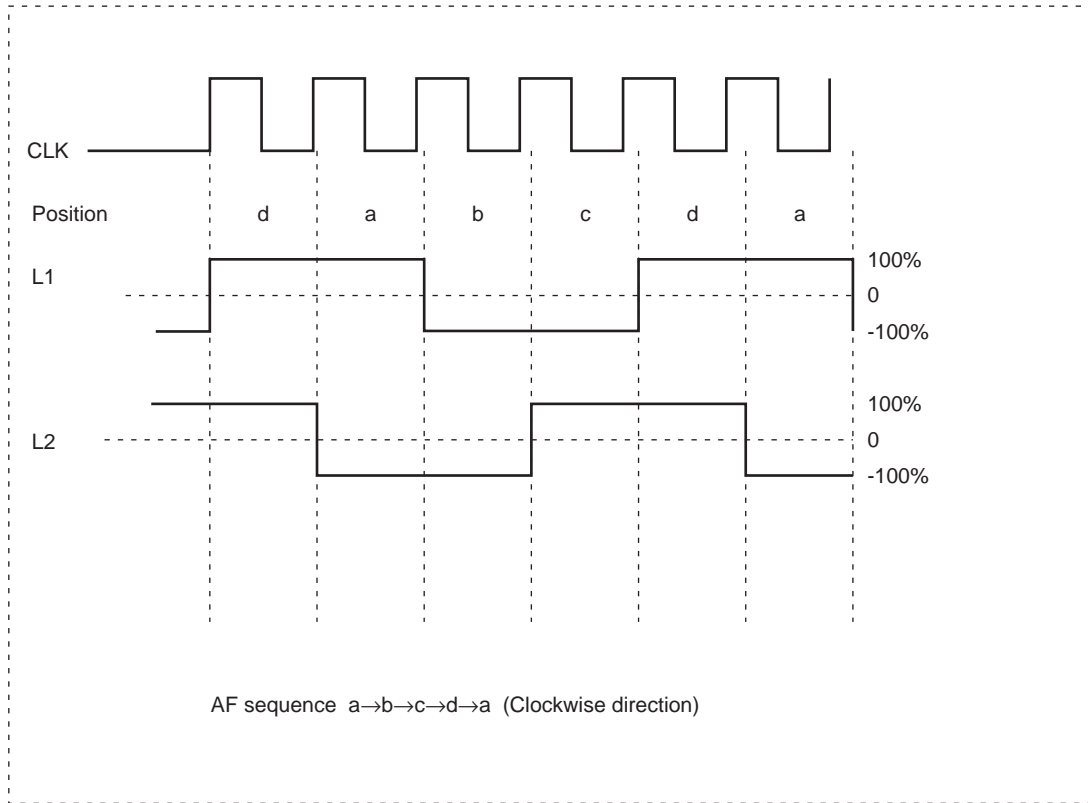
AF sequence (1-2 phase excitation drive) (1 cycle = 8CLK)

AF sequence a→b→c→d→e→f→g→h→a (Clockwise direction)