Ordering number : ENA1609

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV8483CS — For Camera Modules Composite Channel Lens Driver

Overview

LV8483CS is a constant current driver IC for voice coil motors (VCM) that includes a constant current 1.5-channel driver. It uses an ultraminiature wafer level package (WLP), which makes the IC ideal for VCM motor, shutter (SH), and iris (IR) drivers used in a wide variety of portable equipment including camera cell phones.

Functions

- Constant current driver for AF VCM + constant current 1.5-channel H-bridge driver for SH and IR
- I^2C bus interface
- Low power consumption achieved using MOS process technologies
- Built-in 4-bit DAC for constant current operation (used for SH and IR H-bridges)
- Built-in 10-bit DAC for constant current control (used for AF VCM driver)
- Built-in constant current detection resistance
- Wafer level package. WLP10 (0.97mm × 2.47mm × 0.5mmt)
- Built-in thermal shutdown circuit and LVS circuit.
- AF VCM overshoot prevention function (current slope function)
- Built-in SH/IR control pin (energization timing control function using trigger input)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		5.0	V
Output applied voltage	V_{OUT} max	OUT1, OUT2, OUT3, OUT4	5.0	V
Input applied voltage	V_{IN} max	ENA, SCL, SDA, SH/IRTR	-0.3 to +5.0	V
GND pin flow-out current	IGND	Per channel	400	mA
Allowable power dissipation	Pd max	With specified substrate *	550	mW
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-40 to +150	°C

* Specified substrate : 50mm × 50mm × 1.6mm, glass epoxy 2-layer board

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.5 to 4.5	V
High level input voltage	V_{IH}	ENA, SCL, SDA and SH/IRTR	0.4 × V_{CC} to	V
Low level input voltage	V_{IL}		to V_{CC} × 0.13	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 2.8V

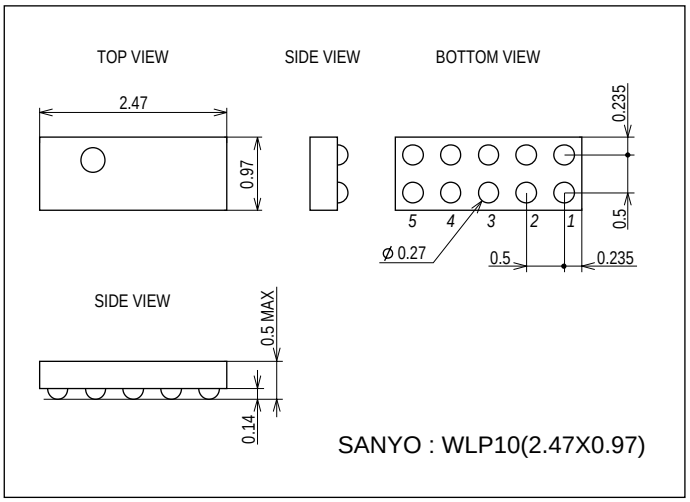
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I_{CCO}	ENA = L			1	μA
	$I_{CCO}1$	ENA = H		0.7	1	mA
Pin input current 1	$I_{IN}1$	ENA, SCL, SDA			1	μA
Pin input current 2	$I_{IN}2$	SH/IR TR		28		μA
V_{CC} low-voltage cutoff voltage	VthV_{CC}			2.0		V
Thermal shutdown temperature	TSD	Design target value		175		°C
Thermal hysteresis width	ΔTSD	Design target value		35		°C
Output ON resistance 1 (out1 + senceR)	Ron11	V_{CC} = 2.8V, I_{OUT} = 80mA (N-channel on-resistance + internal sensing resistor)		2.0	2.55	Ω
Output ON resistance 2 (out2 to out4 + senceR)	Ron21	V_{CC} = 2.8V, I_{OUT} = 80mA (upper side + lower side + internal sensing resistor)		2.4	2.95	Ω
	Ron22	V_{CC} = 4.5V, I_{OUT} = 100mA (upper side + lower side + internal sensing resistor)		2.0	2.4	Ω
AF DAC block						
Resolution				10		bit
Relative accuracy	INL				±4	LSB
Differential linearity	DNL				±1	LSB
Full code current	Ifull			100		mA
Error code current 0	Izero				1	μA
H bridge driver block						
Output constant current DAC1	$I_{OUT}1$	D3-D0code : 0000		260		mA
Output constant current DAC9	$I_{OUT}9$	D3-D0code : 1000		180		mA
Output constant current DAC16	$I_{OUT}16$	D3-D0code : 1111		110		mA
Energization time	TSH	D5-D4code : 00		10		ms
Output turn ON time	Traise	OUT2-OUT4		1	3	μs
Output turn OFF time	Tfall	OUT2-OUT4		0.2	1	μs
SDA pin low level output	V_{OL}	I_O = 300μA		0.2	0.3	V

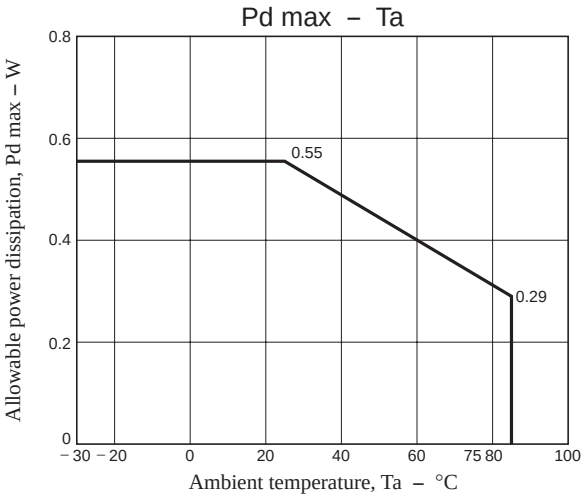
* Design guarantee value and no measurement is made.

Package Dimensions

unit : mm (typ)

3362



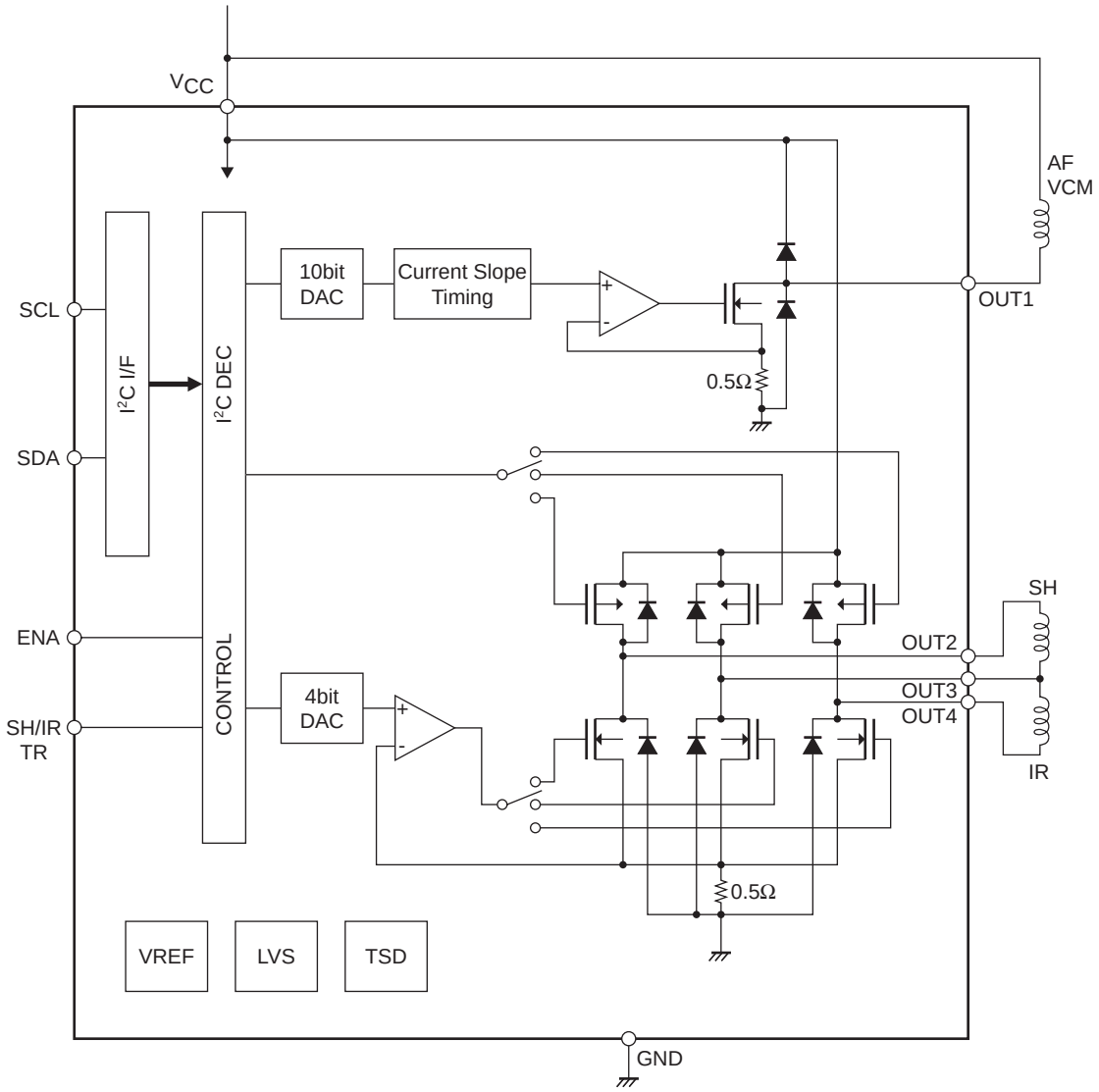


Pin Assignment

	1	2	3	4	5
A	SH/IR TR	V_{CC}	ENA	SDA	SCL
B	OUT4	OUT3	GND	OUT2	OUT1

Top view

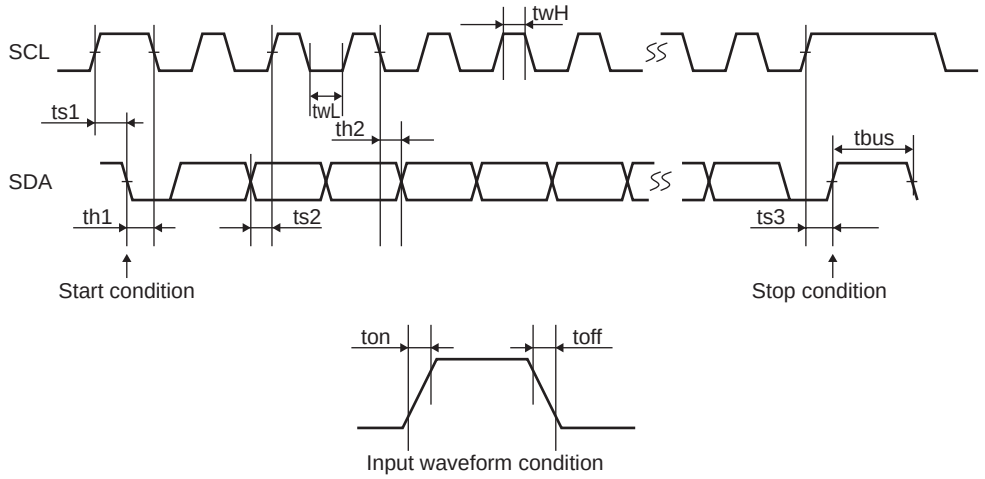
Block Diagram



Serial Bus Communication Specifications

I^2C serial transfer timing conditions

Standard mode



Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	250			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0			μs
Data hold time	th1	Hold time of SCL with respect to the falling edge of SDA	4.0			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			μs
Pulse width	twL	SCL low period pulse width	4.7			μs
	twH	SCL high period pulse width	4.0			μs
Input waveform conditions	ton	SCL, SDA rising time			1000	ns
	toff	SCL, SDA falling time			300	ns
Bus free time	tbus	Interval between stop condition and start condition	4.7			μs

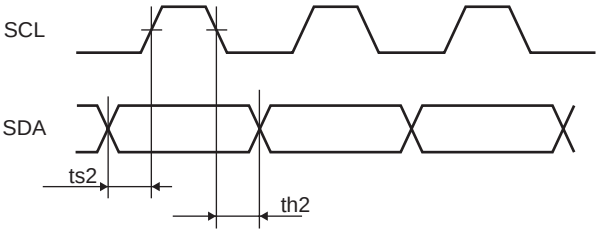
High-speed mode

Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	100			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6			μs
Data hold time	th1	Hold time of SCL with respect to the falling edge of SDA	0.6			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0			μs
Pulse width	twL	SCL low period pulse width	1.3			μs
	twH	SCL high period pulse width	0.6			μs
Input waveform conditions	ton	SCL, SDA (input) rising time			300	ns
	toff	SCL, SDA (input) falling time			300	ns
Bus free time	tbus	Interval between stop condition and start condition	1.3			μs

I²C bus transmission method

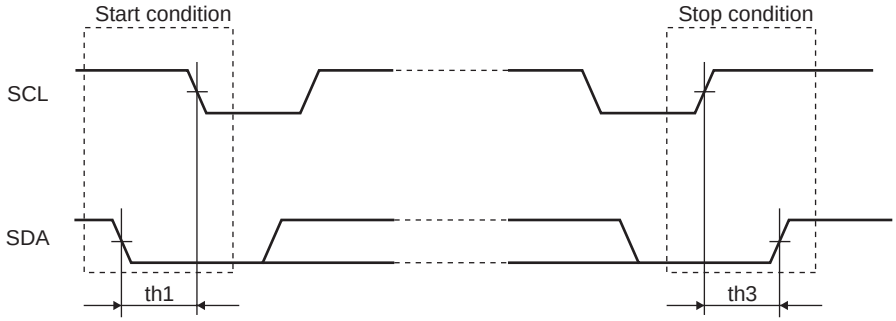
Start and stop conditions

The I²C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.



When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.

Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.



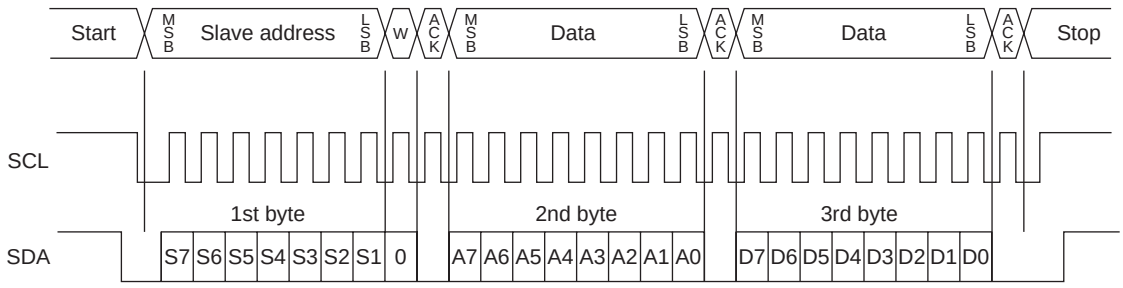
Data transfer and acknowledgement response

After the start condition has been generated, the data is transferred one byte (8 bits) at a time. Generally, in an I²C bus, a unique 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) indicating the transfer direction of the subsequent data.

Every time 8 bits of data for each byte are transferred, the ACK signal is sent from the receiving end to the sending end.

Immediately after the clock pulse of SCL bit 8 in the data transferred has fallen to low, SDA at the sending end is released, and SDA is set to low at the receiving end, causing the ACK signal to be sent.

When, after the receiving end has sent the ACK signal, the transfer of the next byte remains in the receiving status, the receiving end releases SDA at the falling edge of the ninth SCL clock.



Number of Slave Address is 0110011. (S7→S1)

Data transfer write format

The slave address and Write command must be allocated to the first byte and the register address in the serial map must be designated in the second byte.

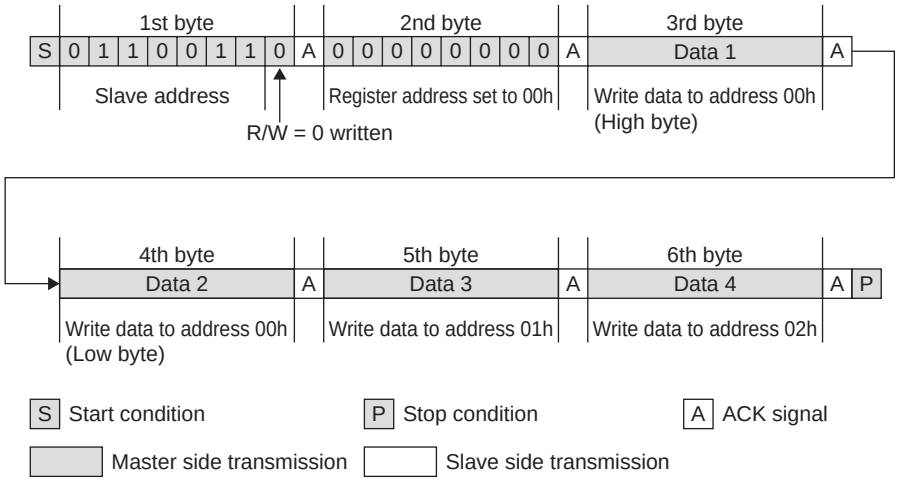
For the third byte, data transfer is carried out to the address designated by the register address which is written in the second byte. Subsequently, if data continues, the register address value is automatically incremented for the fourth and subsequent bytes. (*)

Thus, continuous data transfer starting at the designated address is made possible.

Since no auto incrementing occurs for address 02h and higher, it is necessary to send a stop condition after sending the data at address 02h.

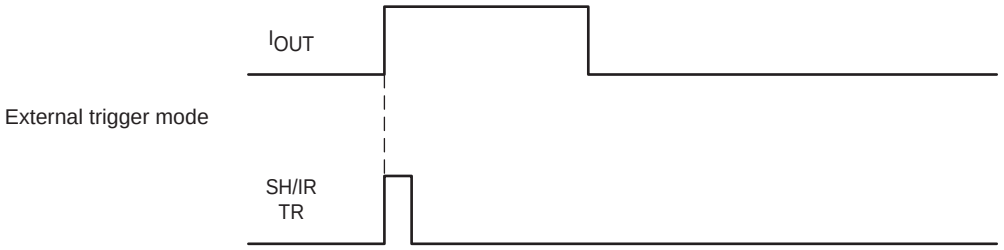
(*) Since 2-byte data is allocated to address 00h, when resister address 00h is specified in the second byte, the register address is auto-incremented to 01h after 2 bytes of data is sent.

Data write example

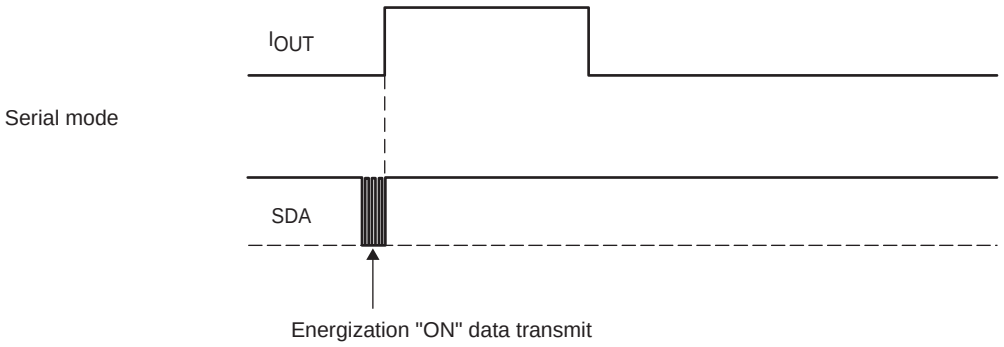


H-bridge Energization Timing Charts

Energization time : Internal setting mode · · · Energization is automatically stopped when the time that is selected from 10ms, 13ms, and 20ms expires.

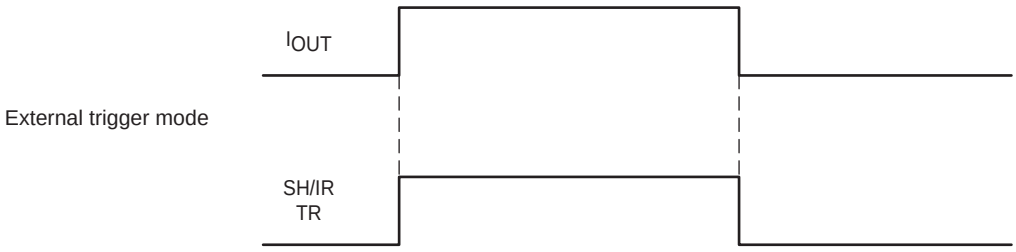


Energization starts on a rising edge of the SH/IR TR signal in the external trigger mode.

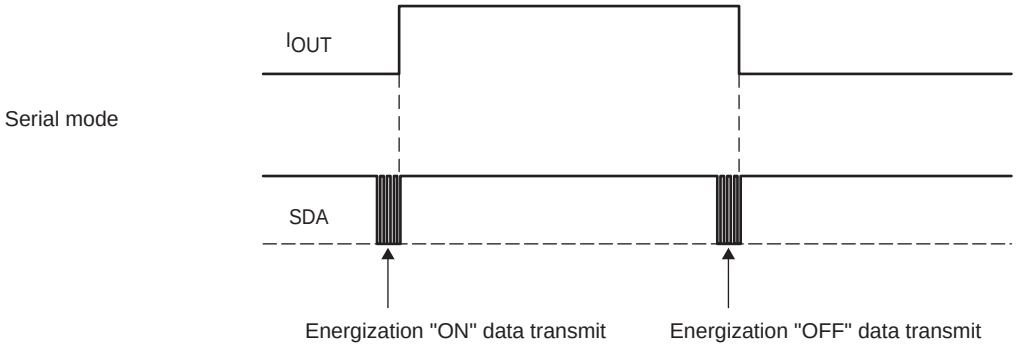


In the serial mode, energization is started by setting energization ON with serial data.

Energization time : Free mode · · · Starting and stopping of energization must both be set using the external trigger or serial data.



In the external trigger mode, energization is started on a rising edge of the SH/IR TR signal and stopped on the falling edge.



In the serial mode, energization is started by setting energization ON with serial data and stopped by setting it OFF.