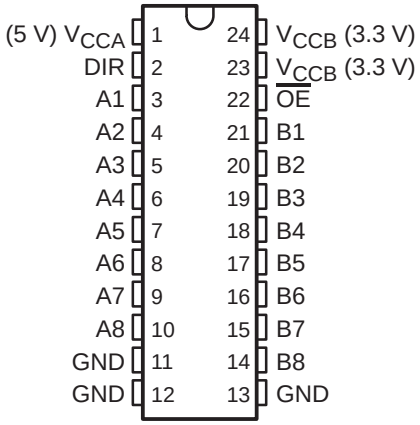
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **3.3-V to 5-V Bidirectional Level Shifter**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

**DB, DW, OR PW PACKAGE**
**(TOP VIEW)**




## description

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has $V_{CCB}$, which is set at 3.3 V, and A port has $V_{CCA}$, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

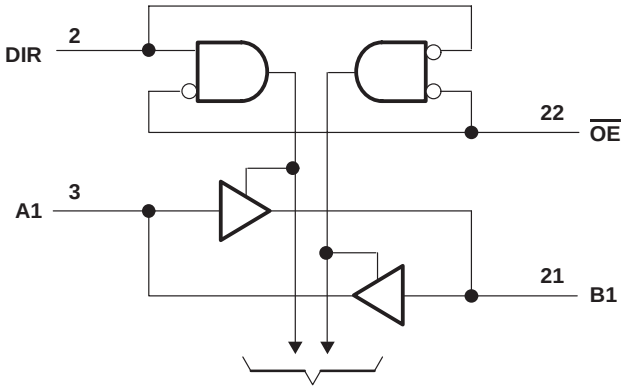
The SN74LVC4245A pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin ’245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional ’245 pinout.

The SN74LVC4245A is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range for $V_{CCA}$ = 5 V (unless otherwise noted)†

Supply voltage range, $V_{CCA}$ . . . . . –0.5 V to 6.5 V
Input voltage range, $V_I$: A port (see Note 1) . . . . . –0.5 V to $V_{CCA}$ + 0.5 V
Control inputs . . . . . –0.5 V to 6 V
Output voltage range, $V_O$: A port (see Note 1) . . . . . –0.5 V to $V_{CCA}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through each $V_{CCA}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 104°C/W
DW package . . . . . 81°C/W
PW package . . . . . 120°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 6 V maximum.
2. The package thermal impedance is calculated in accordance with JESD 51.

### absolute maximum ratings over operating free-air temperature range for $V_{CCB}$ = 3.3 V (unless otherwise noted)†

Supply voltage range, $V_{CCB}$ . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$: B port (see Note 3) . . . . . –0.5 V to $V_{CCB}$ + 0.5 V
Output voltage range, $V_O$: B port (see Note 3) . . . . . –0.5 V to $V_{CCB}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through $V_{CCB}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 104°C/W
DW package . . . . . 81°C/W
PW package . . . . . 120°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. The package thermal impedance is calculated in accordance with JESD 51.
3. This value is limited to 4.6 V maximum.

### recommended operating conditions for $V_{CCA}$ = 5 V (see Note 4)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CCA}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CCA}$ | V |
| $I_{OH}$ | High-level output current | | –24 | mA |
| $I_{OL}$ | Low-level output current | | 24 | mA |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at the associated $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### recommended operating conditions for $V_{CCB}$ = 3.3 V (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCB}$ | Supply voltage | | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CCB}$ = 2.7 V to 3.6 V | 2 | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CCB}$ = 2.7 V to 3.6 V | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CCB}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CCB}$ | V |
| $I_{OH}$ | High-level output current | $V_{CCB}$ = 2.7 V | | –12 | mA |
| | | $V_{CCB}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CCB}$ = 2.7 V | | 12 | mA |
| | | $V_{CCB}$ = 3 V | | 24 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at the associated $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range for $V_{CCA}$ = 5 V (unless otherwise noted) (see Note 5)

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 μA | | 4.5 V | 4.3 | | | V |
| | | | | 5.5 V | 5.3 | | | |
| | | $I_{OH}$ = –24 mA | | 4.5 V | 3.7 | | | |
| | | | | 5.5 V | 4.7 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | 4.5 V | | | 0.2 | V |
| | | | | 5.5 V | | | 0.2 | |
| | | $I_{OL}$ = 24 mA | | 4.5 V | | | 0.55 | |
| | | | | 5.5 V | | | 0.55 | |
| $I_I$ | Control inputs | $V_I = V_{CCA}$ or GND | | 5.5 V | | | ±1 | μA |
| $I_{OZ}$‡ | A port | $V_O = V_{CCA}$ or GND | | 5.5 V | | | ±5 | μA |
| $I_{CCA}$ | | $V_I = V_{CCA}$ or GND, | $I_O$ = 0 | 5.5 V | | | 80 | μA |
| $\Delta I_{CCA}$§ | | One input at 3.4 V, | Other inputs at $V_{CCA}$ or GND | 5.5 V | | | 1.5 | mA |
| $C_i$ | Control inputs | $V_I = V_{CCA}$ or GND | | Open | | 5 | | pF |
| $C_{io}$ | A port | $V_O = V_{CCA}$ or GND | | 5 V | | 11 | | pF |

† All typical values are measured at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or the associated $V_{CC}$.
NOTE 5: $V_{CCB}$ = 2.7 V to 3.6 V

## electrical characteristics over recommended operating free-air temperature range for $V_{CCB}$ = 3.3 V (unless otherwise noted) (see Note 6)

| PARAMETER | | TEST CONDITIONS | | $V_{CCB}$ | MIN | TYP¶ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 μA | | 2.7 V to 3.6 V | $V_{CC}$–0.2 | | | V |
| | | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | | |
| | | | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | | 3 V | 2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | 2.7 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | |
| $I_{OZ}$‡ | B port | $V_O = V_{CCB}$ or GND | | 3.6 V | | | ±5 | μA |
| $I_{CCB}$ | | $V_I = V_{CCB}$ or GND, | $I_O$ = 0 | 3.6 V | | | 50 | μA |
| $\Delta I_{CCB}$§ | | One input at $V_{CCB}$ – 0.6 V, | Other inputs at $V_{CCB}$ or GND | 2.7 V to 3.6 V | | | 0.5 | mA |
| $C_{io}$ | B port | $V_O = V_{CCB}$ or GND | | 3.3 V | | 11 | | pF |

‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or the associated $V_{CC}$.
¶ All typical values are measured at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
NOTE 6: $V_{CCA}$ = 5 V ± 0.5 V

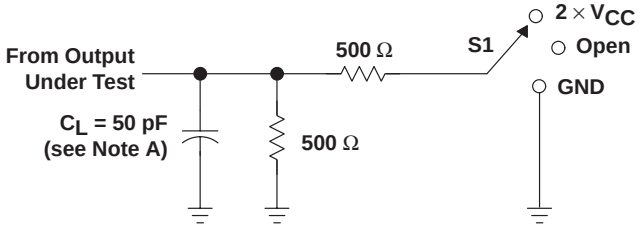
**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCA}$ = 5 V ± 0.5 V, $V_{CCB}$ = 2.7 V TO 3.6 V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{PHL}$ | A | B | 1 | 6.3 | ns |
| $t_{PLH}$ | | | 1 | 6.7 | |
| $t_{PHL}$ | B | A | 1 | 6.1 | ns |
| $t_{PLH}$ | | | 1 | 5 | |
| $t_{PZL}$ | $\overline{OE}$ | A | 1 | 9 | ns |
| $t_{PZH}$ | | | 1 | 8.1 | |
| $t_{PZL}$ | $\overline{OE}$ | B | 1 | 8.8 | ns |
| $t_{PZH}$ | | | 1 | 9.8 | |
| $t_{PLZ}$ | $\overline{OE}$ | A | 1 | 7 | ns |
| $t_{PHZ}$ | | | 1 | 5.8 | |
| $t_{PLZ}$ | $\overline{OE}$ | B | 1 | 7.7 | ns |
| $t_{PHZ}$ | | | 1 | 7.8 | |

**operating characteristics, $V_{CCA}$ = 5 V, $V_{CCB}$ = 3.3 V, $T_A$ = 25°C**

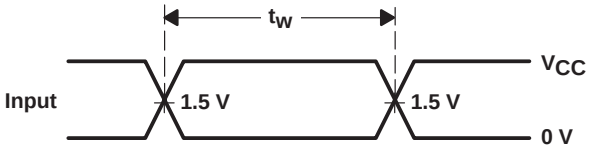
| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per transceiver | Outputs enabled | $C_L$ = 0, | f = 10 MHz | 39.5 | pF |
| | | Outputs disabled | | | 5 | |

## PARAMETER MEASUREMENT INFORMATION (A PORT)

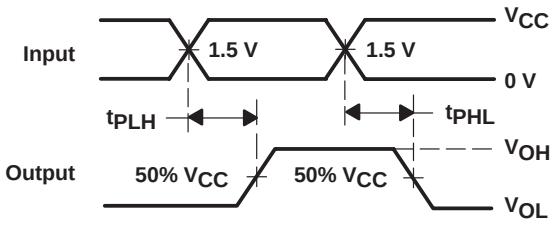



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

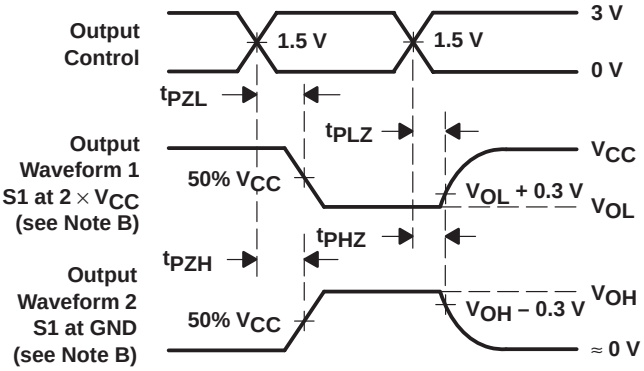
LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

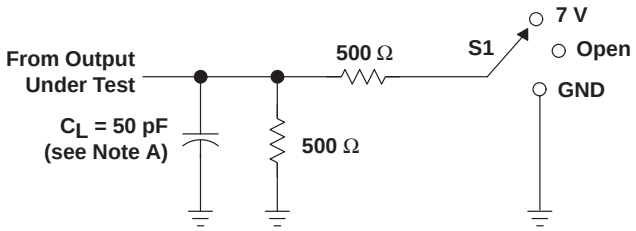



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

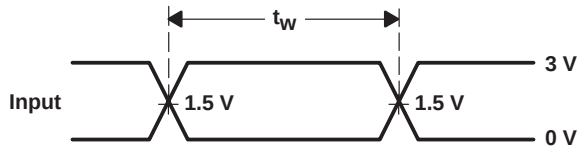
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION (B PORT)

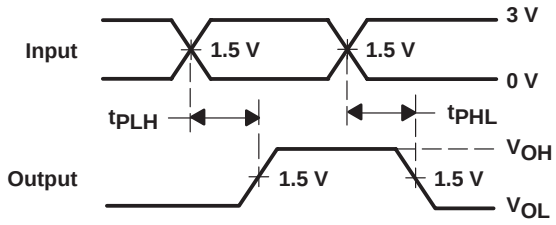



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | GND |

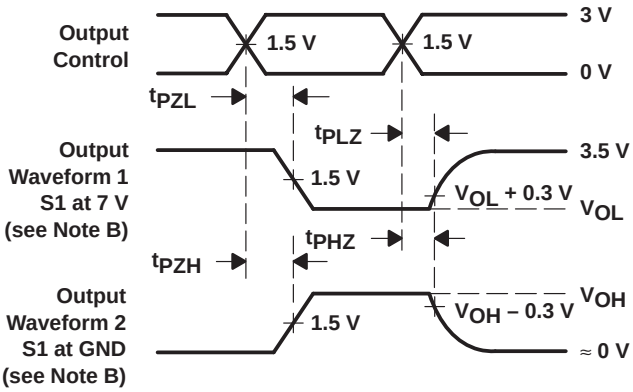
LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

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