LX1673

High Frequency PWM Regulator

PRODUCTION DATA SHEET

DESCRIPTION

The LX1673 is a highly integrated power supply controller IC featuring one PWM switching regulator stage with an additional onboard linear regulator driver.

With several switching frequencies available (up to 900kHz) the LX1673 can be optimized for both cost and PCB space. Utilizing external compensation, a wide selection of external components can be chosen for use in any application while maintaining stable operation.

The LX1673 incorporates a fully programmable soft-start and power sequence capabilities. The LDO and PWM have independent enable pins.

With onboard gate drivers, the switching PWM output is capable of sourcing up to 15A. The LX1673 also features an additional Linear Regulator Controller output, which when coupled with an inexpensive MOSFET is capable of supplying up to an additional 5A for I/O, memory, and other supplies surrounding today's microprocessor designs.

Each regulator output voltage is programmed via a simple voltage-divider network.

Integrated hiccup mode current limiting is implemented utilizing MOSFET $R_{DS(ON)}$ impedance. This enables the LX1673 to monitor maximum current limit conditions without the use of expensive current sense resistors.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

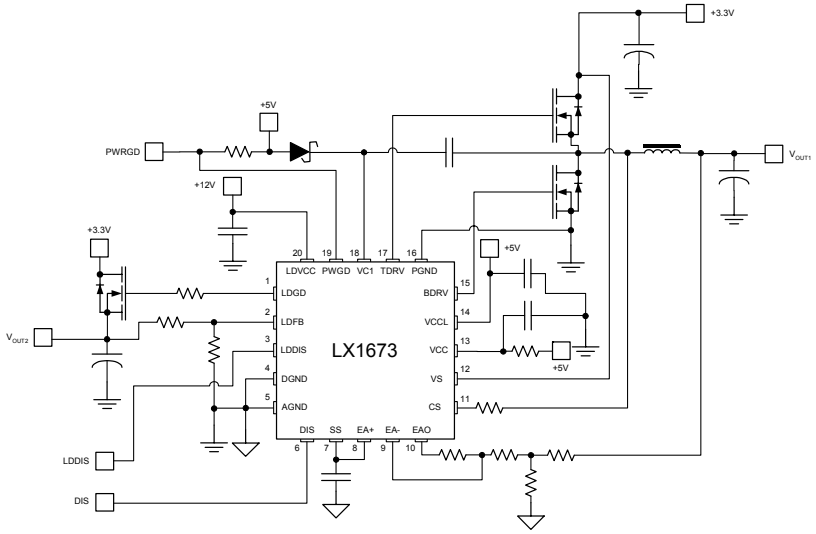
KEY FEATURES

- Two Independently Regulated Outputs
- Outputs As Low As 0.8V Generated From An Internal 1% Reference
- Integrated High Current MOSFET Drivers
- 300KHz, 600KHz, and 900KHz High Frequency Operation Minimizes External Component Requirements
- Soft-Start and Power Sequencing Control
- Adjustable Linear Regulator Driver Output
- No current-sense resistors

APPLICATIONS/BENEFITS

- Video Card Power Supplies
- PC Peripherals
- Computer Add-On Cards
- 3.3V Power Conversion
- DDR Memory Termination

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)	Switching Frequency (kHz)	PW Plastic TSSOP 20-Pin RoHS Compliant / Pb-free	LQ Plastic MLPQ 20-Pin RoHS Compliant / Pb-free
-40 to 85	300	LX1673-03CPW	LX1673-03CLQ
-40 to 85	600	LX1673-06CPW	LX1673-06CLQ
-40 to 85	900	LX1673-09CPW	LX1673-09CLQ

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1673-03CPW-TR)

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LX1673

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) DC ..... -0.3V to 5.5V
Supply Voltage (V_{CC}) Transient ..... -0.3V to 6V
Driver Supply Voltage (V_{CCL}) DC ..... -0.3V to 13V
Driver Supply Voltage (V_{CCL}) Transient ..... -0.3V to 16V
Driver Supply Voltage (V_{C1}) DC ..... -0.3V to 19V
Input Voltage (SS/DIS) ..... -0.3V to 5.5V
Output Drive Peak Current Source (HO, LO) 1A (500ns)
Output Drive Peak Current Sink (HO, LO) 1A (500ns)
Operating Temperature Range ..... -40°C to 85°C
Maximum Operating Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering 180 seconds) ..... 235°C
Package Peak Temp. for Solder Reflow (40 Seconds Maximum Exposure).. 260°C(+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

The limitation on transient time is thermal and is due to zener diodes on the supply pins, application of maximum voltages will increase current into that pin and increase package power dissipation.

THERMAL DATA

PW **Plastic TSSOP 20-Pin**

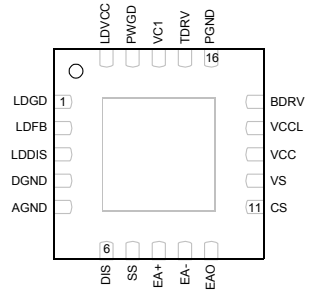
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	90°C/W

LQ **Plastic MLPQ 20-Pin**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	35°C/W

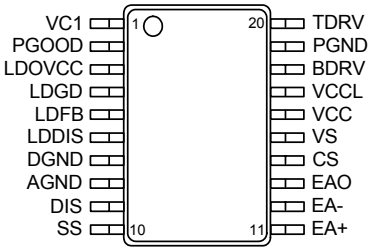
Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JC})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system.
All of the above assume no airflow.

PACKAGE PIN OUT



LQ PACKAGE
(Top View)

N.C. – No Internal Connection
N/U – Not Used
RSVD – Do Not Use



PW PACKAGE
(Top View)

Pb-free 100% Matte Tin Lead Finish

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FUNCTIONAL PIN DESCRIPTION

NAME	DESCRIPTION
EA-	Voltage Feedback – Output voltage is connected through a resistor network to this pin for feedback to set the desired output voltage of the switching PWM output.
EAO	Error Amplifier Output – Sets error amplifier gain and external compensation if used.
EA+	Voltage Reference – Connect to the SS pin or any other external voltage. Used in conjunction with EA-, and an external resistor divider, to set the desired output voltage for the PWM output.
VCC	IC supply voltage (nominal 5V).
VCCL	Power supply pin for Low side drivers.
LDFB	Low Dropout Regulator Voltage Feedback – Sets output voltage of external MOSFET via resistor network.
CS	Over-Current Limit Set – Connecting a resistor between CS pin and the source of the high-side MOSFET sets the current-limit threshold for the PWM output. A minimum of 1KΩ must be in series with this pin.
SS	PWM Soft-start/Hiccup Capacitor Pin – During start-up, the voltage on this pin controls the output voltage of the switching regulator. An internal 20KΩ resistor and the external capacitor set the time constant for soft-start function. The Soft-start function does not initialize until the supply voltage on V_{CC} exceeds the UVLO threshold. When an over-current condition occurs, this capacitor is used for the timing of hiccup mode protection.
AGND	Analog ground reference.
DGND	Digital ground reference.
LDGD	Low Dropout Regulator Gate Drive – Connect to gate of external N-Channel MOSFET for linear regulator function.
PGND	MOSFET Driver Power Ground. Connects to the source of the bottom N-channel MOSFETS of the switching regulator.
TDRV	High Side MOSFET Gate Driver
BDRV	Low Side MOSFET Gate Driver
VC1	High-Side MOSFET Gate Driver Supply – Connect to separate supply or boot strap supply to ensure proper high-side gate driver supply voltage.
LDDIS	LDO Disable Input – High disables LDO output. This pin has a 100KΩ pull down resistor.
VS	Voltage reference for Short Circuit Current sense. This pin is also the supply pin for the Current Sense Comparator. This pin cannot be left floating, if current limit is not used connect to VCC.
PWGD	Power Good Output – Open drain output, goes high at end of Soft Start and no Fault. Pulls low if any Fault condition occurs.
LDVCC	LDO VCC Supply – Connect to voltage supply greater than supply rail for LDO MOSFET drain.
DIS	PWM Disable Input –High disables the PWM output. This pin has a 80KΩ pull down resistor.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature $0°C \leq T_A \leq 70°C$ except where otherwise noted and the following test conditions: V_{CC} = 5V, V_{CCL} = 5V, V_{C1}=12V, LDVCC = 12V, TDRV = BDRV = 3000pF Load.

Parameter	Symbol	Test Conditions	LX1673 Min	LX1673 Typ	LX1673 Max	Units
SWITCHING REGULATORS						
Input Voltage	V_{CC}		4.5		5.5	V
	V_{CCL},V_{C1}				16	
Operation Current	I_{CC}	Static and Dynamic		6		mA
LDO Operating Current	I_{LDVCC}			1		mA
Reference Voltage	V_{SS}	T_A=25°C	0.792	0.8V	0.808	V
		$0°C \leq T_A \leq 70°C$	0.784		0.816	V
Line Regulation Note 1			-1		1	%
Load Regulation Note 1			-1		1	
Dead Time		3000pF Load 2 Volt Level			160	nS
Minimum Pulse Width		All Frequencies			150	nS
Maximum Duty Cycle		LX1673-03 Load = 3000pF	85			%
Maximum Duty Cycle		LX1673-06 Load = 3000pF	75			%
Maximum Duty Cycle		LX1673-09 Load = 3000pF	70			%
ERROR AMPLIFIERS						
Input Offset Voltage	V_{OS}	Common Mode Voltage = 1V	-6.0		6.0	mV
DC Open Loop Gain				70		dB
Unity Gain Bandwidth	UGBW			16		MHz
High Output Voltage	V_{OH}	I Source = 2mA	3.8	5.0		V
Low Output Voltage	V_{OL}	I Sink = 10uA			100	mV
Input Common Mode Voltage Range		Input Offset Voltage $\leq$ 20mV	0.1		3.5	V
Input Bias Current		0 and 3.5 V Common Mode Voltage		100		nA
CURRENT SENSE						
Current Sense Bias Current	I_{SET}	$V_{CS} = V_{VS} – 0.3V$, V_{VS} = 5V	45	50	55	µA
Trip Threshold	V_{TRIP}	Referenced to VS , $V_{VS = 5V}$	260	300	340	mV
Current Sense Delay	T_{CSD}			350		nS
Current Sense Comparator Operating Current	I_{CS}	Current into VS pin		2	5	mA
OUTPUT DRIVERS – N-CHANNEL MOSFETS						
Low Side Driver Operating Current	I_{VCCL}	Static		2.5		mA
High Side Driver Operating Current	I_{VC1}	Static		3		mA
Drive Rise Time, Fall Time	T_{RF}	C_L = 3000pF		50		nS
High Level Voltage	V_{DH}	I_{SOURCE} = 20mA, V_{CCL} = 12V	10	11		V
Low Level Voltage	V_{DL}	I_{SINK} = 20mA, V_{CCL} = 12V		0.15	0.25	V
OSCILLATOR						
PWM Switching Frequency	F_{SW}	LX1673-03	255	300	345	KHz
		LX1673-06	510	600	690	
		LX1673-09	765	900	1035	
Ramp Amplitude	V_{RAMP}			1.25		V_{PP}

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 70°C except where otherwise noted and the following test conditions: V_{CC} = 5V, V_{CCL} = 5V, V_{C1}=12V, LDVCC = 12V, TDRV = BDRV = 3000pF Load.

Parameter	Symbol	Test Condition	LX1673 Min	LX1673 Typ	LX1673 Max	Units
UVLO AND SOFT-START (SS)						
Start-Up Threshold (V_{C1}, V_{CCL}, LD_{VCC})				4.0		V
Start-Up Threshold (V_{CC})			4.0	4.25	4.5	V
Hysteresis V_{CC}				0.1		V
SS Input Resistance	R_{SS}			20		KΩ
SS Shutdown Threshold	V_{SHDN}			0.1		V
Hiccup Mode Duty Cycle		C_{SS} = 0.1µF		10		%
LINEAR REGULATOR CONTROLLER						
Voltage Reference Tolerance		V_{LDFB} = .8V, C_{OUT} = 330µF		2		%
Source Current	I_{HDRV}	V_{OUT} = 10V	30			mA
Sink Current	I_{LDRV}	V_{OUT} = 0.4V		0.2		mA
DISABLE INPUTS						
PWM Disable	DIS	Threshold		1		V
		Internal Pull down Resistance		80		KΩ
LDO Disable	LDDIS	Threshold		2.5		V
		Internal Pull down Resistance		100		KΩ
POWER GOOD						
Drain to Source Voltage		I = 3mA		0.4		V
Leakage				0.05		µA

Note 1: System Specification

Note 2: Low duty cycle pulse testing techniques are used which maintain junction and case temperatures equal to the ambient temperature

Note 3: Functionality over the –40 to 85 deg C operating temperature range is assured by design, characterization, and statistical process control

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BLOCK DIAGRAM

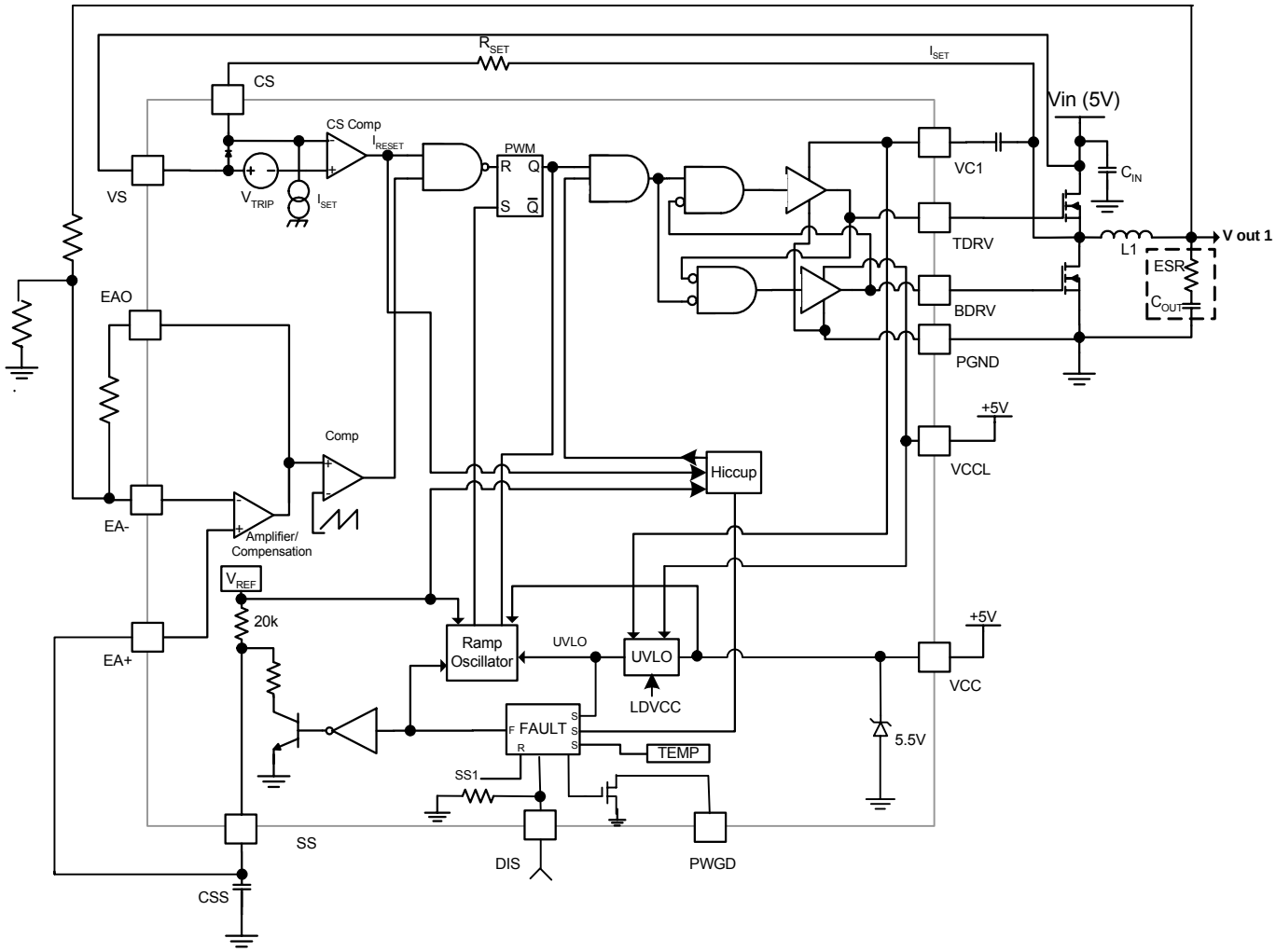

Figure 1 – Block Diagram of PWM Phase

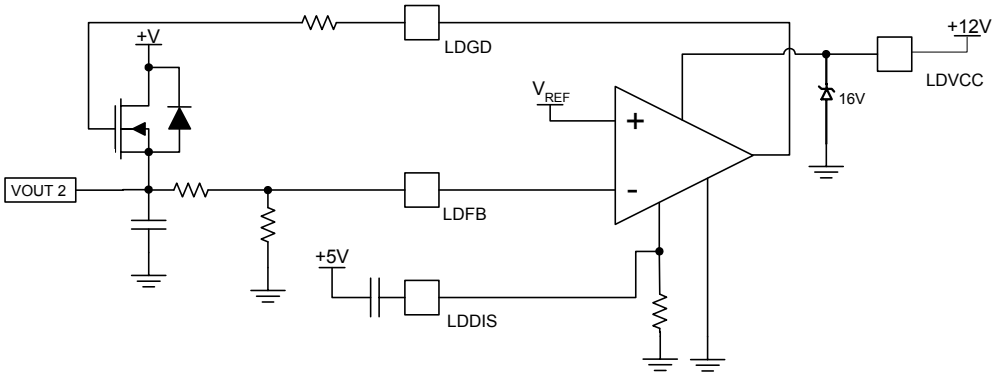

Figure 2 – LDO Controller Block Diagram

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APPLICATION SCHEMATIC

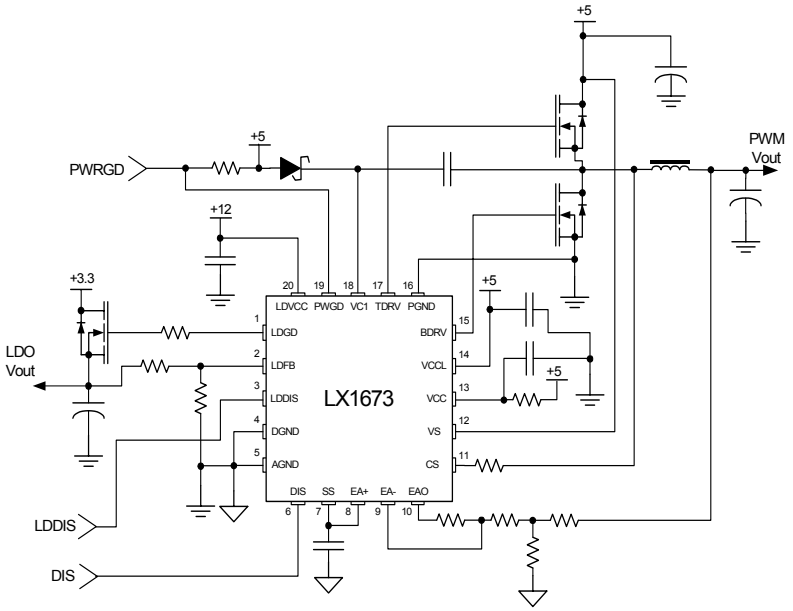

Figure 3 – Schematic with Bootstrap Supply for PWM High Side Drive

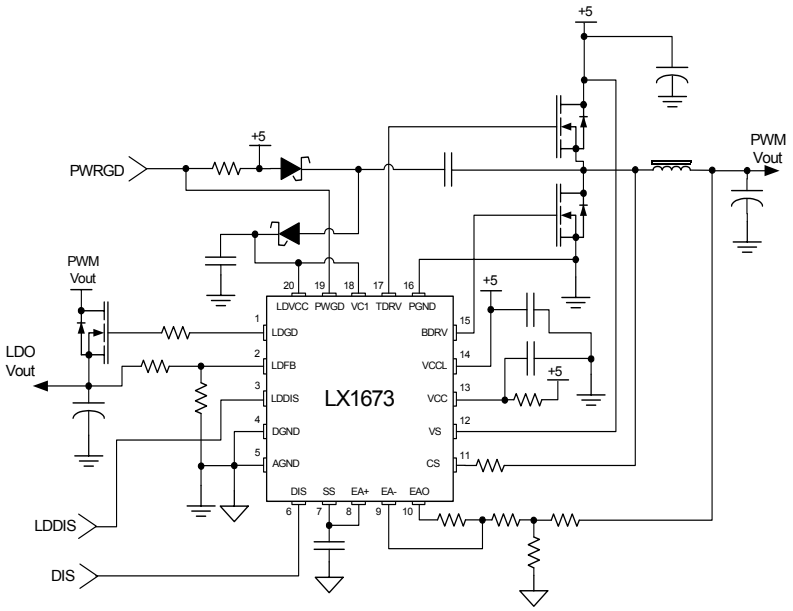

Figure 4 – Schematic for 5 Volt only Input

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THEORY OF OPERATION

GENERAL DESCRIPTION

The LX1673 is a voltage-mode pulse-width modulation controller integrated circuit. The internal oscillator and ramp generator frequency is fixed to 300KHz, 600KHz, or 900KHz. The device has external compensation, for more flexibility of output current magnitude.

UNDER VOLTAGE LOCKOUT (UVLO)

At power up, the LX1673 monitors the supply voltage for VCC, VCCL, LDVCC and VC1 (there is no requirement for sequencing the supplies). Before all supplies reach their under-voltage lock-out (UVLO) thresholds, the soft-start (SS) pin is held low to prevent soft-start from beginning, the oscillator is disabled and all MOSFETs are held off. There is an internal delay that will filter out transients less that 1.5µSec.

SOFT-START

Once the supplies are above the UVLO threshold, the soft-start capacitor begins to be charged by the reference through a 20kΩ internal resistor. The capacitor voltage at the SS pin rises as a simple RC circuit. The SS pin is connected to the error amplifier's non-inverting input that controls the output voltage. The output voltage will follow the SS pin voltage if sufficient charging current is provided to the output capacitor.

The simple RC soft-start allows the output to rise faster at the beginning and slower at the end of the soft-start interval. Thus, the required charging current into the output capacitor is less at the end of the soft-start interval. A comparator monitors the SS pin voltage and indicates the end of soft-start when SS pin voltage reaches 95% of V_{REF}.

OVER-CURRENT PROTECTION (OCP) AND HICCUP

The LX1673 uses the $R_{DS(ON)}$ of the upper MOSFET, together with a resistor (R_{SET}) to set the actual current limit point. The current sense comparator senses the MOSFET current 350nS after the top MOSFET is switched on in order to reduce inaccuracies due to ringing. A current source supplies a current (I_{SET}), whose magnitude is 50µA. The set resistor R_{SET} is selected to set the current limit for the application. R_{SET} and VS should be connected directly at the upper MOSFET drain and source to get an accurate measurement across the low resistance $R_{DS(ON)}$.

When the sensed voltage across $R_{DS(ON)}$ plus the set resistor exceeds the 300mV, V_{TRIP} threshold, the OCP comparator outputs a signal to reset the PWM latch and to start hiccup mode. The soft-start capacitor (C_{SS}) is discharged slowly (10 times slower than when being charged up by R_{SS}). When the voltage on the SS pin reaches a 0.1V threshold, hiccup finishes and the circuit soft-starts again. During hiccup both MOSFETs are held off.

Hiccup is disabled during the soft-start interval, allowing the circuit to start up with maximum current. If the rate of rise of the output voltage is too fast, the required charging current to the output capacitor may be higher than the limit-current. In this case, the peak MOSFET current is regulated to the limit-current by the current-sense comparator. If the MOSFET current still reaches its limit after the soft-start finishes, the hiccup is triggered again. When the output has a short circuit the hiccup circuit ensures that the average heat generation in both MOSFETs and the average current is much less than in normal operation,.

Over-current protection can also be implemented using a sense resistor, instead of using the $R_{DS(ON)}$ of the upper MOSFET, for greater set-point accuracy.

OSCILLATOR FREQUENCY

An internal oscillator sets the switching frequency at 300kHz, 600kHz, or 900kHz.

APPLICATION NOTE

OUTPUT INDUCTOR

The output inductor should be selected to meet the requirements of the output voltage ripple in steady-state operation and the inductor current slew-rate during transient. The peak-to-peak output voltage ripple is:

$$V_{RIPPLE} = ESR \times I_{RIPPLE}$$

where

$$\Delta I = \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{f_s}$$

ΔI is the inductor ripple current, L is the output inductor value and ESR is the Effective Series Resistance of the output capacitor.

ΔI should typically be in the range of 20% to 40% of the maximum output current. Higher inductance results in lower output voltage ripple, allowing slightly higher ESR to satisfy the transient specification. Higher inductance also slows the inductor current slew rate in response to the load-current step change, ΔI, resulting in more output-capacitor voltage droop. When using electrolytic capacitors, the capacitor voltage droop is usually negligible, due to the large capacitance

The inductor-current rise and fall times are:

$$T_{RISE} = L \times \frac{\Delta I}{(V_{IN} - V_{OUT})}$$

and

$$T_{FALL} = L \times \frac{\Delta I}{V_{OUT}}$$

.

The inductance value can be calculated by

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times \frac{D}{f_s}$$

OUTPUT CAPACITOR

The output capacitor is sized to meet ripple and transient performance specifications. Effective Series Resistance (ESR) is a critical parameter. When a step load current occurs, the output voltage will have a step that equals the product of the ESR and the current step, ΔI. In an advanced microprocessor power supply, the output capacitor is usually selected for ESR instead of capacitance or RMS current capability. A capacitor that satisfies the ESR requirements usually has a larger capacitance and current capability than strictly needed. The allowed ESR can be found by:

$$ESR \times (I_{RIPPLE} + \Delta I) < V_{EX}$$

Where I_{RIPPLE} is the inductor ripple current, ΔI is the maximum load current step change, and V_{EX} is the allowed output voltage excursion in the transient.

Electrolytic capacitors can be used for the output capacitor, but are less stable with age than tantalum capacitors. As they age, their ESR degrades, reducing the system performance and increasing the risk of failure. It is recommended that multiple parallel capacitors be used, so that, as ESR increase with age, overall performance will still meet the processor's requirements.

There is frequently strong pressure to use the least expensive components possible; however, this could lead to degraded long-term reliability, especially in the case of filter capacitors. Microsemi's demonstration boards use the CDE Polymer AL-EL (ESRE) filter capacitors, which are aluminum electrolytic, and have demonstrated reliability. The OS-CON series from Sanyo generally provides the very best performance in terms of long term ESR stability and general reliability, but at a substantial cost penalty. The CDE Polymer AL-EL (ESRE) filter series provides excellent ESR performance at a reasonable cost. Beware of off-brand, very low-cost filter capacitors, which have been shown to degrade in both ESR and general electrolytic characteristics over time.

INPUT CAPACITOR

The input capacitor and the input inductor, if used, are to filter the pulsating current generated by the buck converter to reduce interference to other circuits connected to the same 5V rail. In addition, the input capacitor provides local de-coupling for the buck converter. The capacitor should be rated to handle the RMS current requirements. The RMS current is:

$$I_{RMS} = I_L \sqrt{d(1-d)}$$

Where I_L is the inductor current and d is the duty cycle. The maximum value occurs when d = 50%, then $I_{RMS} = 0.5I_L$. For a 5V input and output voltages in the range of 2 to 3V, the required RMS current is very close to $0.5I_L$.

SOFT-START CAPACITOR

The value of the soft-start capacitor determines how fast the output voltage rises and how large the inductor current is required to charge the output capacitor. The output voltage will follow the voltage at the SS pin if the required inductor current does not exceed the maximum allowable current for the inductor.

APPLICATION NOTE (CONTINUED)

The SS pin voltage can be expressed as:

$$V_{SS} = V\,ref\left(1 - e^{-t/R_{SS}C_{SS}}\right)$$

Where R_{SS} and C_{SS} are the soft-start resistor and capacitor.

The current required to charge the output capacitor during the soft start interval is.

$$Iout = Cout\frac{dVss}{dt}$$

Taking the derivative with respect to time results in

$$Iout = \frac{VrefCout}{RssCss}e^{-t/R_{SS}C_{SS}}$$

and at t=0

$$Imax = \frac{VrefCout}{RssCss}$$

The required inductor current for the output capacitor to follow the soft start voltage equals the required capacitor current plus the load current. The soft-start capacitor should be selected to provide the desired power on sequencing and insure that the overall inductor current does not exceed its maximum allowable rating.

Values of C_{SS} equal to 0.1µf or greater are unlikely to result in saturation of the output inductor unless very large output capacitors are used.

OVER-CURRENT PROTECTION

Current limiting occurs at current level I_{CL} when the voltage detected by the current sense comparator is greater than the current sense comparator threshold, V_{TRIP} (300mV).

$$I_{CL} \times R_{DS(ON)} + I_{SET} \times R_{SET} = V_{TRIP}$$

So,

$$R_{SET} = \frac{V_{TRIP} - I_{CL} \times R_{DS(ON)}}{I_{SET}} = \frac{300\,mV - I_{CL} \times R_{DS(ON)}}{50\,\mu A}$$

Example:

For 10A current limit, using FDS6670A MOSFET (10mΩ $R_{DS(ON)}$):

$$R_{SET} = \frac{0.3 - 10 \times 0.010}{50 \times 10^{-6}} = 4K\,\Omega$$

Note: Maximum R_{SET} is 6KΩ . Any resistor 6KΩ or greater will not allow startup since I_{CL} will equal zero (50µA x 6KΩ = 300mV).

At higher PWM frequencies or low duty cycles where the upper gate drive is less than 350nS wide the 350nS delay for current limit enable may result in current pulses exceeding the desired current limit set point. If the upper MOSFET on time is less than 350nS and a short circuit condition occurs the duty cycle will increase, since V_{OUT} will be forced low. The current limit circuit will be enabled when the upper gate drive exceeds 350nS although the actual peak current limit value will be higher than calculated with the above equation.

Short circuit protection still exists due to the narrow pulse width even though the magnitude of the current pulses will be higher than the calculated value.

If OCP is not desired connect both VSX and VCX to VCC. Do not leave them floating.

OUTPUT DISABLE

The LX1673 PWM MOSFET driver outputs are shut off by pulling the disable (DIS) pin above 1.2V. There is a 80KΩ pull down resistor on this input.

The LDO voltage regulator has its own Disable pin (LDDIS) for control of this output voltage. Pulling this pin above 3 V disables the LDO. There is a 100KΩ pull down resistor on this input.

PROGRAMMING THE OUTPUT VOLTAGE

The output Voltage is sensed by the feedback pin (FB_X) which is compared to a 0.8V reference. The output voltage can be set to any voltage above 0.8V (and lower than the input voltage) by means of a resistor divider (see Figure 1).

$$V_{OUT} = V_{REF}(1 + R_1/R_2)$$

Note: This equation is simplified and does not account for error amplifier input current. Keep R_1 and R_2 close to 1KΩ (order of magnitude).

DDR V_{TT} TERMINATION VOLTAGE

Double Data Rate (DDR) SDRAM requires a termination voltage (V_{TT}) in addition to the line driver supply voltage (VDDQ) and receiver supply voltage (VDD).

V_{TT} for DDR memory can be generated with the LX1673 by using the positive input of the phase 2 error amplifier RF2 as a reference input from an external reference voltage V_{REF} which is defined as one half of VDDQ. Using V_{REF} as the reference input will insure that all voltages are correct and track each other as specified in the JEDEC (EIA/JESD8-9A) specification. The phase 2 output will then be equal to V_{REF} and track the VDDQ supply as required.

When an external reference is used the connection between the error amplifier positive input and the Soft Start pin is lost and Soft Start will not function. It is recommended that the external reference voltage have an R-C time constant that will be long enough to allow the output capacitor to charge slowly.

See Microsemi Application Note 17 for more details

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APPLICATION NOTE CONSIDERATIONS

1. The minimum R_{SET} resistor value is 1k ohm for the current limit sensing. If this resistor becomes shorted, it will do permanent damage to the IC.
2. A resistor has been put in series with the gate of the LDO pass transistor to reduce the output noise level. The resistor value can be changed to optimize the output transient response versus output noise.
3. To delay the turn on of the LDO controller output, a capacitor should be connected between the LDDIS pin and the +5volts. The LDDIS input has a 100K pull down resistor, which keeps the LDO active until this pin is pulled high. During the power up sequence the capacitor connected to the LDDIS pin will keep the LDO off until this capacitor, being charge by the 100K pull down resistor, goes through the low input threshold level.
4. . If current limit is not used connect the VS and VC pins together and to VCC. Do not leave them floating. A floating VS pin will result in operation resembling a hiccup condition.

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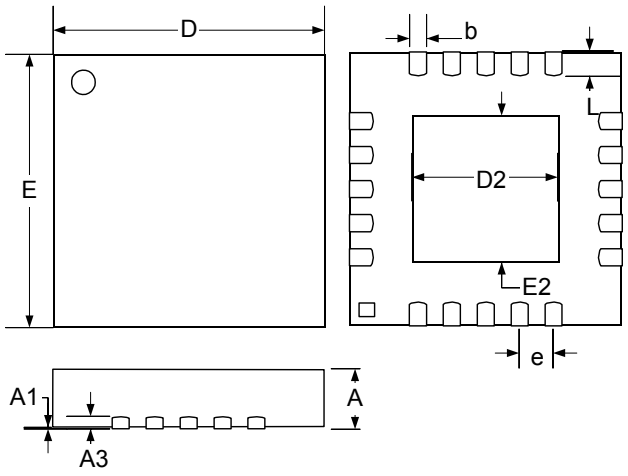
PACKAGE DIMENSIONS

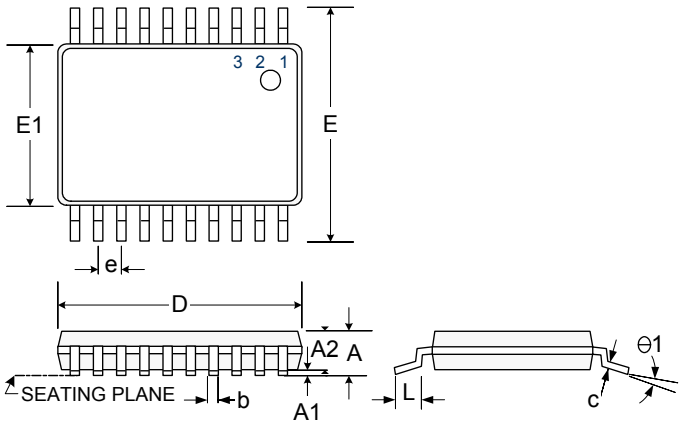
LQ 20-Pin Micro Leadframe Package (MLPQ) Package



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.25 REF		0.010	
b	0.23	0.38	0.009	0.015
D	5.00 BSC		0.197	
D2	1.25	3.25	0.050	0.128
E	5.00 BSC		0.197	
E2	1.25	3.25	0.050	0.128
e	0.65 BSC		0.026	
L	0.35	0.75	0.014	0.030

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(0.006") on any side. Lead dimension shall not include solder coverage.

PW 20-Pin Thin Small Shrink Outline (TSSOP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.10	-	0.043
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	6.40	6.60	0.252	0.260
E	6.25	6.55	0.246	0.258
E1	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
Θ1	0°	8°	0°	8°
*LC	-	0.10	-	0.004

solder coverage.

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NOTES

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