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LX1691

Enhanced Multi-Mode CCFL Controller

PRODUCTION DATA SHEET

DESCRIPTION

Microsemi's LX1691 is a cost reduced, enhanced feature set, Direct Drive CCFL (Cold Cathode Fluorescent Lamp) Controller. Its architecture is based on the very popular LX1689. By limiting V_{DDP} to 5.5V and using advanced processing, die size and package pin count is decreased while improving dimming precision.

LX1691 based inverter modules can be designed for virtually any CCFL appliance from digital cameras and PDA's to big screen monitors and driver viewable automotive displays.

New versatile dimming circuitry can accept digital and analog control inputs and provides six different dimming modes that control both lamp current amplitude and duty cycle, either simultaneously or separately. Designers can select normal or reverse polarity dimming and precisely program minimum and maximum lamp currents with resistors. The LX1691 fault shutdown feature is enhanced to include regulation and shutdown for over voltage and over current conditions.

Microsemi's proven and patented Direct Drive architecture works with system voltages from 3 volts to more than 50 volts, limited only by the external power FET's that drive the high voltage transformer.

The LX1691 includes the Microsemi proven and patented strike method that allows significant efficiency gains while guaranteeing strong striking power at all operating temperatures. Our method *sweeps* strike frequency smoothly up to the unloaded resonant frequency of the lamp and high voltage transformer. This, coupled with the LX1691's active high output voltage regulation, produces just enough strike voltage without generating unpredictable high voltage spikes that cause arcing and component failures. Competitive devices that simply *switch* to a higher frequency for striking do not have this "real time" control over output voltage, and require much more attention to transformer design.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

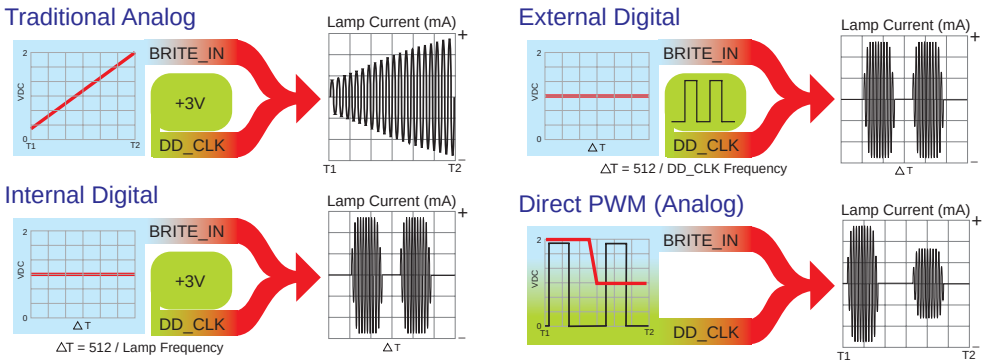
KEY FEATURES

- Simultaneous Amplitude And Duty Cycle Dimming Modes
- Resistor Programmable Min and Max Lamp Currents
- Digital Dimming Can Synch To External Or Internal Clocks
- 100 ms Power On Delay
- Open Or Shorted Lamp Regulation & Shutdown
- "On Chip" Full Wave Lamp Current & Voltage Rectifiers
- 16 Pin TSSOP Package
- Very Stable Oscillator with On-Chip Timing Capacitor
- Soft Start-Up Striking
- Enhanced Digital Dimming Resolution

BENEFITS

- Low Component Count / Module Cost / And Size
- High "Nits/Watt" Efficiency
- Operates Directly From a Single Li-Ion Cell
- Industries Safest And Highest Performing Strike Voltage Generation (Patented)
- Tight Operating Frequency Tolerance For Easier System Level RFI Control

PRODUCT HIGHLIGHT



Four of Six Dimming Modes

PACKAGE ORDER INFO

T_A (°C)	MIN V_{DDP}	MAX V_{DDP}	PW Plastic TSSOP 16-PIN
-40 to +85	2.8V	5.5V	**LX1691IPW** Pb-free

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1691IPWTR)

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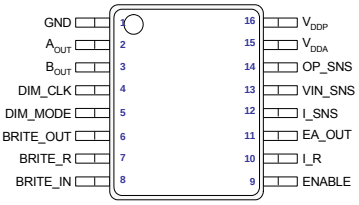
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DDP}) 6V
Digital Input (ENABLE) ..... -0.3V to V_{DDP} +0.5V
Analog Inputs (I_SNS, OC_SNS, OV_SNS) clamped to +/- 10V. Max peak current +/-100mA
Analog Inputs (BRITE_IN) ..... -0.3V to V_{DDP} +0.5V
DIM_MODE Input ..... -0.3V to V_{DDP} +0.5V
DD_CLK Digital Input ..... 0.3V to V_{DDP} +0.5V
Digital Output (A_{OUT}, B_{OUT}) ..... -0.3V to V_{DDP} +0.5V
Analog Outputs (BRITE_R, I_R, EA_OUT,BRITE_OUT) ..... -0.3V to V_{DDP} +0.5V
Operating Temperature Range ..... -55 to 125°C
Maximum Junction Temperature ..... 150°C
Package Peak Temperature for Solder Reflow (40 Seconds Maximum Exposure) ..... 255°C (+5 -0)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



PW PACKAGE
(Top View)

Pb-free 100% Matte Tin Lead Finish

THERMAL DATA

PW **Plastic TSSOP 16-Pin**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	99°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

FUNCTIONAL PIN DESCRIPTION

PIN NAME	DESCRIPTION
GND	Ground
V_{DDP}	Voltage Input, 3.0 to 5.5V input range. V_{DDP} is switched (see ENABLE) to remove power from chip. An LDO regulator follows the switch and generates V_{DDA} (see V_{DDA}). The output driver stages are powered directly from the V_{DDP} input. Care must be taken in power distribution design to minimize transients and noise coupling from V_{DDP} to the V_{DDA} output.
V_{DDA}	Analog V_{DDA} Supply Output. This output pin is used to connect an external capacitor to stabilize and filter the on chip V_{DDA} LDO regulator. The input of the LDO is the switched V_{DDP} supply. LDO output is normally 3.0V and is used to drive all circuitry except the output buffers at AOUT and BOUT. Drop out voltage is typically 50mV (@ 25°C) at 5mA, the average internal load. This output can supply up to a 5 mA external load. The output capacitor recommended is <1000nF of the ceramic dielectric type.
A_{OUT}	A buffer N-FET driver output. 10K internal pull down, ± 100 mA peak current with 3 VDC applied to V_{DDP} pin.
B_{OUT}	B buffer N-FET driver output. 10K internal pull down, ± 100 mA peak current with 3 VDC applied to V_{DDP} pin.
DD_CLK*	Digital Dimming Clock / Dimming Polarity. An input pin that may be selected to control burst frequency for Digital Dimming. This input can be forced to V_{DDA} or VSS or any clock signal up to 1MHz. This pin is also used to control the dimming polarity when operating in the internally clocked digital dimming mode*. If DIM_MODE is in the open condition (Analog Dimming Mode) the DD_CLK input is tied to V_{DDA} or open (internal pull-up) to select conventional dimming polarity. It is tied to Ground for reverse polarity. Conventional polarity means that lamp brightness increases with increasing voltage on the BRITE_IN pin. Reverse polarity means that brightness decreases with increasing voltage. If DIM_MODE is open and a low frequency pulse is applied to DD_CLK, lamp current amplitude is directly proportional to the voltage at BRITE_IN, and its duty cycle follows the DD_CLK waveform, e.g., current flows when DD_CLK is high. In this mode pulse count should be greater than fault count..

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FUNCTIONAL PIN DESCRIPTION (CONTINUED)

PIN NAME	DESCRIPTION
DIM_MODE*	Dimming Mode Input. This three state input pin places the IC in Analog Dimming Mode, internal Digital Dimming Mode, or external Digital Dimming Mode. If the input is left open or forced to V_{DDA} / 2, Analog mode is selected. If connected to V_{DDA}, Digital Dimming mode with an external clock from the DD_CLK input controls the burst timing generator. Burst frequency is the external clock frequency divided by 512. If DIM_MODE is connected to Ground, Digital Dimming with an internal clock is selected. Burst frequency in internal clock mode is lamp current frequency divided by 512, and burst duty cycle is directly proportional to the voltage at BRITE_IN.
OC_SNS	Over Current Sense Input. A full wave AC voltage input centered on ground that is proportional to total high voltage transformer secondary winding current. The OC_SNS input is full wave rectified, and then applied to a digital comparator with a 2V reference to cause peak voltages greater than 2V to establish another regulation loop besides ISNS regulation loop. If an abnormal condition continues (>2V) then over current shut-off occurs. Frequency range of the input signal is 10 KHz to 500KHz. Normal operating voltage is less than ± 2V, and abnormal voltage can operate continuously as high as ± 7V peak under load fault conditions. Transients under fault conditions can reach ± 10VPK. Input voltage greater than ± 3V peak but less than ± 10V peak may cause saturation but will not cause malfunction, phase reversal, or reliability issues with the IC.
OV_SNS	Over Voltage Sense Input. A full wave AC voltage input centered around ground that is proportional to lamp voltage. The OV_SNS input will be full wave rectified, then applied to a digital comparator with a 2V reference to cause peak voltage greater than 2V to digitally reset the PWM logic on a pulse by pulse basis. Frequency range of the input signal is 10Khz to 500KHz. Normal operating voltage is less than ± 2V, and abnormal voltage can operate continuously as high as ±7V peak under load fault conditions. Transients under fault conditions can reach ± 10VPK. Input voltage greater than ± 3V peak but less than ± 10V peak may cause saturation but will not cause malfunction, phase reversal, or reliability issues with the IC. The input has a 20K ±12K (max over temperature) pull down resistor that serves as a DC restorer to the external capacitor that divides down lamp voltage.
I_SNS	Current Sense Input. A full wave AC voltage input centered around ground that is proportional to lamp current. The I_SNS input is full wave rectified and amplified, then presented to the inverting input of the current error amplifier. During the strike mode the current sense input will regulate to 2V regardless of BRITE_IN setting. Frequency range of the input signal is 10 KHz to 500KHz. Normal operating voltage is less than ± 2V, and abnormal voltage can operate continuously as high as ± 7V peak under load fault conditions. Transient under fault conditions can reach ± 10VPK. Input voltages of up to ± 3V peak are linearly rectified. Input voltage above ± 3V peak but less than ±10V peak may cause saturation but do not cause malfunction, phase reversal, or reliability issues with the IC.
EA_OUT	Error Amp Output. An external capacitor is connected from this pin to GND to adjust loop response of the inverter module. This capacitor value can vary from 10pF to 5000pF in various applications.
BRITE_IN	Brightness Control Input. The input signal should be a DC voltage or a filtered high frequency pulse width modulated digital signal. Active DC voltage range is 0.0 to 2.0V. On chip signal conditioning amplifiers clip inputs above 2V.
ENABLE	Chip Enable Input. If logic high, all functions are enabled. If logic low, internal power is disconnected from the V_{DDP} pin, disabling all functions. Maximum current into V_{DDP} when ENABLE < 0.3V, V_{DDP}<5V, is 10µA. ENABLE may be connected directly to V_{DDP} if the disable function is not used.
I_R	Current Reference Resistor Input. Connects to an external resistor that determines the magnitude of internal bias currents. The nominal lamp frequency can be adjusted by varying this resistor value in the range of 40K to 100K Ohms. $I_{I\_R} = \frac{1.00V}{R_{I\_R}}$

*See dimming mode truth table for a summary of dimming operation with respect to DD_CLK & DIM_MODE inputs.

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FUNCTIONAL PIN DESCRIPTION (CONTINUED)

PIN NAME	DESCRIPTION
BRITE_OUT	Brightness Reference Current Output. This variable current source is the mirror of BRITE_R current multiplied by the BRITE_IN signal and becomes the reference voltage to the error amplifier when DIM_MODE is open or ½ V_{DDA}. Connecting an additional resistor to VDDA determines minimum lamp current in order to prevent fault condition. A light sensor (LX1970) may be used in conjunction with BRITE_OUT to change amplitude of lamp current in response to ambient light intensity. $V_{BRITE\ OUT} = V_{BRITE\ IN}$ X BRITE_OUT/BRITE_R (When DD_CLK is connected to V_{DDA}) $V_{BRITE\_OUT} = (2\text{-}V_{BRITE\_IN})$ X BRITE_OUT/BRITE_R (When DD_CLK is connected to GND) When DIM_MODE is GND or V_{DDA}, then BRITE_OUT has to be biased with an external resistor.
BRITE_R	Dedicated bias resistor for BRITE_OUT current source when DIM_MODE is open or ½ $V_{DDA.}$ Connecting an additional resistor to VDDA determines minimum Burst Duty Cycle in digital dimming. A light sensor (LX1970) may be used in conjunction with BRITE_R to change Burst Duty Cycle in response to ambient light intensity.

DIMMING TABLE

DESCRIPTION	DIM_ MODE	DD_ CLK	CONDITIONS
Reversed Internal Digital Dimming Internally Clocked PWM Burst Generator, External Input to BRITE_IN	0V	Low	Voltage at BRITE_IN controls lamp current burst duty cycle. Duty cycle is inversely proportional to voltage at BRITE_IN. Burst period is LX1691 oscillator frequency divided by 1024 (lamp current frequency divided by 512). An external voltage connected to the BRITE_OUT pin sets lamp current amplitude.
Conventional Internal Digital Dimming Internally clocked PWM Burst Generator, External Input to BRITE_IN		High	Voltage at BRITE_IN controls lamp current burst duty cycle. Duty cycle is directly proportional to voltage at BRITE_IN. Burst period is LX1691 oscillator frequency divided by 1024 (lamp current frequency divided by 512). An external voltage connected to the BRITE_OUT pin sets lamp current amplitude
Conventional External Digital Dimming Externally clocked PWM burst generator, external input to BRITE_IN	VDDA	Pulse	Voltage at BRITE_IN controls lamp current burst duty cycle. Duty cycle is directly proportional to voltage at BRITE_IN. Burst period is DD_CLK input divided by 512. An external voltage connected to the BRITE_OUT pin sets lamp current amplitude.
Reversed Analog Amplitude Dimming	½ VDDA or open	Low	Voltage at BRITE_IN controls lamp current amplitude. Amplitude is inversely proportional to voltage at BRITE_IN.
Conventional Analog Amplitude Dimming		High	Voltage at BRITE_IN controls lamp current amplitude. Amplitude is directly proportional to voltage at BRITE_IN.
Conventional Analog Amplitude Dimming with External Direct PWM Control		Pulse	Voltage at BRITE_IN controls lamp current amplitude. Amplitude is directly proportional to voltage at BRITE_IN. Burst period and duty cycle are directly proportional to signal at DD_CLK input pin. If held low, duty cycle is 0% (Zero duty will cause a fault shut down. Minimum duty to prevent fault shut down is lamp and temperature dependent. User must characterize lamp to determine minimum duty cycle.). If held high, duty cycle is 100% (full brightness).

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RECOMMENDED OPERATING CONDITIONS

Parameter	LX1691			Units
	Min	Typ	Max	
Supply Voltage (V_{DDP})	2.8		5.5	V
Digital Input (ENABLE)	0		5.5	V
Analog Inputs (I_SNS, OC_SNS, OV_SNS)	-2		2	V_{PK}
BRITE_IN Linear DC Voltage Range	0		2	V
BRITE_OUT, BRITE_R Maximum Source Current			100	µA
Digital Inputs (DIM_MODE, DD_CLK)	0		5.5	V
Internal Oscillator Frequency (I_R Resistor Range 42K to 175K)	60		250	KHz
Maximum Output Gate Charge (A_{OUT}, B_{OUT})		10	20	nC

ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, the following specifications apply over the operating ambient temperature -40°C ≤ T_A ≤ 85°C except where otherwise noted. Test conditions: V_{DDP} =3.3 to 5.5 V, I_R =80.6KΩ, BRITE_R = BRITE_OUT = 20KΩ, OVSNS = OCSNS = 0V, DD_CLK = DIM_MODE = Floating

Parameter	Symbol	Test Conditions	LX1691			Units
			Min	Typ	Max	
POWER						
Power Supply Input Voltage	$V_{\_BATT}$		2.8		5.5	V
Regulator Output Voltage	V_{DDA}	V_{DDP}= 3.3 to 5.5V, I Load = 0 mADC	2.85	3.0	3.15	V
V_{DDA} Drop Out Voltage	$V_{DROPOUT}$	I Load = 0 mADC		50	150	mV
V_{DDP} Operating Current	I_{BB}	C_{AOUT} = C_{BOUT} = 1000pF; f_{OSC} = 130kHz		10	15	mA
Sleep Mode Current	I_{DD_SLEEP}	V_{ENABLE} = 0.8V, V_{DDP} = 5.5V		10		µA
ENABLE INPUT						
Run Threshold	V_{TH_ENRUN}			1.5	2.8	V
Shutdown Threshold	V_{TH_ENSHDN}		0.8	1.1		V
Input High Current	I_{IH_ENABLE}	ENABLE = 2V		2	12	µA
Input High Current	I_{IH_ENABLE}	ENABLE = 5V		35	80	µA
Input Low Current	I_{IL_ENABLE}	ENABLE = 0V	-1	0	1	µA
UNDER VOLTAGE LOCKOUT						
Startup Threshold	V_{TH_UVLO}	Run Mode		2.55	2.8	V
UVLO Threshold		Shutdown Mode	2.1	2.35		
UVLO Hysteresis	V_{H_UVLO}			200		mV
BIAS BLOCK						
Voltage at Pin I_R	$V_{\_IR}$	80.6K	0.975		1.025	V
Pin I_R Max Source Current	I_{MAX_IR}			100		µA
Voltage Reference Voltage (Internal node)	V_{2P0}		1.98		2.02	V
OUTPUT BUFFER BLOCK						
Output Sink Current	I_{SK_OUTBUF}	V_{AOUT}, V_{BOUT} = V_{DDP}		100		mA
Output Source Current	I_{S_OUTBUF}	V_{AOUT}, V_{BOUT} = 0V		100		mA

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Test Conditions	LX1691			Units
			Min	Typ	Max	
RAMP GENERATOR						
Max Strike / Run Frequency Ratio	F_{RAMP_STK}	Ratio to run frequency, I_SNS = OV_SNS = 0V		3		
Maximum Lamp Run Frequency	F_{RAMP_RUNMAX}	Lamp is ignited; I_R = 20K	250	262		KHz
Lamp Run Frequency	F_{LAMP_RUN}	Lamp is ignited, I_R = 80.6K, T_A = 25°C	63	65	67	KHz
Lamp Run Frequency	F_{LAMP_RUN}	Lamp is ignited, I_R = 80.6K	61	65	69	KHz
Lamp Run Frequency Regulation over V_{DDP}	F_{LAMP_REG}	$3.3 \leq V_{DDP} \leq 5.5V$		0.1		%
Internal Digital Dimming Burst Frequency	F_{BURST}	DIM_MODE = 0V, F_{LAMP_RUN} / 512, I_R = 80.6K		127		Hz
PWM BLOCK						
Error Amp Transconductance	G_{M_EAMP}		60	150		µmho
Error Amp Output Source Current	I_{S_EAMP}			100		µA
Error Amp Output Sink Current	I_{SK_EAMP}			100		µA
Error Amp Output High Voltage	V_{H_EAMP}	BRITE_OUT – EA_IN = 50mV	2.5	2.9		V
Error Amp Output Low Voltage	V_{L_EAMP}	EA_IN – BRITE_OUT = 50mV		0.015	0.5	V
Error Amp Input Offset Voltage	V_{OS_EAMP}				30	mV
Max Duty Cycle	DC_{MAX}			47		%
Ramp Valley Voltage	R_{VV}			100		mV
Ramp Peak Voltage	R_{PV}			2.1		V
DD_CLK INPUT						
Pull-up Resistance		To V_{DDA}		50		KΩ
Input High Threshold	$V_{TH\_DD\_CLK}$	Conventional Dimming		1.6	2.0	V
Input Low Threshold	$V_{TL\_DD\_CLK}$	Reverse Dimming	0.4	0.9		V
Input High Current	$I_{IH\_DD\_CLK}$	DD_CLK = 5V; VDDP=5V		45	70	µA
Input Low Current	$I_{IL\_DD\_CLK}$	DD_CLK = 0V; VDDP=5V		-65	-100	µA
DIM_MODE INPUT						
Low State	$V_{TL\_TRI\_}$		0.4	0.85		V
Floating State	V_{TF_TRI}		1.2	1.35	1.8	V
High State	V_{TH_TRI}			2.35	2.8	V
Input High Current	I_{IH_TRI}	DIM_MODE = 5V		70	120	µA
Input Low Current	I_{IL_TRI}	DIM_MODE = 0V		-25	-50	µA
ANALOG DIMMER BLOCK						
BRITE_IN Input Current	BRITE_IN $_{II}$	BRITE_IN = 0 to 5V	-1		1	µA
Conventional Dimming BRITE_OUT		BRITE_IN = 0V	0	25	60	mV
		BRITE_IN $\geq$ 2.05V	1.9	2.0	2.10	V
		BRITE_ IN $\leq$ 0V	1.9	2.0	2.1	V
		BRITE_IN $\geq$ 2.05V	0	25	60	mV

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Test Conditions	LX1691 Min	LX1691 Typ	LX1691 Max	Units
DIGITAL DIMMER BLOCK						
Conventional Dimming Duty Cycle		Minimum Duty Cycle; BRITE_IN = 0.1V	2	5	7	%
		Maximum Duty Cycle; BRITE_IN =1.90V	90	95	100	%
		Maximum Duty Cycle; BRITE_IN ≥ 2.05V	100			%
Reverse Dimming Duty Cycle		Maximum Duty Cycle; BRITE_IN = 0.0V	100			%
		Maximum Duty Cycle; BRITE_IN = 0.1V	90	95	100	%
		Minimum Duty Cycle; BRITE_IN = 1.95V	2	5	7	%
TIMING GENERATOR BLOCK						
Number of Lamp Return Current Cycles before Run Mode	N_{IGNITE}	To switch to Run Mode		4		Cycles
I_SNS Run Mode Checking Interval		Lamp return current cycles		2048		Cycles
Strike Validation Threshold		To switch to run mode, T_A =25°C		700		mV_{PK}
Fault Comparator Threshold Run		I_ SNS Open Lamp Fault Detect, T_A =25°C		300		mV_{PK}
Number of Strike sweep Attempts Before Fault Shutdown	N_{STRK_FAULT}	FLAMP Sweep Cycles, I_SNS = 0V_SNS = 0V		6		
Power On Delay Before Strike	T_{D_PWRON}	I_R = 80.6K		125		ms
Number of Sweeping Strike Frequency Steps per Attempt				512		Steps
Number of Output Pulses per Striking Step				16		Cycles
LAMP FEEDBACK CONDITIONING BLOCK						
I_SNS Input Current	I_SNS_{IIN}	I_SNS = +2.5V		14		µA
		I_SNS = -2.5V		-40		µA
OV_SNS Input High Threshold	$V_{TH\_OV\_SNS}$	Active Over Voltage Protection		± 2.2		V_{PK}
OV_SNS Input Low Threshold	$V_{TL\_OV\_SNS}$	Inactive Over Voltage Protection		± 1.8		V_{PK}
OV_SNS Input Current	OV_SNS_{IIN}	OV_SNS = +2.5V		140		µA
		OV_SNS = -2.5V		-170		µA
OC_SNS Input High Threshold	$V_{TH\_OC\_SNS}$	Active Over Current Protection		± 2.2		V_{PK}
OC_SNS Input Low Threshold	$V_{TL\_OC\_SNS}$	Inactive Over Voltage Protection		± 1.8		V_{PK}
OC_SNS Input Current	OC_SNS_{IIN}	OC_SNS = 10V		14		µA
		OC_SNS = -2.5V		-40		µA
Full Wave Rectifiers RMS Transfer	I_SNS_{RMS}	I_SNS = 0.3VDC, T_A = 25°C		0.3		V
		I_SNS = 2.5VDC, T_A = 25°C		2.5		V
		I_SNS = -0.3VDC, T_A = 25°C		0.3		V
		I_SNS = -2.5VDC, T_A = 25°C		2.5		V

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BLOCK DIAGRAM

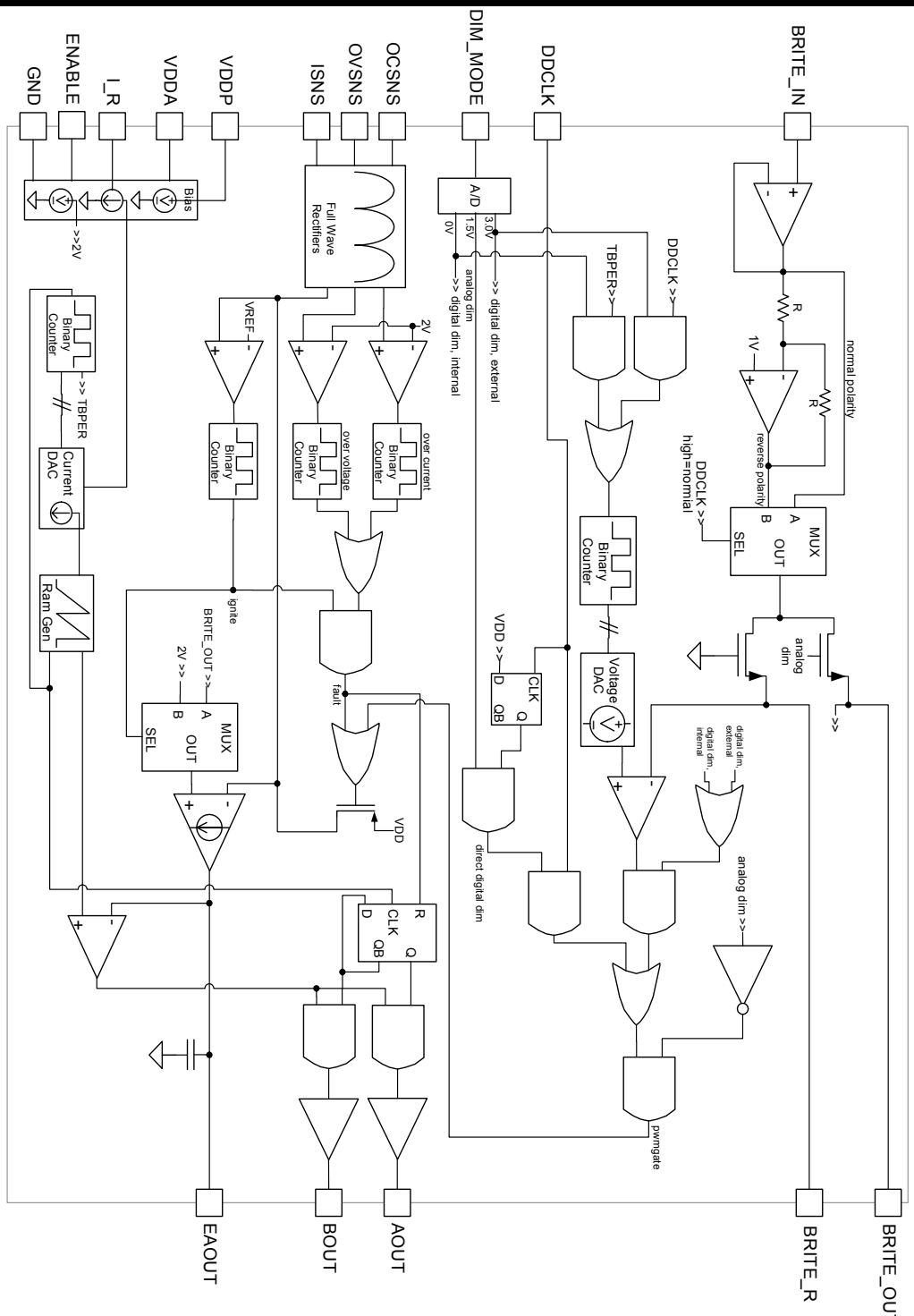

FIGURE 1 – Simplified Block Diagram

TYPICAL APPLICATION

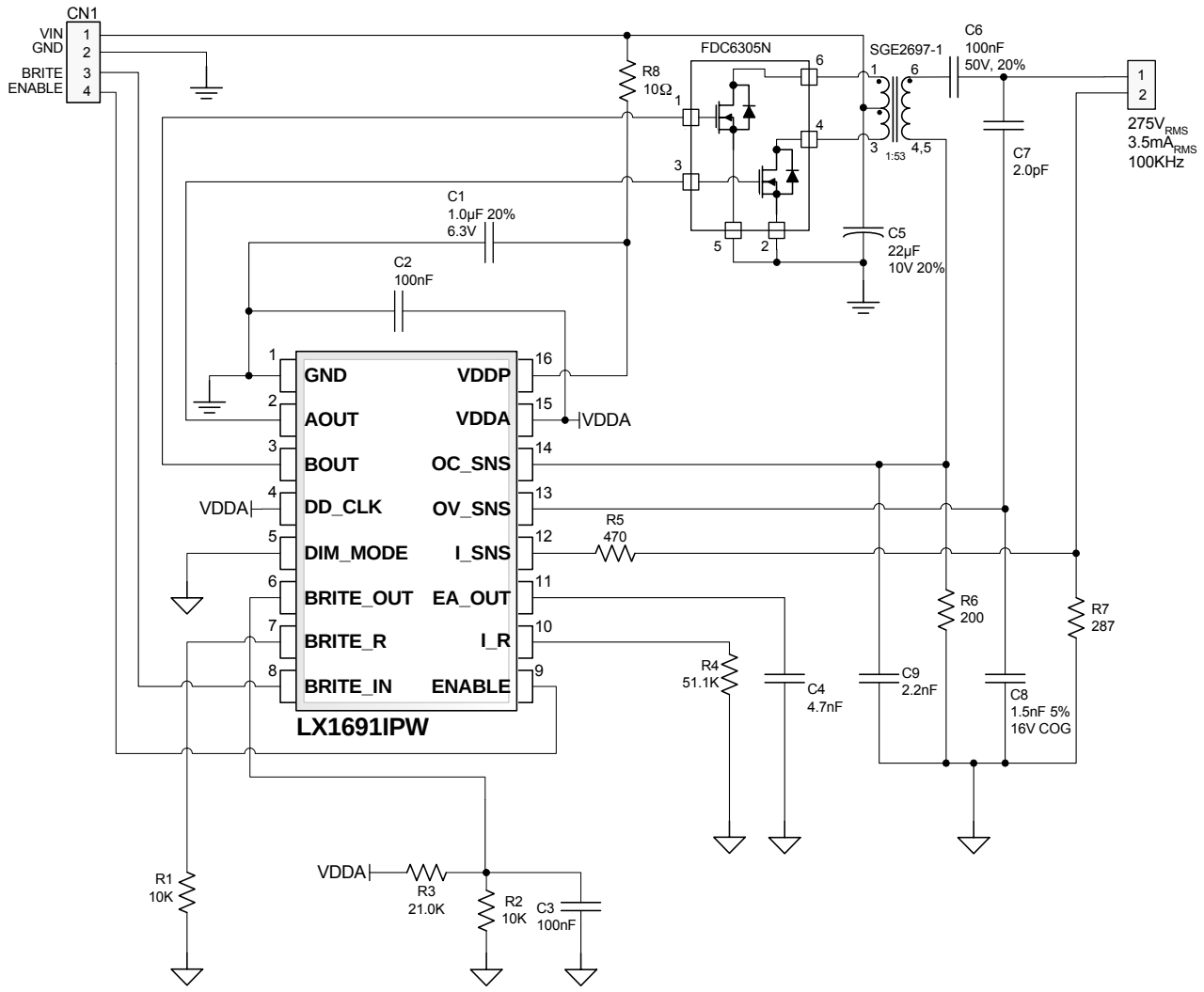

FIGURE 2 – LX1691 Inverter for PDA With Single Cell LI_ION Battery, Digital Dimming maximum current of 3.5mA$_{RMS}$ @ 100KHz set to 1.33mA via R2/R3.

Brite Input Control Range (Linear DCV)
Min. Brite 'Lo' = 150mV
Max. Brite 'Hi' = 2.0V
Burst Rate Frequency = 200 Hz
Enable Input
Off Logic 'Lo' <= 0.80V
On Logic 'Hi' >= 1.7V

Lamp Current mA$_{RMS}$	R3	R7
5.0	21.0K	200
4.5	21.0K	221
4.0	21.0K	249
3.5	21.0K	287
3.0	32.4K	249
2.5	32.4K	294
2.0	60.4K	226
1.5	60.4K	301

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DETAILED DESCRIPTION

FEATURE REVIEW

On-Chip LDO Regulator

An LDO regulator keeps critical analog control circuits operating optimally over the entire input voltage range. Brightness control voltage and operating frequency are extremely stable.

Under Voltage Lockout

If the battery input voltage is too low for the controller to function properly, it will turn itself off, preventing spurious operation. If the battery voltage falls to less than 1V where UVLO is no longer guaranteed, 10K pull down resistors on the A_{OUT} and B_{OUT} pins insure the external power FETs cannot be biased on.

Power On Delay

A power up reset that delays A_{OUT} and B_{OUT} turn on for approximately 100 milliseconds after power is applied. This give extra time for the BRITE_IN source voltage to stabilize so the lamp is not inadvertently powered up at high brightness and then suddenly lowered, creating an undesirable light flash.

Enhanced BRITE Conditioning Circuitry

The BRITE_IN pin offers a high impedance input with a linear control range of 0 to 2.0V The function of the pin depends on which of six dimming modes the controller is programmed. (see dimming table page 4) A new feature of the LX1691 allows the DD_CLK input to control the burst frequency and duty cycle while the BRITE_IN input controls the output current amplitude (see additional information below).

Digital or Analog Dimming Modes

A DIM_MODE input pin selects either Analog or Digital mode. In Analog mode DC voltage at BRITE_IN controls lamp current amplitude. In Digital mode it controls digital dimming duty cycle. When in Digital mode, the dimming burst frequency can be synchronous to lamp current by selecting internal clocking, or to an external clock. With an external clock source, burst frequency will be the clocks frequency divided by 512. When using the internal clock source the burst frequency will be the internal oscillator divided by 1024 which is equivalent to lamp current frequency divided by 512.

Brightness Polarity and Dual Mode Dimming Control

In Analog dimming mode the IC can be programmed to either increase or decrease lamp current amplitude as a function of increasing signal at the BRITE_IN pin by simply connecting the DD_CLK input to V_{DDA} or ground (see Dimming Table). If simultaneous amplitude control and digital dimming is desired, apply a PWM signal to DD_CLK. The lamp current waveform will exactly follow DD_CLK (DD_CLK is not divided in this mode); e.g., lamp current flows when DD_CLK is high and stops when it is low.

In Digital dimming mode, lamp current duty cycle is either directly or inversely proportional to DC input voltage at the BRITE_IN pin, depending on the state of DD_CLK. If external clock is selected, duty cycle will be directly proportional to voltage at BRITE_IN and the burst period will be DD_CLK period X 512.

Lamp current amplitude can be set and varied by applying a separate DC voltage at the BRITE_OUT pin. This voltage can range from zero to 2.0 VDC. Zero volts will produce zero current (and therefore a lamp fault). 2.0V will produce the maximum current as defined by the value of the current sensing resistor from I_{SNS} to GND.

Strike Voltage Generation

Improved strike voltage generation circuits ramp strike voltage slowly to programmed maximum potential and hold it there for approximately 350mSec @65Hz operating frequency. This insures a worst case lamp will strike at any temperature. Strike potential is removed immediately when the lamp strikes or if the time limit is reached.

Strike Detection

The LX1691 includes a new lamp strike detection scheme that saves a package pin and three external components. Internal circuits monitor lamp current pulses at the I_SNS input to determine if the lamp strikes and if it stays ignited once operational.

Fault Time Out

If the lamp fails to ignite within approximately 350mSec, or if it extinguishes after ignition, or if the clock signal at the DD_CLK pin terminates when in external digital dim mode, the output drive is shut down.

Fault mode will also be invoked if the lamp is short circuited or left open for more than 350mSec.

On Chip Rectifiers

Integrating full wave rectifiers for each of three lamp inputs significantly reduces lamp feedback component count. Current Sense (I_SNS), Over Current Sense (OC_SNS) and Over Voltage Sense (OV_SNS) signals are detected using only one external scaling resistor or capacitor each. Rectification accuracy is improved with high performance on chip rectifiers to provide better lamp current and voltage regulation.

Complete Fault Protection

In addition to the lamp fault time out, maximum output voltage and current under all fault conditions is regulated. Open circuit voltage can never go higher than the preset maximum strike potential and total current from the circuit is safely limited with a scaling resistor. UL safety specifications can now be easily met in any application.

Familiar Magnetics

The LX1691 can use the same magnetics as all other Direct Drive controllers. Refer to Application Note 13 for transformer design and power FET selection criteria.

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DETAILED DESCRIPTION (CONTINUED)

LX1691 Operation

Four operating modes: Power On Delay, Strike, Run, and Fault modes are employed by the LX1691. Upon power up or ENABLE going true, Power On Delay is automatically invoked. Immediately after termination of Power On Delay, or ENABLE going true, strike mode is entered. After a successful strike, e.g., lamp is ignited, run mode is entered. If ignition is unsuccessful, or if the lamp extinguishes while running, Fault mode is entered. Lamp ignition is determined by monitoring the lamp current feedback voltage at pin I_SNS. Lamp current cycles are counted from the beginning of Strike mode. If 4 or more complete cycles occur the lamp is declared ignited. If less than 4, the lamp is considered not ignited and Strike mode continues until ignition is detected or strike time out (approximately 350ms) is reached.

After run mode is entered lamp current pulse count is sampled several times a second to determine that the lamp has not inadvertently extinguished. If lamp current pulses are counted in each sample, Run mode is maintained. Otherwise, Fault mode is entered. Strike mode can be entered only once for each on/off cycle of either V_{DDP} or ENABLE. This insures that even intermittent lamp failures cannot cause the module to continuously output maximum strike voltage.

During strike, operating frequency is swept from the normal run value approximately to 3X run frequency. This will excite the unloaded resonant frequency of the transformer and lamp load to generate the required lamp striking voltage. If the lamp has not ignited after about 350mS, a fault is declared and the A & B outputs are shut off.

If while strike frequency is sweeping, the over voltage set point at OV_SNS is detected or overcurrent voltage set point at OV_SNS is deteted the, strike frequency will hold at the frequency value until either the lamp strikes or the timeout is reached. This causes maximum strike potential to be continuously impressed across the lamp for the entire strike period.

Also, if while strike frequency is sweeping, the over current set point at OC_SNS is detected, strike frequency will hold at the present value until either the lamp strikes or the timeout is reached. This insures short circuit current regulation will be maintained, thus enabling UL fault requirements to be easily met at the inverter module level.

The only way to re-initiate the strike process is to either cycle VDDP or ENABLE off and on.

If ignition is successful, ramp frequency immediately returns to its programmed run value.

Power ON Delay Mode

All functions are activated except that AOUT and BOUT are inhibited. Delay is in the 100mSec range and is determined by a counter. Power on delay is activated at every V_{DDP} power up sequence and ENABLE sequence.

Strike Mode

Entered from Power On Delay, or upon an ENABLE sequence. Control of the Ramp Generator frequency is switched to the DAC output. Frequency is increased from its normal run value to up to three times that value for up to 6 sweeps If while strike frequency is sweeping, the set points at OV_SNS and / or OC_SNS are detected, strike frequency will freeze at the present value until either the lamp strikes or the timeout is reached. Strike Mode is terminated by reaching 6 sweep counts or by detecting lamp ignition. If strike is successful, Run Mode is entered. If unsuccessful, Fault mode is entered.

Run Mode

Entered only by detection of a successful Strike. Frequency control is immediately switched to a fixed reference that sets the programmed run frequency. The lamp current cycle counter is monitored to insure at least 4 current cycles received during each period. If less than 4, the lamp is considered extinguished and the Fault Mode is entered.

Fault Mode

Fault Mode may be entered from either Strike or Run Mode as described above. In Fault Mode, the A & B output buffers are forced low. Fault mode may be cleared by cycling ENABLE off then on, or by removing and applying V_{DDP}.

Design Procedure

Selecting the I_R resistor value

This resistor determines the value of several internal reference currents that control timing. It must be chosen first, and will be in the range of 40 to 120K ohms. We use an 80.6K, 1% low TCR value in our designs to set nominal lamp current frequency to 65kHz. The output frequency is approximated by the following formula: $R_{I\_R} = 5.24E9 / F_{LAMPOUT/HZ}$.

Driving the BRITE_IN Input

The BRITE_IN input circuitry includes on-chip active voltage clamps that ignore input voltage greater than 2.0V. Input impedance is very high so it can also be driven from a 100K potentiometer with no offset error. BRITE_IN can be a DC voltage, or a higher frequency externally filter PWM The BRITE_IN input has a linear active range between 0.0 and 2.0V

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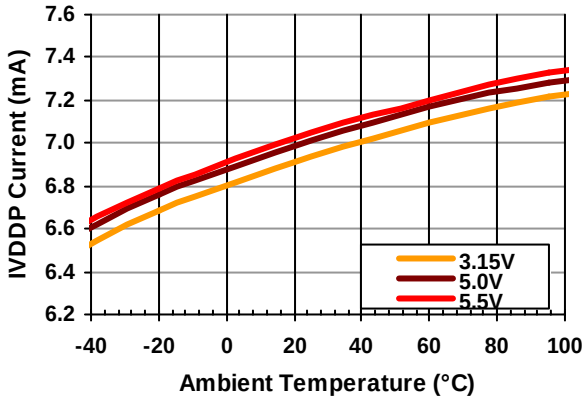
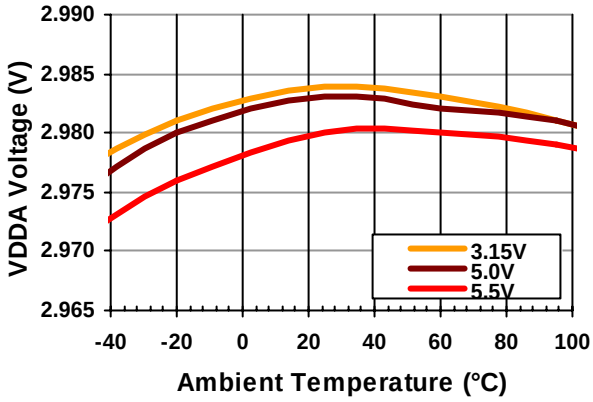
IVDDP OVER TEMPERATURE



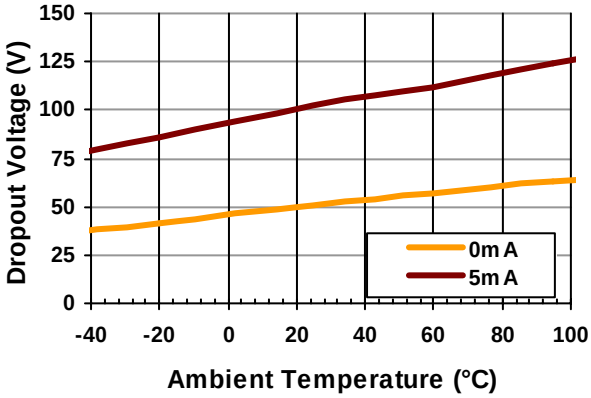
IVDDP over Temperature

VDDA OVER TEMPERATURE



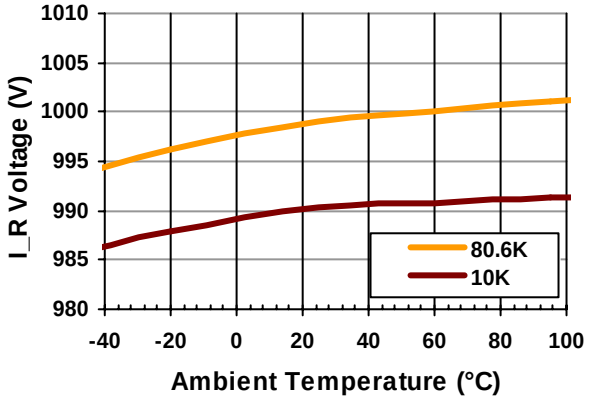
VDDA Over Temperature

VDDA DROPOUT VOLTAGE



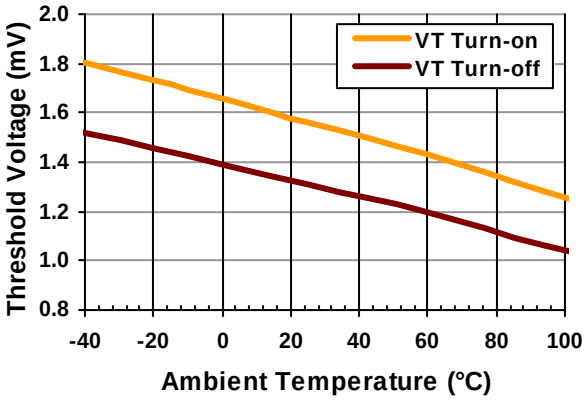
VDDA Dropout Voltage over Temperature

I_R VOLTAGE OVER TEMPERATURE



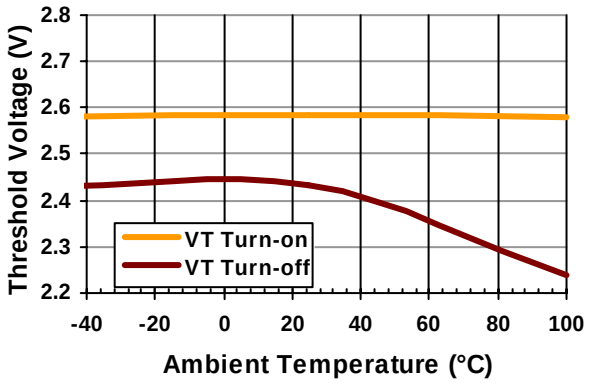
I_R Voltage over Temperature

ENABLE THRESHOLD OVER TEMP



Enable Threshold over Temperature

UVLO THRESHOLD OVER TEMP



UVLO Threshold over Temperature

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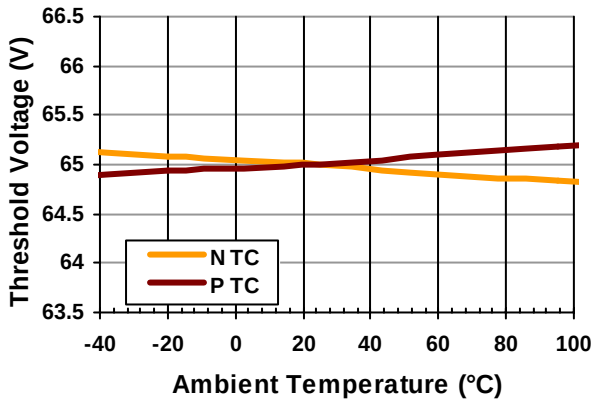
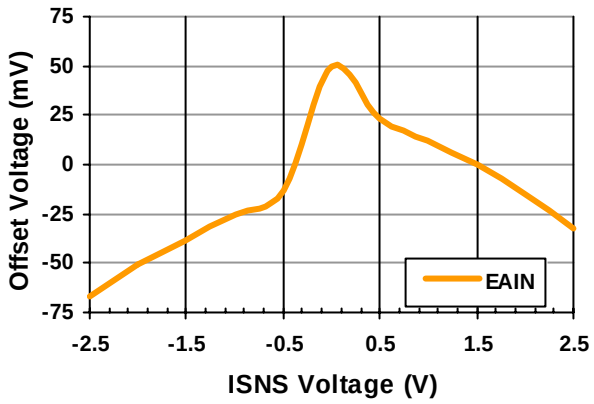
LAMP FREQ OVER TEMPERATURE



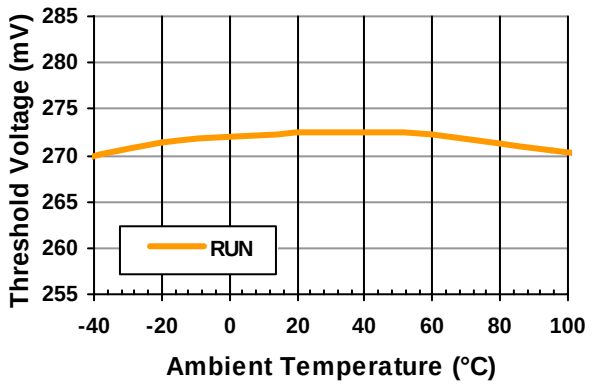
Lamp Frequency over Temperature

FWRECT TRANSFER OFFSET



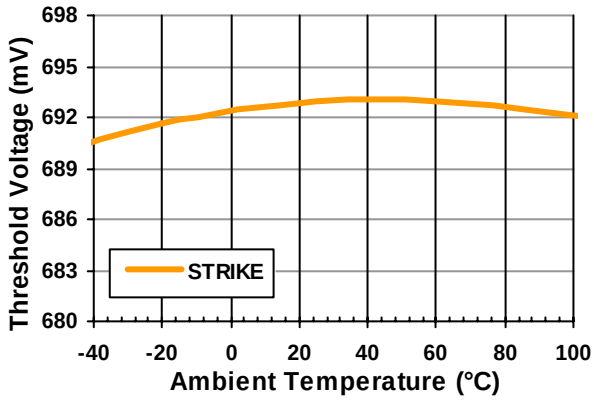
FWRECT Transfer Offset

FAULT THRESHOLD OVER TEMP



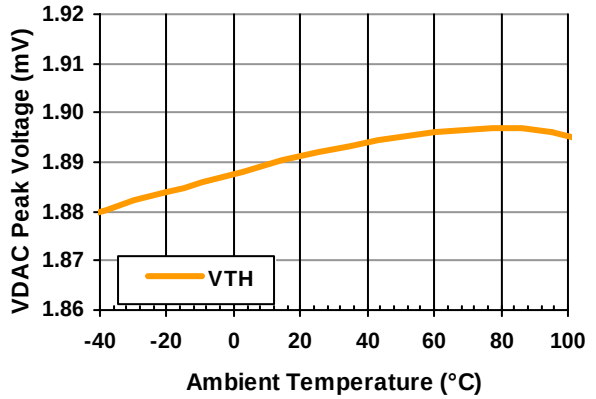
Fault Threshold over Temperature

STRIKING THRESHOLD OVER TEMP



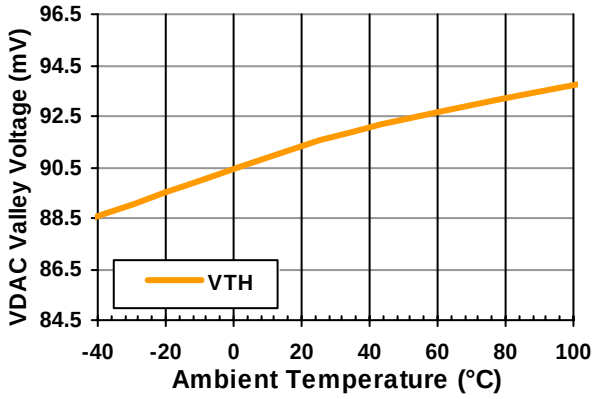
Striking Threshold over Temperature

VDAC PEAK OVER TEMPERATURE



VDAC Peak over Temperature

VDAC VALLEY OVER TEMPERATURE



VDAC Valley over Temperature

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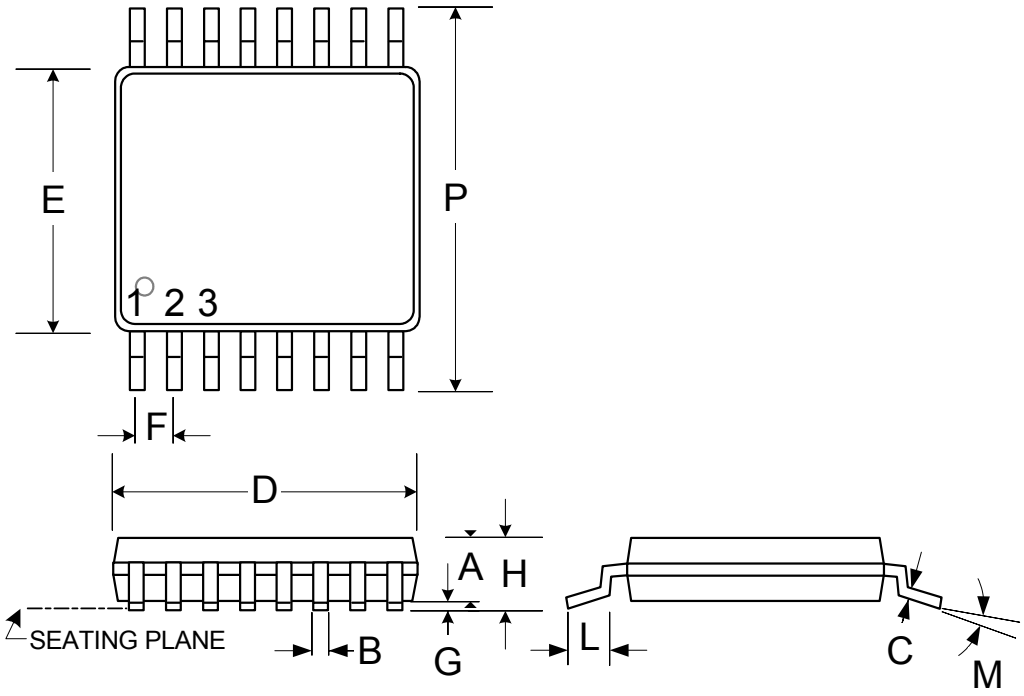
MECHANICAL DRAWING

PW 16-Pin Thin Small Shrink Outline (TSSOP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	0.95	0.033	0.037
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.10	0.192	0.200
E	4.30	4.50	0.169	0.177
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H	–	1.10	–	.0433
L	0.50	0.75	0.020	0.030
M	0°	8°	0°	8°
P	6.25	6.50	0.246	0.256
*LC	–	0.10	–	0.004

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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