Microsemi

LX1701

2W Filterless Mono Class-D Audio Amplifier

PRODUCTION DATA SHEET

DESCRIPTION

The LX1701 family represents a new generation of a fully integrated audio mono class-D amplifier from Microsemi. This CMOS monolithic class-D amplifier series is optimized for low voltage, low power operation and minimum system cost. The products are ideal for use in battery powered applications where low power consumption is desirable such as cell phones, PDA's, web tablets and other low power systems.

The LX1701 family provides very low quiescent current consumption through the use of a proprietary output modulation scheme. This technology enables filter-less operation in many applications. The part features on board, low Rdson, complementary output MOSFET's that reduces the need for external components.

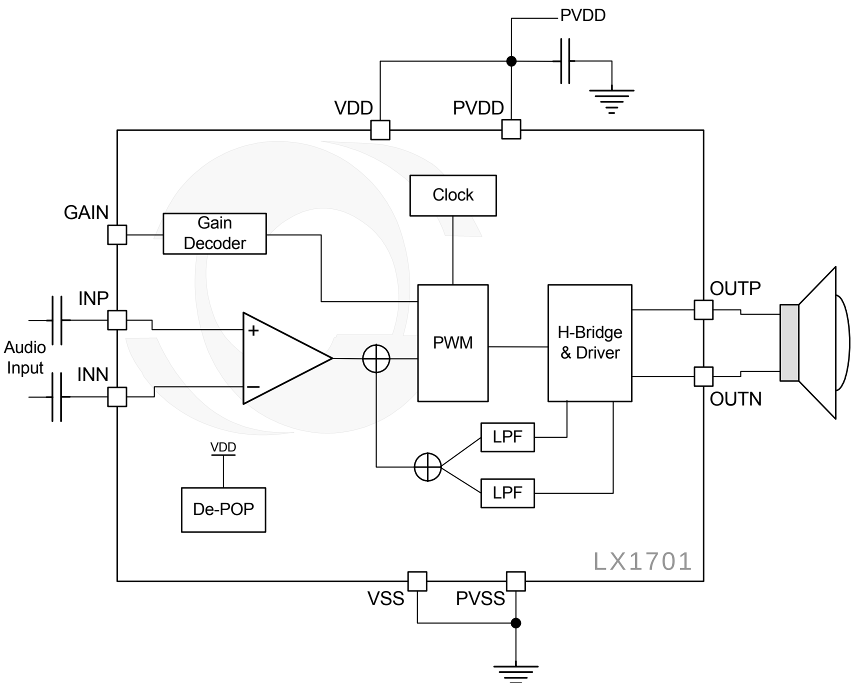
The LX1701 is offered in a small footprint, low profile surface mountable 16-pin MLPQ package.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

KEY FEATURES

- No Output Filter Required
- Low EMI Design
- Low Quiescent Current: 2mA
- Low Shutdown Current:1µA
- Low And Wide Supply Voltage Range: 1.8-6.0 Volt
- 2W Output Power Into 4Ω Load With THD<1%
  3W Into 2Ω With THD<1%
- THD+N As Low As 0.09%
- Small Form Factor: 16-pin MLPQ Package: 4mmx4mm
- -40 to +85°C Operating Range
- Only **1** External Component Needed, No Input AC Coupling Capacitor Required, Under Certain Conditions
- Built-in Clock Frequency 200KHz
- Built-in Feedback Loop, Allows High Audio Fidelity
- 14dB/8dB Gain Selectable
- 20/300Hz Bandwidth Selectable
- Shut-down Function
- Internal Thermal Shut-down
- High Efficiency: 85% Through Modulation Scheme And Class-D Operation
- Built-in De-pop Circuit, No Turn ON/OFF "POP" Noise

PRODUCT HIGHLIGHT



APPLICATIONS/BENEFITS

- PDA's
- Cell Phones
- Portable Audio
- Laptop Computer Speaker Amplifier
- LCD TV/Desktop Monitor Speaker Amplifier
- PC Audio Multimedia Amplifier

PACKAGE ORDER INFO

T_J (°C)	Bare Die	LQ Plastic MLPQ 16-Pin
-40 to 85	LX1701	LX1701CLQ

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1701CLQTR)

WWW.Microsemi.COM

LX1701

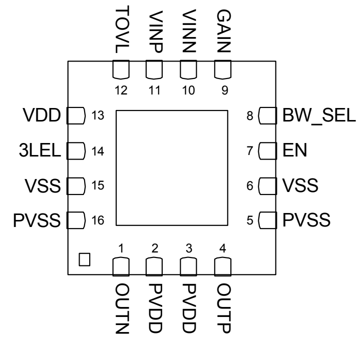
Microsemi
Integrated Products Division
11861 Western Avenue, Garden Grove CA. 92841 714-898-8121, FAX 714-893-2570

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (VDD, PVDD).. -0.3 to 7.0V
Operating Temperature ....-40°C to +85°C
Maximum Operating Junction Temperature .... 150°C
Storage Temperature...-65°C to 150°C
Lead Temperature (Soldering, 10 seconds) .... 300°C
Package Peak Temp for Solder Reflow(40 second maximum exposure)...... 250°C (+5, -0)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



LQ PACKAGE
(Top View)

Pb-free 100% Matte Tin Finish

THERMAL DATA

LQ **Plastic Micro Lead Quad Package 16-Pin**

THERMAL RESISTANCE-JUNCTION TO CASE, θ_{JC}	3.22°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	38.1°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow. Thermal Test Board: JESD5-7 (Leaded Surface Mount Package)

FUNCTIONAL PIN DESCRIPTION

Name	Description
OUTN	Negative Audio (PWM) Output
PVDD	Positive Supply to Negative Output Stage
PVDD	Positive Supply to Positive Output Stage
OUTP	Positive Audio (PWM) Output
PVSS	Negative Supply to Positive Output Stage (ground)
VSS	Negative Supply to Analog Stage (ground)
EN	Enable Pin, Active High.
BW_SEL	Bandwidth Selection Pin: VDD 300Hz HP filter VSS No HP (< 20Hz)
GAIN	Gain Selection Pin: Tied to VDD Gain = 14dB Tied to VSS Gain = 8dB
VINN	Negative Audio Input
VINP	Positive Audio Input
TOVL	Thermal Overload Indicator Output, Active HIGH.
VDD	Analog Positive Power Supply
3LVL	Three Level Modulation Selection Pin: Tied to VSS 2 LEVEL PWM Modulation Scheme, +PVDD | -PVDD; Tied to VDD 3 LEVEL PWM Modulation Scheme, +PVDD | PVSS | -PVDD;
VSS	Negative Power Supply to Analog Stage
PVSS	Negative Supply to Negative Output Stage (ground)

SYSTEM CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature T_A = 25°C except where otherwise noted and the following test conditions: Default settings: 20Hz corner low frequency, 14dB gain.

Parameter	Symbol	Test Conditions		LX1701 Min	Typ	Max	Units
Supply Current, Quiescent	IQQ	No Load, VDD = PVDD = 1.8V			0.9	1.2	mA
		No Load, VDD = PVDD = 3.3V			1.3	1.8	
		No Load, VDD = PVDD = 5.0V			2.0	2.5	
Supply Current, Shutdown Mode	IQQSD	Disable pin active				1	µA
Output Power @ 8 Ohms	PO	VDD = PVDD = 5V, Fin = 1kHz	THD+N = 1%		1.3		W
			THD+N = 10%		1.8		
		VDD = PVDD = 3.3V, Fin = 1kHz	THD+N = 1%		0.5		
			THD+N = 10%		0.7		
Output Power @ 4 Ohms	PO	VDD = PVDD = 5V, Fin = 1kHz	THD+N = 1%		2.1		W
			THD+N = 10%		2.8		
		VDD = PVDD = 3.3V, Fin = 1kHz	THD+N = 1%		0.9		
			THD+N = 10%		1.2		
Output Power @ 2 Ohms	PO	VDD = PVDD = 5V, Fin = 1kHz	THD+N = 1%		3.0		W
			THD+N = 10%		3.9		
		VDD = PVDD = 3.3V, Fin = 1kHz	THD+N = 1%		1.3		
			THD+N = 10%		1.8		
Power Efficiency	η	VDD = PVDD = 5V, Fin = 1kHz, RL = 8 Ω			85		%
Total Harmonic Distortion @ 50% of Max Power	THD+N	VDD = PVDD = 5V, Fin = 1kHz, RL = 8 Ω			0.09		%
Signal-to-Noise Ratio	SNR	VDD = PVDD = 5V, F = 1KHz, PO = 1W, A-Weighted			99		dB
Output Noise Floor	VN	Input Grounded A-weighted 20-20kHz			25		μV_{RMS}
Frequency Response Lower Corner Frequency	FLO	3dB relative to 1kHz, BW Select = VSS			20		Hz
	FHI	3dB relative to 1kHz, BW Select = VDD			300		Hz
Frequency Response		VDD = PVDD = 1.8 to 5.5V, RL = 4 Ω , PO = 200mW @ 20~80KHz, filterless				3	dB
Power Supply Rejection Ratio	PSRR	VDD = PVDD = 1.8V to 5.5V			65		dB
Common Mode Rejection Ratio	CMRR	VDD = PVDD = 1.8V to 5.5V			70		dB
Gain	GSYS	Pin 9 tied to VDD, VDD = PVDD = 1.8V to 5.5V			14		dB
		Pin 9 tied to VSS, VDD = PVDD = 1.8V to 5.5V			8		

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature -40°C ≤ T_A ≤ 85°C except where otherwise noted.

Parameter	Symbol	Test Conditions		LX1701 Min	LX1701 Typ	LX1701 Max	Units
Supply Voltage	VDD PVDD			1.8		6.0	V
Oscillator Frequency	fSW	VDD = PVDD = 1.8~5.5V		180	200	225	KHz
Supply Current, Quiescent	IQQ	No Load	VDD = PVDD = 5V		2.0	2.5	mA
			VDD = PVDD = 3.3V		1.3	1.8	
			VDD = PVDD = 1.8V		0.9	1.2	
Supply Current, Shutdown Mode	IQQSD	Disable Pin active				1	µA
Power Supply Rejection Ratio	PSRR	VDD = PVDD = 1.8V to 5.5V			65		dB
Common Mode Rejection Ratio	CMRR	VDD = PVDD = 1.8V to 5.5V			70		dB
Input Impedance							
Input voltage Range	VIN	VDD = PVDD = 1.8~5.5V		-0.3		VDD +0.3	V
Input Resistance Differential	K_{IN}	Gain = 14dB, BW = 20Hz			65		KΩ
		Gain = 14dB, BW = 300Hz			72		
		Gain = 8dB, BW = 20Hz			98		
		Gain = 8dB, DB = 300Hz			102		
Output DC Offset	VOFF	Input shorted to GND, 20Hz corner, 14dB gain VDD = PVDD = 3.3V			2	8	mV
Input DC Offset Dynamic Range Max. with Output VOFF < 200mV	V_{INOFF}	Gain = 14dB BW = 20Hz, PVDD = 5V			0.14		V
		Gain = 14dB, BW = 300Hz, PVDD = 5V			1.50		
		Gain = 8dB, BW = 20Hz, PVDD = 5V			0.25		
		Gain = 8dB, BW = 300Hz, PVDD = 5V			2.70		
Static Drain-to-source ON-Resistance	RDSON	VDD = PVDD=5V	P Channel		360		mΩ
			N Channel		350		
		VDD = PVDD=3.3V	P Channel		490		
			N Channel		460		
		VDD = PVDD=1.8V	P Channel		600†		
			N Channel		600†		
Stage Gain	GH	Pin 9 tied to VDD, VDD = PVDD = 1.8V to 5.5V			14		dB
	GL	Pin 9 tied to VSS, VDD = PVDD = 1.8V to 5.5V			8		
Thermal Indicator Junction	T_J				150		°C
Thermal Indicator Output	VTOVL	VDD = PVDD = 1.8~5.5V			VDD	VDD +0.3	V
Under Voltage Threshold Level	VUV			1.55	1.65	1.75	V
Enable Threshold		VDD = PVDD =3.3V		1.3	1.5	1.7	V

† At +85°C ambient temperature.

Microsemi
Integrated Products Division
11861 Western Avenue, Garden Grove CA. 92841 714-898-8121, FAX 714-893-2570

SIMPLIFIED BLOCK DIAGRAM

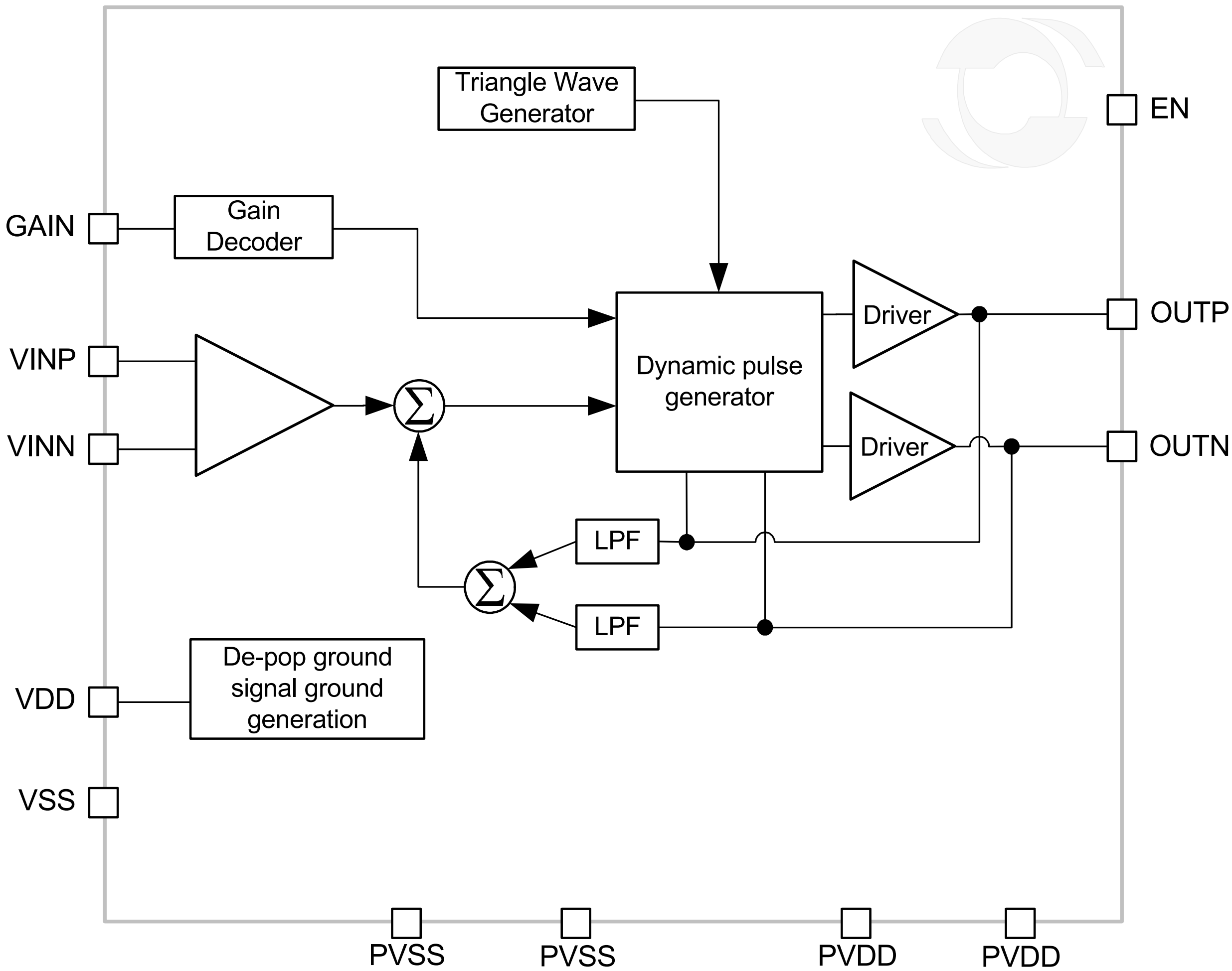


Figure 1 – LX1701 Simplified Block Diagram

TYPICAL APPLICATION SCHEMATIC

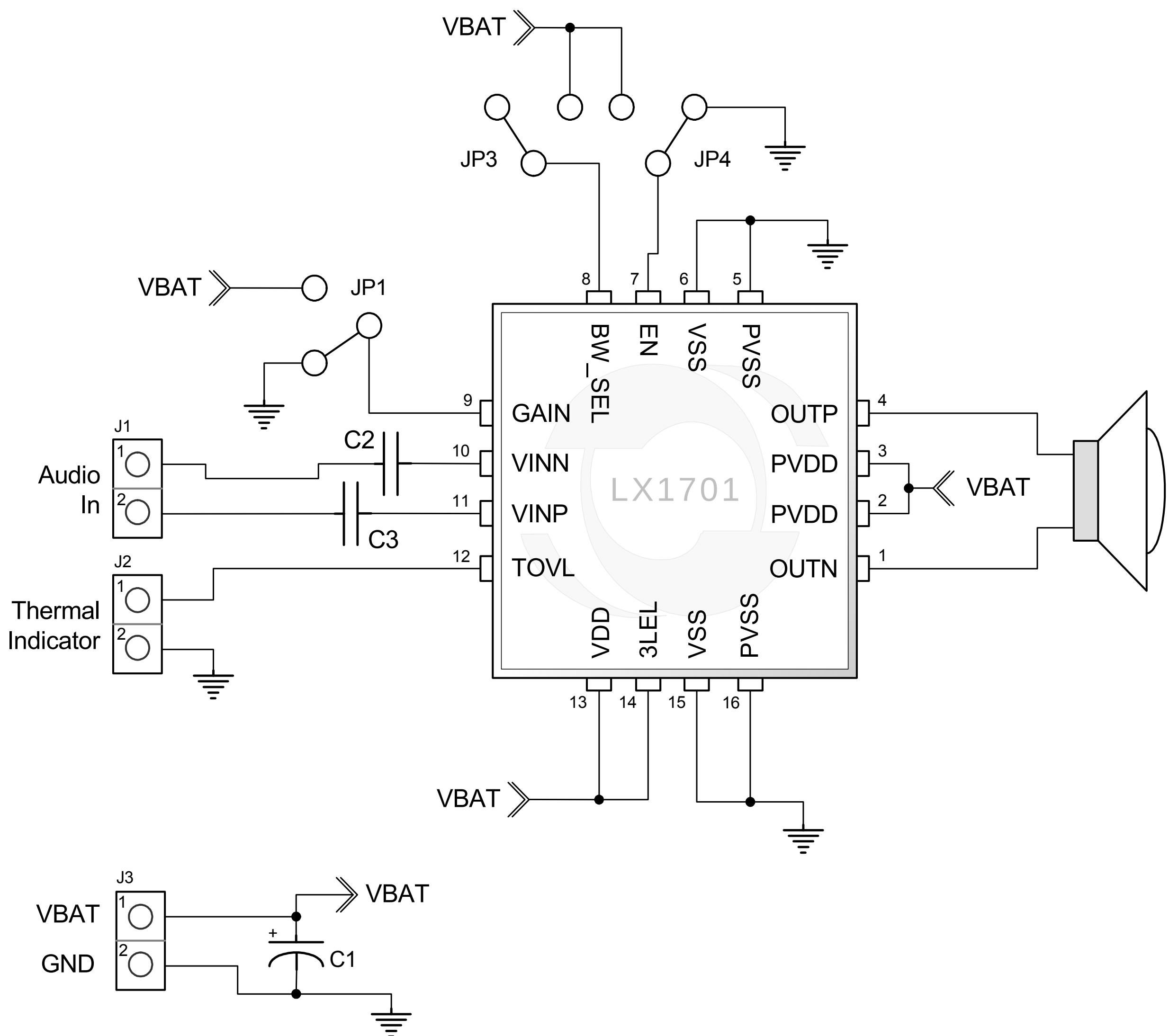


Figure 2 – LX1701 Typical Application Circuit

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

The LX1701 is a filterless, low-EMI, class-D audio power amplifier. It offers high performance (THD+N is just 0.1% at 2W), high efficiency (>85% at 1.2W), and best in class EMI radiation (just 20dBuV/m). The internal signal path is completely differential to minimize common-mode noise pickup. The inputs may be driven single-ended or differentially and they may be direct or AC coupled. The LX1701 may be operated with just a single decoupling capacitor.

FILTERLESS 3-LEVEL CLASS-D MODULATION

The LX1701 output stage is configured as a full H-bridge push-pull driver. The speaker must be driven differentially from the OUTP and OUTN pins. Each side of the speaker is driven by a 200KHz switching signal that transitions between Vdd and GND. With zero input voltage, the duty cycle at each output is around 50% and the signals are in-phase with each other. In this case, there is basically no differential voltage across the speaker. When the input signal goes positive, the duty cycle at OUTP increases above 50% and the duty cycle at OUTN decreases below 50%. This causes a net positive current to flow into the speaker. A negative input voltage causes the OUTN duty cycle to increase and the OUTP duty cycle to decrease which causes a net negative current to flow into the speaker. The differential voltage across the speaker has a fundamental frequency of twice the 200KHz switching frequency. The speaker itself serves as the low pass filter which then recreates the audio signal. This type of modulation can be described as driving +Vdd, -Vdd, and 0V across the speaker which is why it is referred to as 3-Level modulation.

Classical, 2-Level modulation drives either +Vdd or –Vdd across the speaker at all times. This scheme requires an L-C filter between the amplifier's outputs and the speaker in order to keep the output current low.

LOW-EMI OUTPUT STAGE WITH SLEW RATE LIMITING AND ACTIVE OVERSHOOT CLAMPING

With 3-Level modulation, the carrier frequency drives a full amplitude common-mode signal to the speaker wires. This can cause high EMI radiation. One way to combat this would be to filter the outputs with L-C filters or ferrite beads located close to the amplifier. In the LX1701, the output stage has been carefully designed to minimize EMI radiation so that these types of filters are not required. Slew rate limiting is used to keep the outputs from switching too quickly. Active overshoot clamping is used to minimize the inductive overshoot which occurs at each transition. These two techniques allow the LX1701 to easily meet FCC standards for radiated emissions when driving up to 3 meters of speaker wire.

ACTIVE DC INPUT OFFSET CANCELLATION

An internal DC servo loop senses the output differential voltage and feeds it back to the error amplifier through a low pass filter. The corner frequency of this filter can be set at 20Hz or 300Hz via a control pin. This allows the LX1701 to reject signals below these frequencies. Since this is an active control loop, it does not have the same dynamic range as a purely passive solution (such as an input AC-coupling capacitor). The dynamic range of the offset cancellation loop is a function of the selected gain and high pass corner frequency. In applications where the input offset may be higher than the DC offset cancellation range, AC-coupling capacitors should be used.

DIFFERENTIAL SIGNAL PATH, WIDE DYNAMIC RANGE, AND BUILT-IN THERMAL OVERLOAD PROTECTION

The fully differential signal path uses delta-sigma techniques and multiple feedback loops to provide high performance and low distortion. This is all fully-integrated to eliminate the need for any external feedback components or filters. The gain can be selected to be either 8 or 14dB by a control pin. The differential signal path and internal voltage boosters allow for wide dynamic range. In fact, the LX1701 can be operated from supplies as low as 1.8V and as high as 6V. The output power will be limited by the available supply voltage. An internal thermal sensing circuit shuts down the outputs and forces the TOVL output pin high when the junction temperature exceeds about 150degC to provide thermal overload protection.

EVALUATION MODULE TEST SET-UP

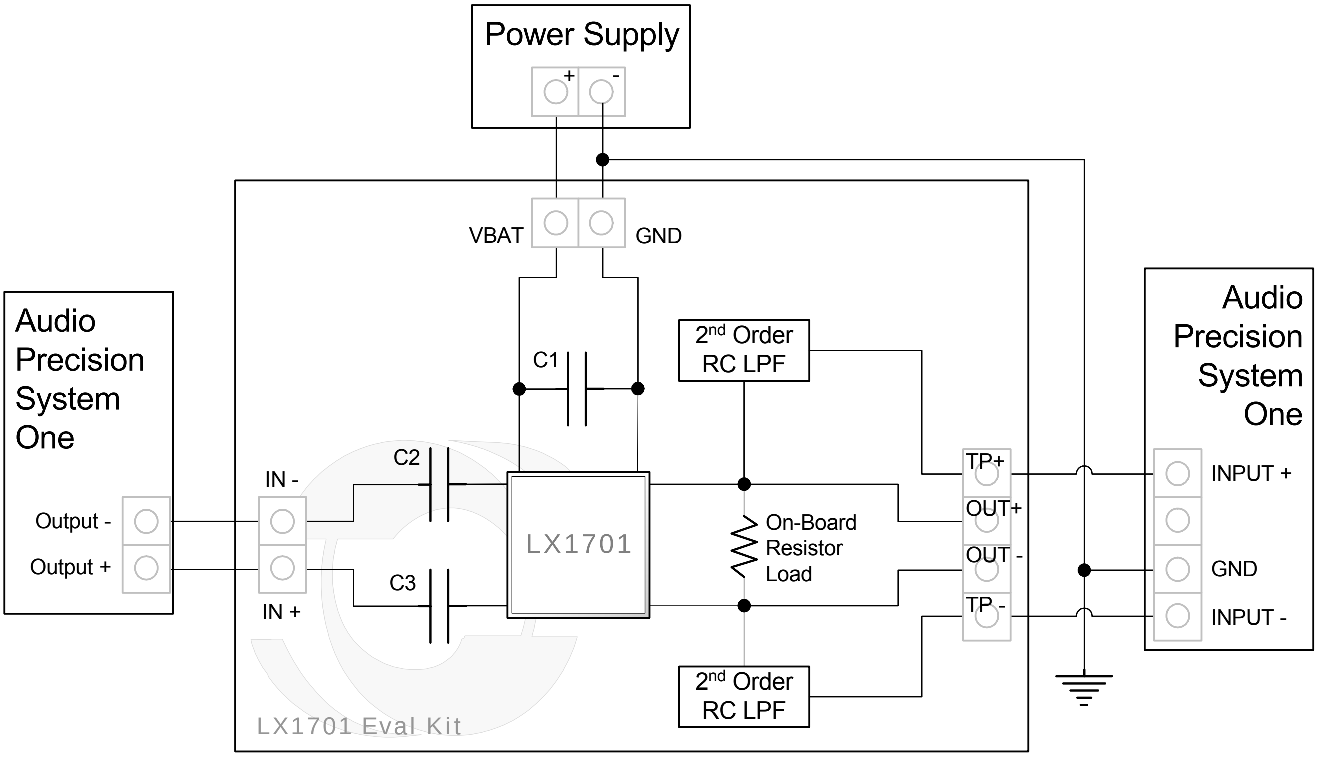


Figure 3 – Typical Test Setup Circuit

Default Settings:

Equipments: Audio Precision SYSTEM 1,
Oscilloscope,
Power Supply ~+5V;

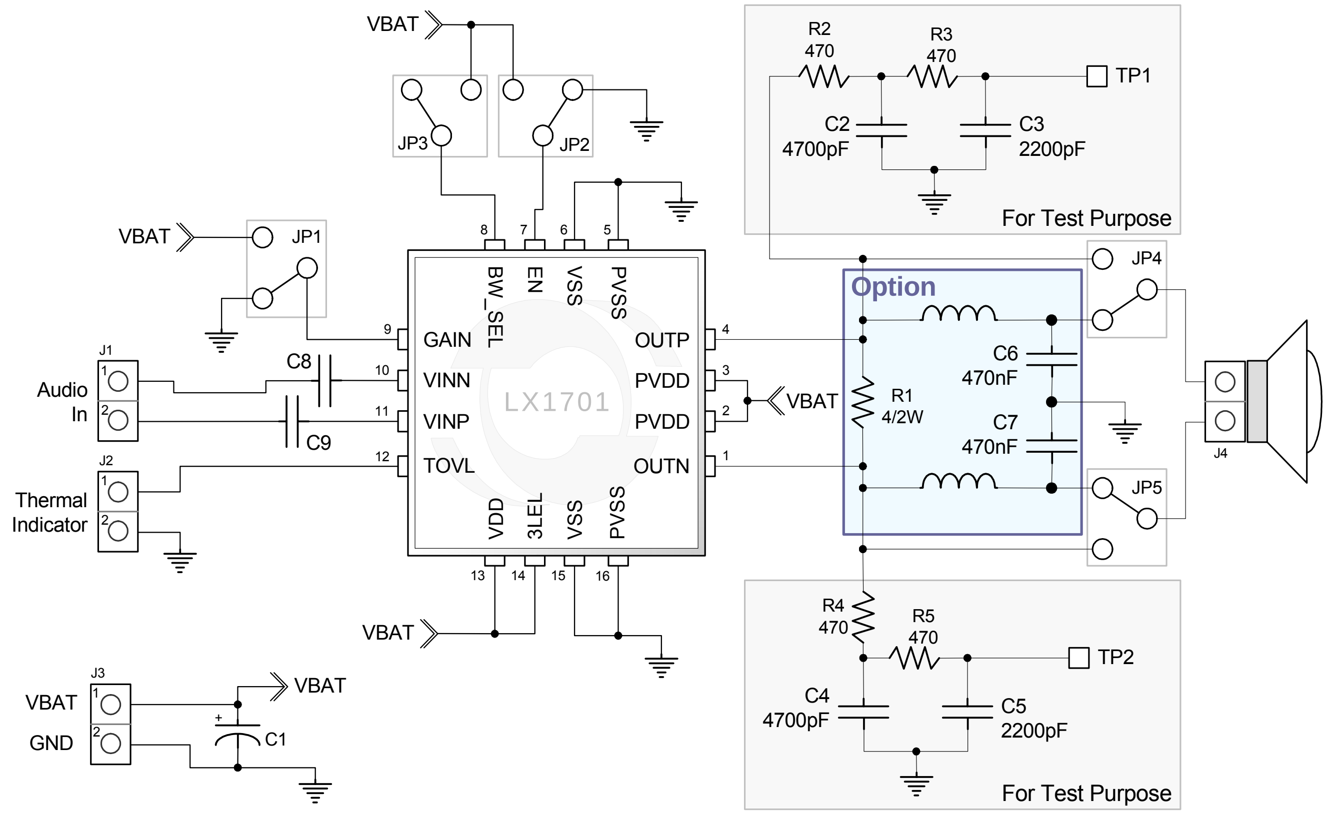
Supply Voltage: 1.8V/3.3V/5.0V 3 corner voltages

On-Board passive LPF: 40KHz cut off frequency (-3dB)

On-Board resistor load: 2/4/8 Ω, 5W

AP settings: 10Hz ~ 22KHz BPF

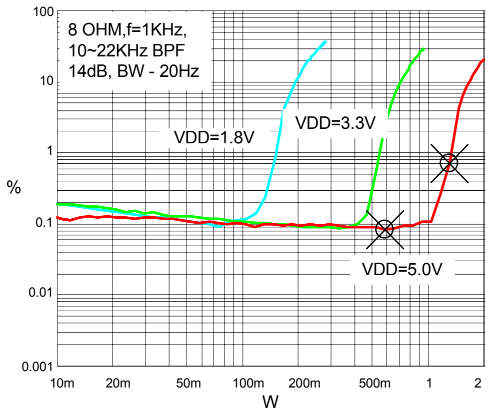
APPLICATION INFORMATION



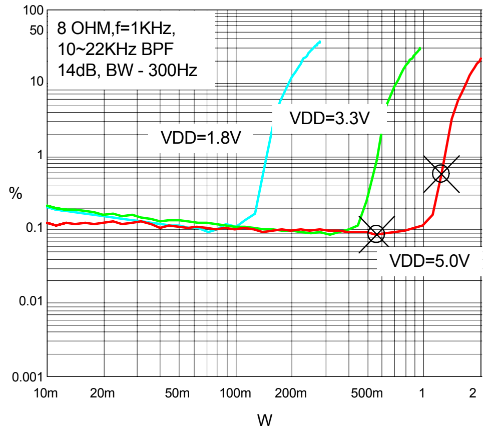
*C1 Value is dependant on the current drain from power supply, 1.0 ~ 33μF with output power 350mW ~ 3.5W

Figure 4 – LXE1701 Evaluation Module Schematic

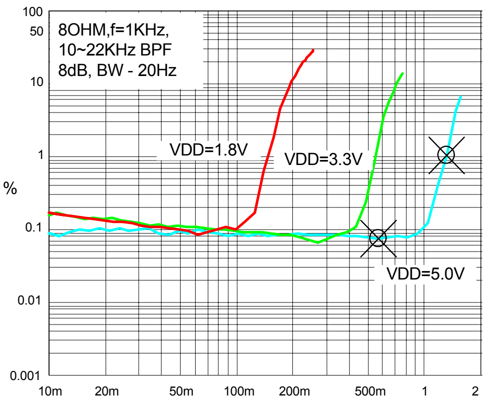
THD+N vs. Power



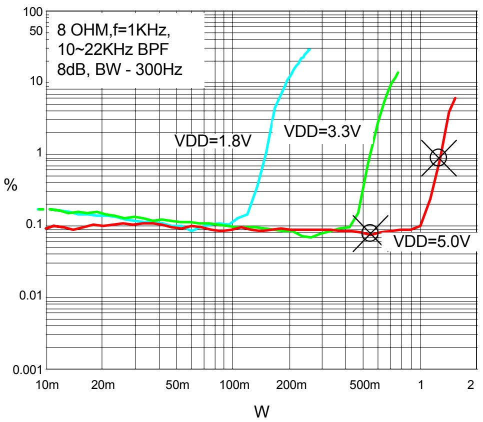
THD+N vs. Power



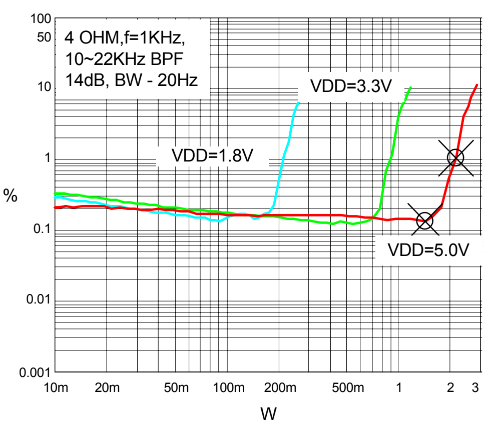
THD+N vs. Power



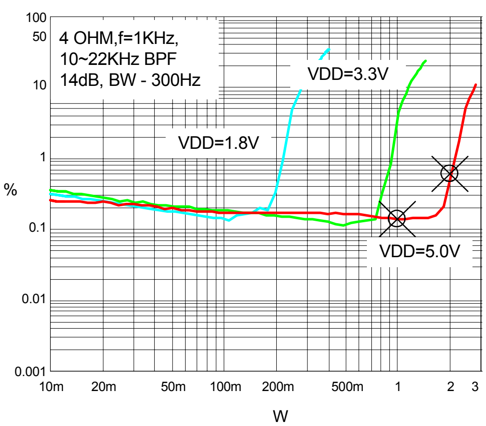
THD+N vs. Power

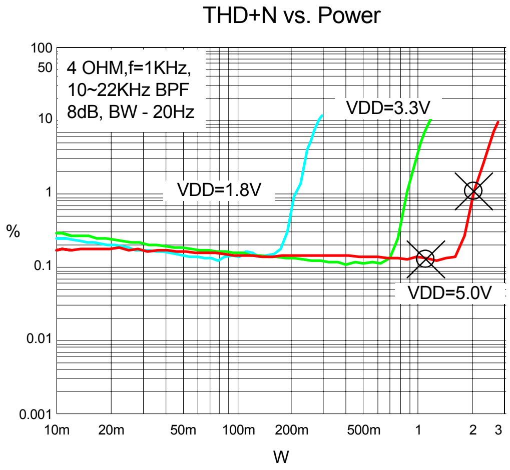


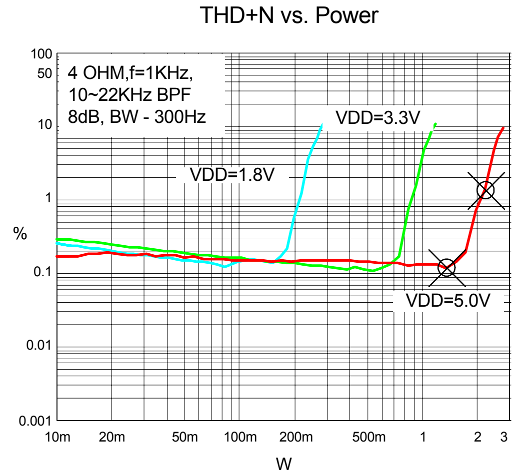
THD+N vs. Power

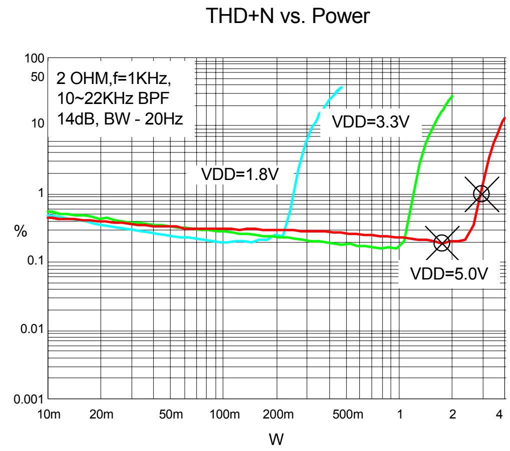


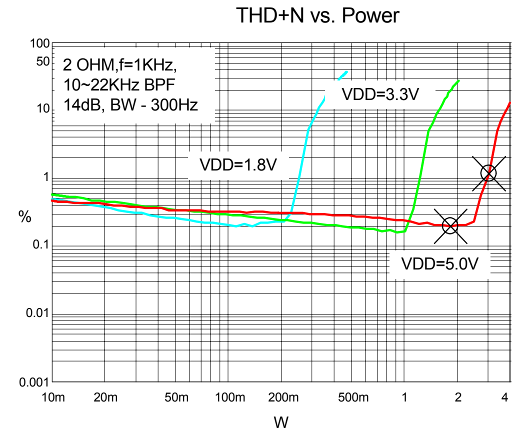
THD+N vs. Power

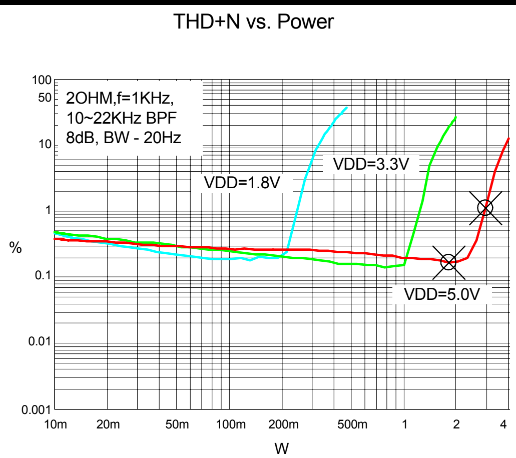


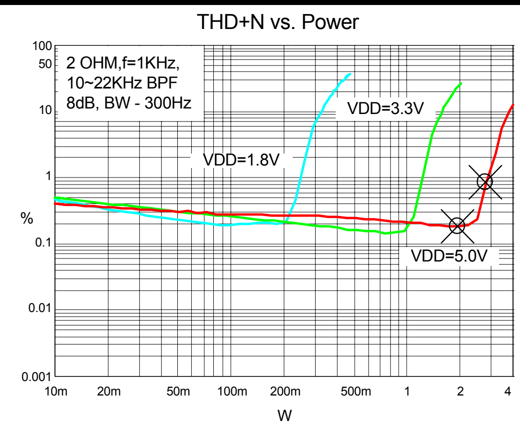

THD+N vs. Power
4 OHM,f=1KHz,
10~22KHz BPF
8dB, BW - 20Hz
VDD=1.8V
VDD=3.3V
VDD=5.0V
%
W

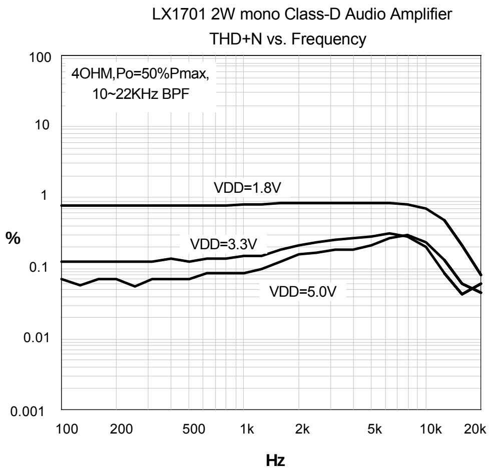

THD+N vs. Power
4 OHM,f=1KHz,
10~22KHz BPF
8dB, BW - 300Hz
VDD=1.8V
VDD=3.3V
VDD=5.0V
%
W

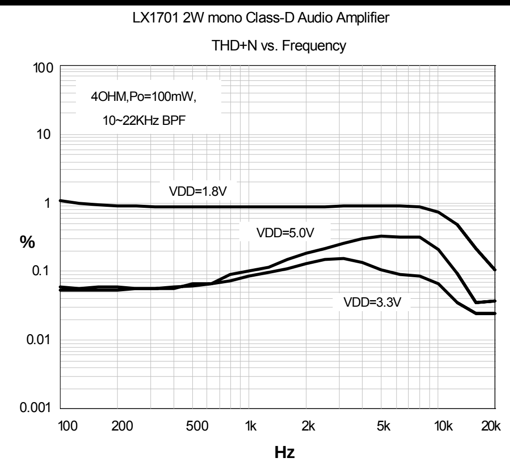

THD+N vs. Power
2 OHM,f=1KHz,
10~22KHz BPF
14dB, BW - 20Hz
VDD=1.8V
VDD=3.3V
VDD=5.0V
%
W

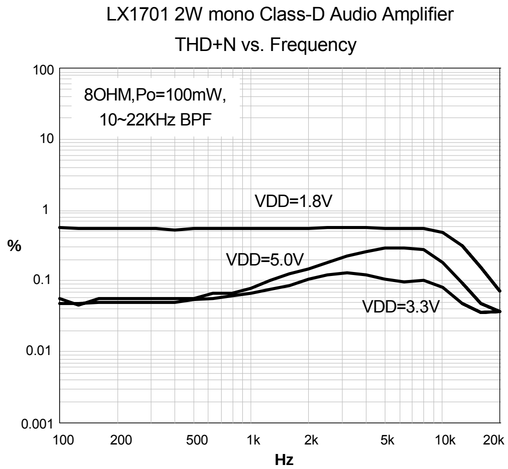

THD+N vs. Power
2 OHM,f=1KHz,
10~22KHz BPF
14dB, BW - 300Hz
VDD=1.8V
VDD=3.3V
VDD=5.0V
%
W

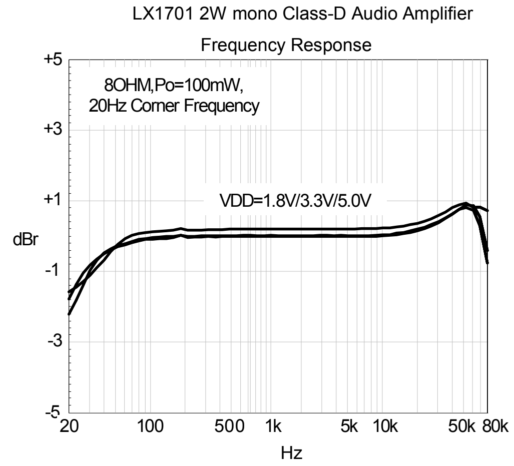

THD+N vs. Power
2OHM,f=1KHz,
10~22KHz BPF
8dB, BW - 20Hz
VDD=1.8V
VDD=3.3V
VDD=5.0V
%
W

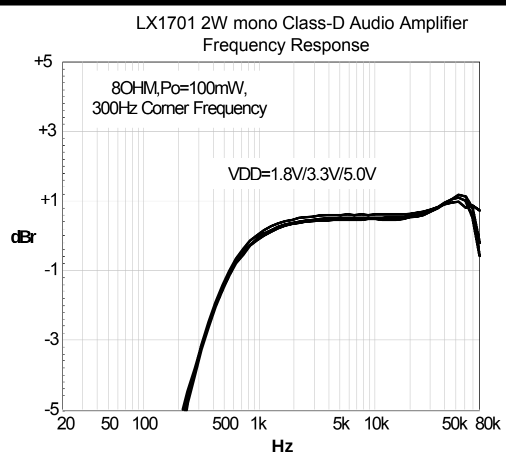

THD+N vs. Power
2 OHM,f=1KHz,
10~22KHz BPF
8dB, BW - 300Hz
VDD=1.8V
VDD=3.3V
VDD=5.0V
%
W

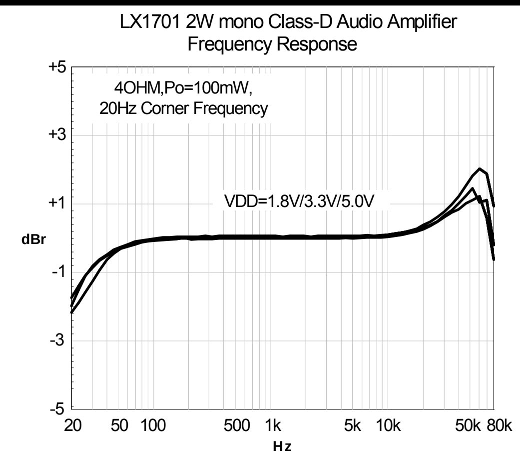

LX1701 2W mono Class-D Audio Amplifier
THD+N vs. Frequency
4OHM,Po=50%Pmax,
10~22KHz BPF
VDD=1.8V
VDD=3.3V
VDD=5.0V
%
Hz


LX1701 2W mono Class-D Audio Amplifier
THD+N vs. Frequency
4OHM,Po=100mW,
10~22KHz BPF
VDD=1.8V
VDD=5.0V
VDD=3.3V
%
Hz

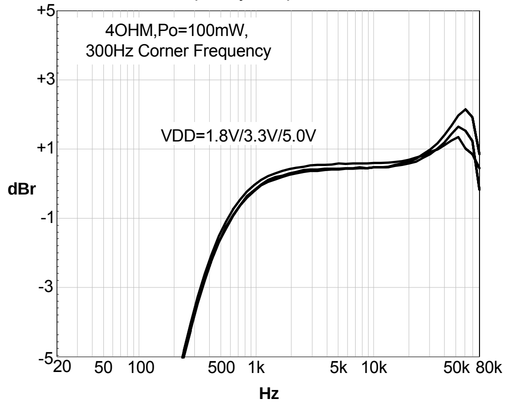

LX1701 2W mono Class-D Audio Amplifier
THD+N vs. Frequency
8OHM,Po=100mW,
10~22KHz BPF
VDD=1.8V
VDD=5.0V
VDD=3.3V
%
Hz


LX1701 2W mono Class-D Audio Amplifier
Frequency Response
8OHM,Po=100mW,
20Hz Corner Frequency
VDD=1.8V/3.3V/5.0V
dBr
Hz

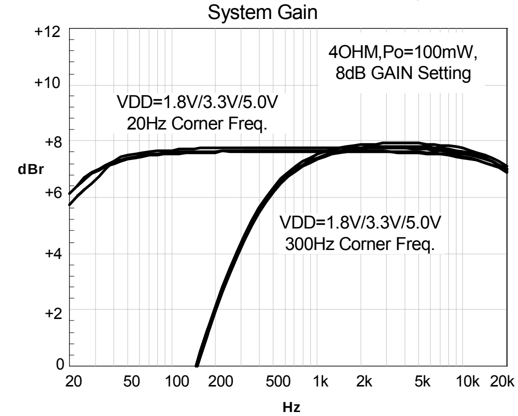

LX1701 2W mono Class-D Audio Amplifier
Frequency Response
8OHM,Po=100mW,
300Hz Corner Frequency
VDD=1.8V/3.3V/5.0V
dBr
Hz


LX1701 2W mono Class-D Audio Amplifier
Frequency Response
4OHM,Po=100mW,
20Hz Corner Frequency
VDD=1.8V/3.3V/5.0V
dBr
Hz

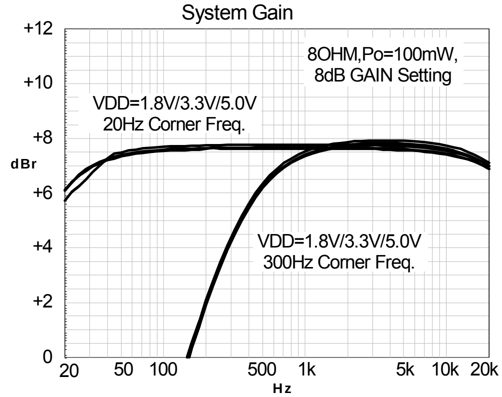
LX1701 2W mono Class-D Audio Amplifier
Frequency Response



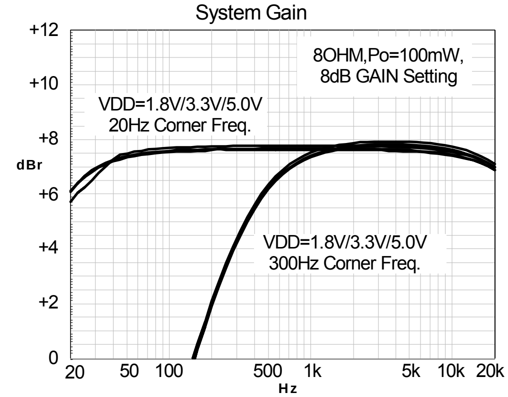
LX1701 2W mono Class-D Audio Amplifier
System Gain



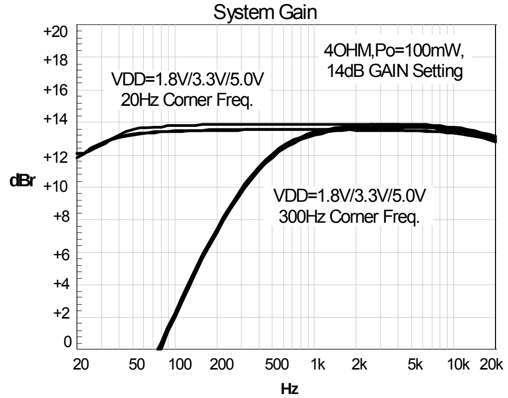
LX1701 2W mono Class-D Audio Amplifier
System Gain



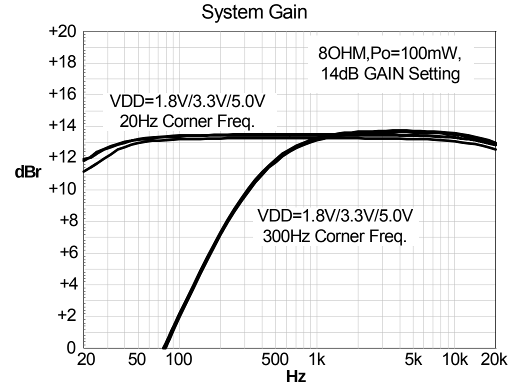
LX1701 2W mono Class-D Audio Amplifier
System Gain



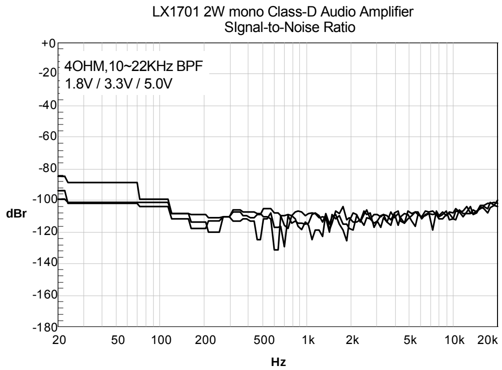
LX1701 2W mono Class-D Audio Amplifier
System Gain



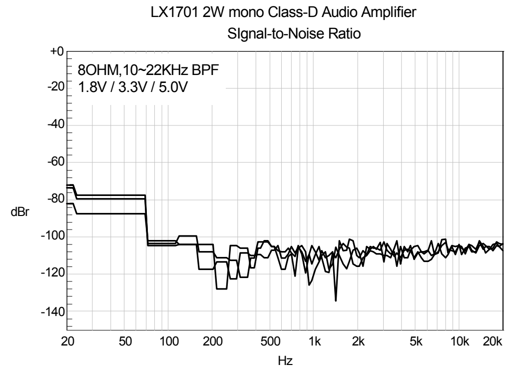
LX1701 2W mono Class-D Audio Amplifier
System Gain



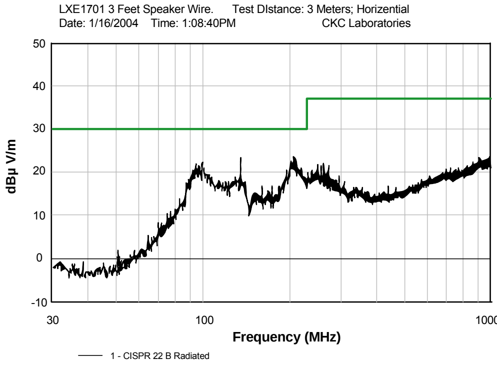
Microsemi
Integrated Products Division
11861 Western Avenue, Garden Grove CA. 92841 714-898-8121, FAX 714-893-2570



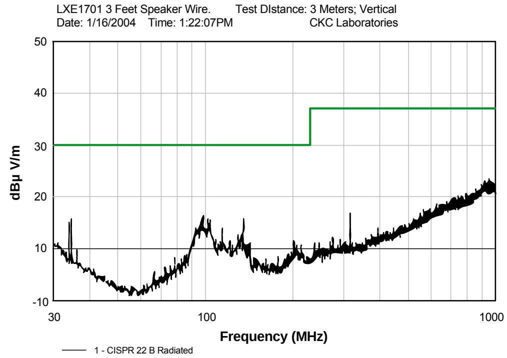
LX1701 2W mono Class-D Audio Amplifier
SIgnal-to-Noise Ratio
4OHM,10~22KHz BPF
1.8V / 3.3V / 5.0V
dBr
Hz



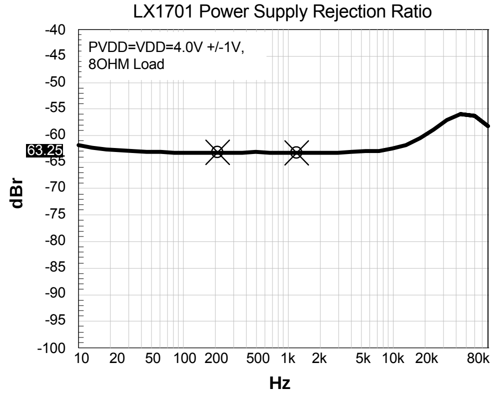
LX1701 2W mono Class-D Audio Amplifier
SIgnal-to-Noise Ratio
8OHM,10~22KHz BPF
1.8V / 3.3V / 5.0V
dBr
Hz

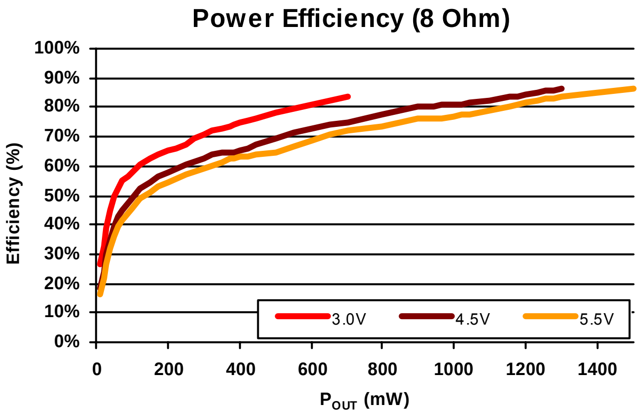


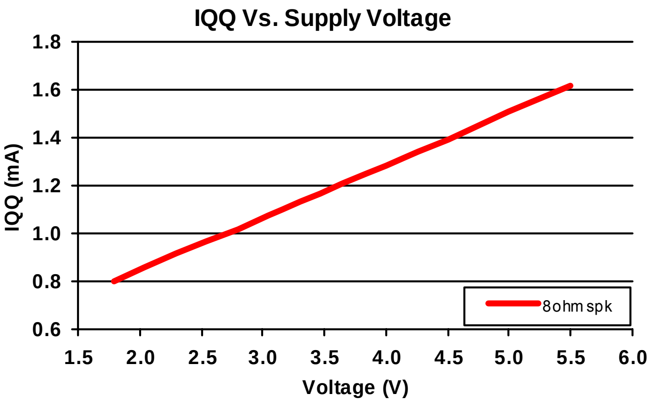
LXE1701 3 Feet Speaker Wire. Test DIstance: 3 Meters; Horizential
Date: 1/16/2004 Time: 1:08:40PM CKC Laboratories
dBμ V/m
Frequency (MHz)
1 - CISPR 22 B Radiated



LXE1701 3 Feet Speaker Wire. Test DIstance: 3 Meters; Vertical
Date: 1/16/2004 Time: 1:22:07PM CKC Laboratories
dBμ V/m
Frequency (MHz)
1 - CISPR 22 B Radiated


LX1701 Power Supply Rejection Ratio
PVDD=VDD=4.0V +/-1V,
8OHM Load
dBr
Hz
-40
-45
-50
-55
-60
63.25
-65
-70
-75
-80
-85
-90
-95
-100
10
20
50
100
200
500
1k
2k
5k
10k
20k
80k


Power Efficiency (8 Ohm)
Efficiency (%)
POUT (mW)
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
0
200
400
600
800
1000
1200
1400
3.0V
4.5V
5.5V


IQQ Vs. Supply Voltage
IQQ (mA)
Voltage (V)
1.8
1.6
1.4
1.2
1.0
0.8
0.6
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
8ohm spk

PCB DESIGN GUIDELINES

PCB DESIGN GUIDELINES

One of the key efforts in implementing the MLP package on a pc board is the design of the land pattern. The MLP has rectangular metallized terminals exposed on the bottom surface of the package body. Electrical and mechanical connection between the component and the pc board is made by screen printing solder paste on the pc board and reflowing the paste after placement. To guarantee reliable solder joints it is essential to design the land pattern to the MLP terminal pattern, exposed PAD and Thermal PAD via. There are two basic designs for PCB land pads for the MLP: Copper Defined style (also known as Non Solder Mask Defined (NSMD)) and the Solder Mask Defined style (SMD). The industry has had some debate of the merits of both styles of land pads, and although we recommend the Copper Defined style land pad (NSMD), both styles are acceptable for use with the MLP package. NSMD pads are recommended over SMD pads due to the tighter tolerance on copper etching than solder masking. NSDM by definition also provides a larger copper pad area and allows the solder to anchor to the edges of the copper pads thus providing improved solder joint reliability.

DESIGN OF PCB LAND PATTERN FOR PACKAGE TERMINALS

As a general rule, the PCB lead finger pad (Y) should be designed 0.2-0.5mm longer than the package terminal length for good filleting. The pad length should extended 0.05mm towards the centerline of the package. The pad width (X) should be a minimum 0.05mm wider than the package terminal width (0.025mm per side), refer to figure 5. However, the pad width is reduced to the width of the component terminal for lead pitches below 0.65mm. This is done to minimize the risk of solder bridging.

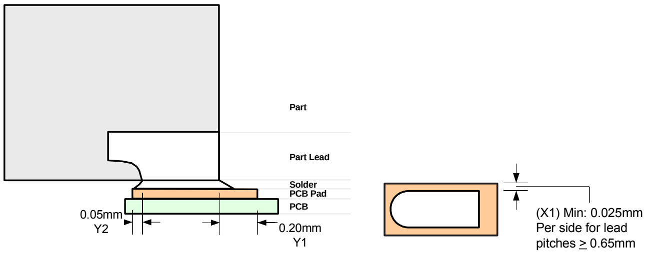


Figure 5 – PC Board Land Pattern Geometry for MLP Terminals

EXPOSED PAD PCB DESIGN

The construction of the Exposed Pad MLP enables enhanced thermal and electrical characteristics. In order to take full advantage of this feature the exposed pad must be physically connected to the PCB substrate with solder.

The thermal pad (D2th) should be greater than D2 of the MLP whenever possible, however adequate clearance (Cpl > 0.15mm) must be met to prevent solder bridging. If this clearance cannot be met, then D2th should be reduced in area. The formula would be: D2TH >D2 only if D2TH < Gmin - (2 x Cpl).

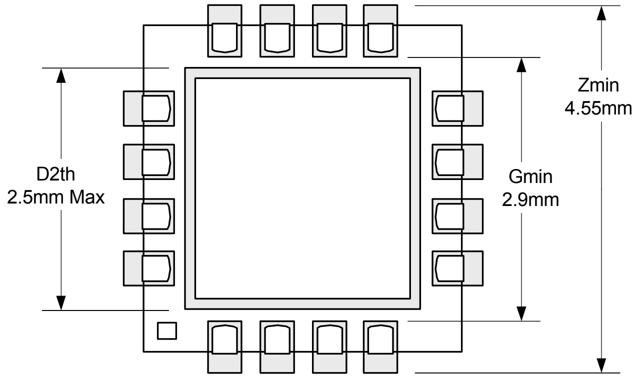


Figure 6 – Land Pattern for LQ16 (4x4mm)

Zmin= D + aaa + 2(0.2)
(where pkg body tolerance aaa=0.15)
(where 0.2 is outer pad extension)
Gmin= D-2(Lmax)-2(0.05)
(where 0.05 is inner pad extension)
(Lmax=0.50 for this example)
D2th max = Gmin-2(CpL)
(where CpL=0.2)

PCB DESIGN GUIDELINES (CONTINUED)

THERMAL PAD VIA DESIGN

There are two types of on-board thermal PAD design, one is using thermal vias to sink the heat to the other layer with metal traces. Based on Jedec Specification JESD 51-5, the thermal vias should be designed like Figure 7. Another one is the no via thermal PAD which is using the same side copper PAD as heatsink, this type of thermal PAD is good for two layer board, since the bottom side is filled with all other kinds of trace also, it's hard to use the whole plane for the heatsink. But you still can use vias to sink the heat to the bottom layer by the metal traces, then layout a NMSD on which a metal heatsink is put to sink the heat to the air.

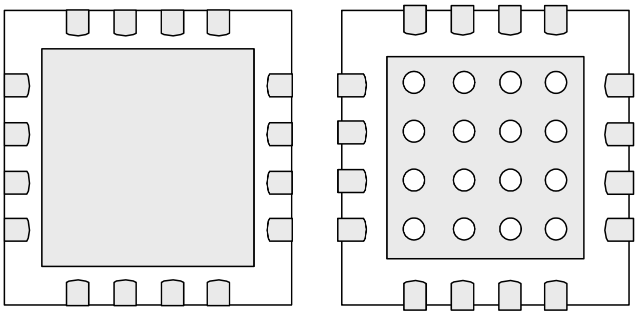


Figure 7 – Comparison of land pattern theory

For LX1701 with MLPQ-4x4 16Lds p ackage, which has θjA =38.1°C/W by package itself, with maximum 2W (@4ohm) output it only has 300mW power dispassion (assuming 85% efficiency), which only has 11.4°C temperature rise. So the non-via type thermal PAD is suggested.

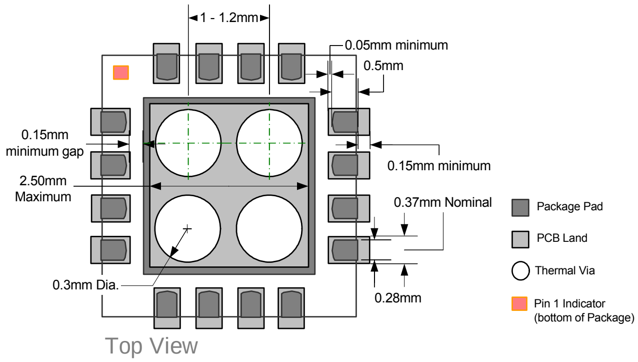


Figure 8 – Recommended Land Pad with Vias for LQ16

APPLICATION INFORMATION

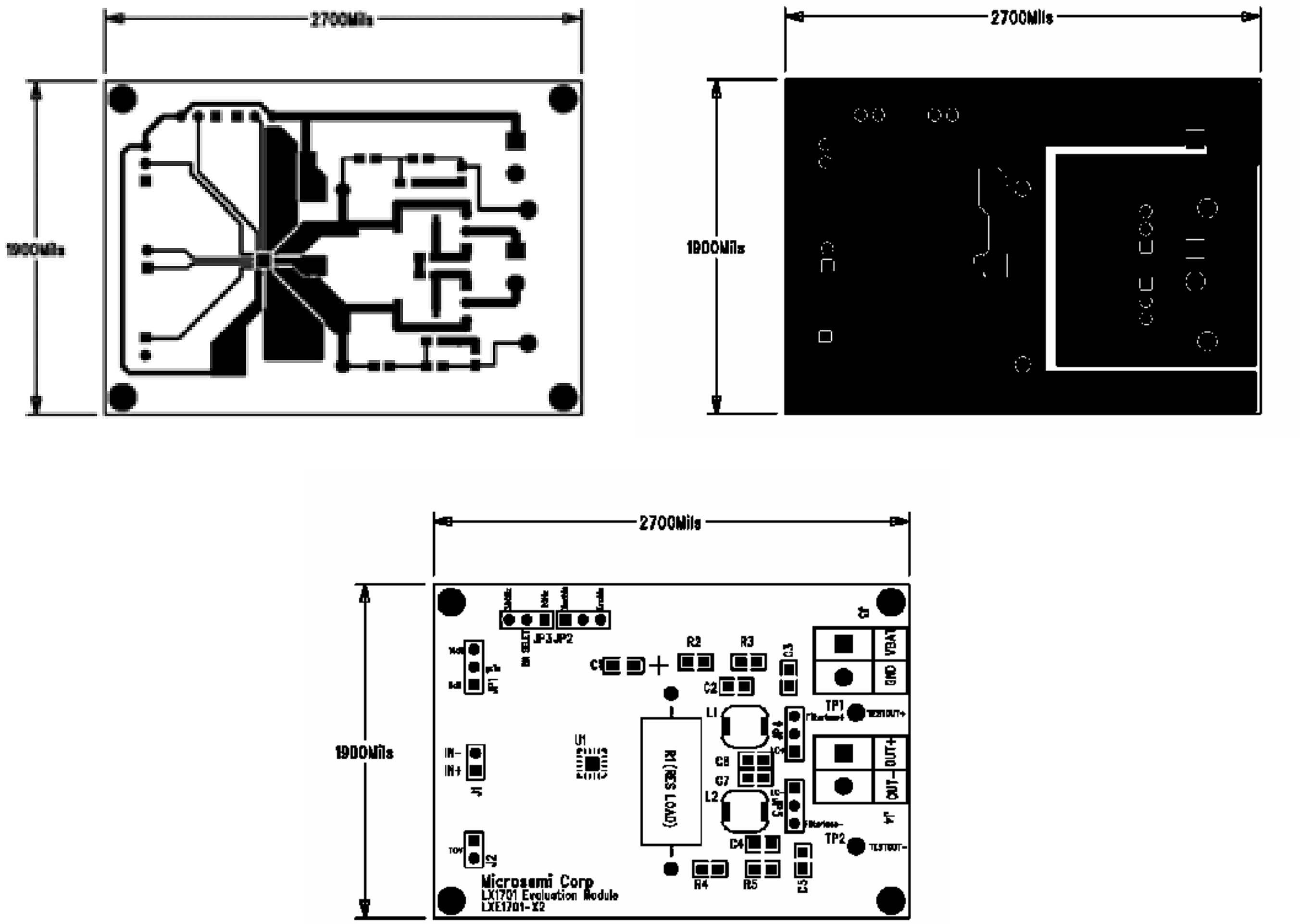


Figure 9 – LXE1701 Evaluation Module PCB Layout

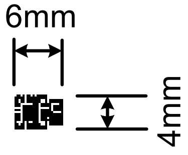
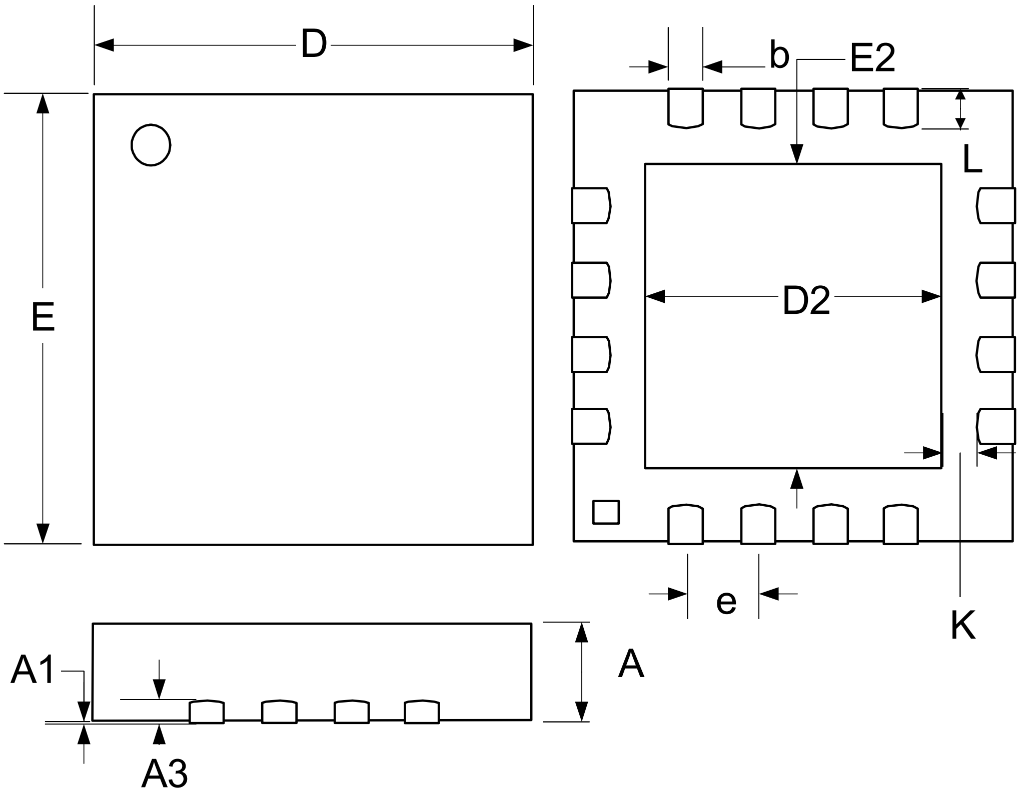


Figure 10 – LX1701 real PCB area with decoupling capacitor

PACKAGE DIMENSIONS

LQ 16-Pin MLPQ Plastic (4x4mm EP / 114x114Cu Exposed Pad)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.2 REF		0.008 REF	
b	0.23	0.38	0.009	0.015
D	4.00 BSC		0.157 BSC	
E	4.00 BSC		0.157 BSC	
e	0.65 BSC		0.026 BSC	
D2	2.55	2.80	0.100	0.110
E2	2.55	2.80	0.100	0.110
K	0.20	-	0.008	-
L	0.30	0.50	0.012	0.020

Note:
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006”) on any side. Lead dimension shall not include solder coverage.

NOTES

Microsemi
Integrated Products Division
11861 Western Avenue, Garden Grove CA. 92841 714-898-8121, FAX 714-893-2570