1.0MHz Inverting DC/DC Converter

DESCRIPTION

The LX1734 is an inverting DC/DC current-mode controller. With a 750mA integrated switch, the LX1734 can generate large output currents in a small footprint. The LX1734 minimizes external component size and cost by implementing a high switching frequency of 1.0MHz, while generating -5V at 250mA.

When configured in the dual inductor inverting topology very low output voltage ripple approaching $1mV_{P-P}$ can be achieved when used in conjunction with ceramic output capacitors. The dual inductor can be implemented as a coupled or separate cores.

Fixed frequency operation ensures a clean output free from low frequency noise typically present with charge pump solutions. The low impedance output remains within 1% of nominal during large load steps. The 18V switch allows high voltage outputs to be generated.

The LX1734 is available in the space saving 6-lead 3x3 Jedec MO-229 package, which has the same footprint and lead spacing as the SOT-23A. A complete inverter function utilizes less than 0.3^2 inches of PCB space.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

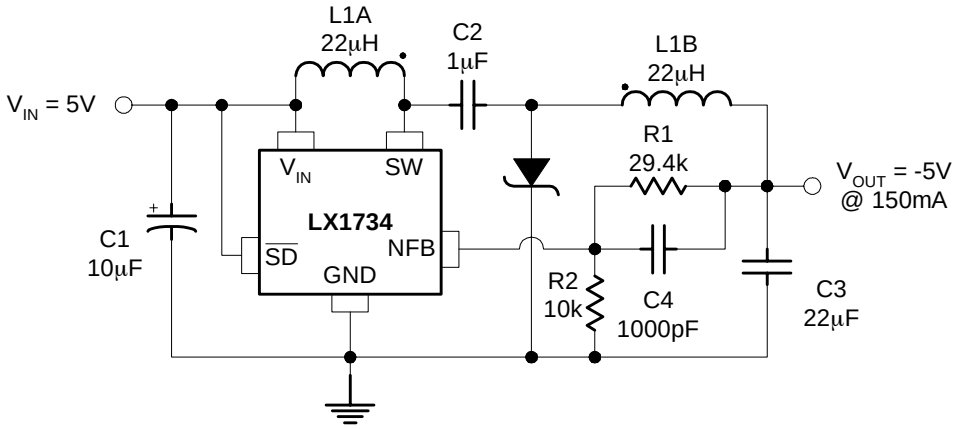
KEY FEATURES

- Fixed Frequency 1.0MHz Operation
- Very Low Noise: $1mV_{P-P}$ Output Ripple Possible With Cuk Topology
- Stable Operation With Ceramic or Tantalum Capacitors
- -5V at 250mA from 5V Input
- Uses Small Surface Mount L/C Components
- Wide Input Range: 4.2V to 8V
- Low VCESAT Switch: 600mV at 600mA
- 6-Lead 3x3mm JEDEC MLPM Package
- Functionally Compatible with LT1611 or LT1931

APPLICATIONS/BENEFITS

- Disk Drive MR Head Bias
- Digital Camera CCD Bias
- LCD Bias
- GaAs FET Bias
- Local -5V or -12V Supplies

PRODUCT HIGHLIGHT



Note: L1A and L1B are shown as coupled. Individual inductors can also be used.
C1, C2, C3 are ceramic capacitors

Figure 1

PACKAGE ORDER INFO

T_A (°C)	LM Plastic MLPL 6-Pin RoHS Compliant / Pb-free Transition DC: 0452
0 to 85	LX1734CLM

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1734CLM-TR)

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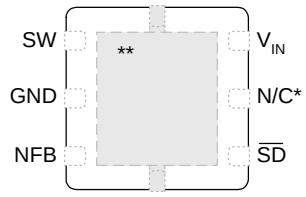
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}), Shutdown ($\overline{SD}$) ..... 0 to 10V
SW Voltage ..... -0.4V to 20V
NFB Voltage ..... -2V
Current Into NFB Pin ..... ±1mA
Operating Temperature Range ..... 0°C to 85°C
Maximum Junction Temperature ..... 125°C
Storage Temperature ..... -65°C to 150°C
Peak Package Solder Reflow Temperature
(40 second maximum exposure) ..... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



LM PACKAGE
(Top View)

* Not Internally Connected.
** Package heatsink should be connected to ground or left floating.

RoHS / Pb-free 100% Matte Tin Lead Finish

THERMAL DATA

LM **Plastic LM 6-Pin**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JC}	8°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JC})$.
The θ_{JC} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

FUNCTIONAL PIN DESCRIPTION

NAME	DESCRIPTION
SW	Power Switch Pin
GND	Common ground reference
NFB	Feedback Pin - Connect to a resistive divider in order to set the output voltage. Feedback threshold is -1.235V. Given the typical NFB bias current (I_{NFB}) of 4µA flows out of the pin, the suggested value for R2 is 10K. Given R_2, set R_1 according to: $$R_1 = \frac{\left|VOUT\right| - 1.235}{\frac{1.235}{R_2} + \left(I_{NFB}\right)}$$
V_{IN}	Input Supply – Input pin must be locally bypassed.
$\overline{SD}$	Shutdown, Connected to >2V, device is active.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 85°C and the following test conditions: V_{IN} = 5V

Parameter		Symbol	Test Conditions	LX1734 Min	LX1734 Typ	LX1734 Max	Units
Minimum Operating Voltage		V_{IN}				4.25	V
V_{IN} Under Voltage Lockout		UVLO	V_{IN} rising, regulator remains off	3.2		4.25	V
Reference Voltage		V_{NFB}		-1.205	-1.235	-1.255	V
Reference Voltage Line Regulation			4.5V ≤ V_{IN} ≤ 5.5V, T_{AMB} ≥ 25°C			18	mV
NFB Pin Bias Current		I_{NFB}			-4	-8	µA
Quiescent Current		I_Q	(Regulator Not Switching, V_{NFB} = -2V)		9	12	mA
Quiescent Current		I_{SHDN}	$V_{\overline{SD}}$ ≤ 0.28V			300	µA
Switching Frequency			I_{OUT} = 5mA to 250mA	0.8		1.4	MHz
Maximum Duty Cycle				82			%
Switch V_{CESAT}			I_{SW} = 600mA		650	800	mV
Switch Leakage Current			V_{SW} = 10V		0.02	1	µA
Switch Circuit Current Limit			Duty Cycle < 50%	700			mA
Shutdown Input Voltage	High	V_{SDH}	Device Active	2			V
	Low	V_{SDL}	Device Disabled			0.8	V
	Bias Current	I_{SD}	$V_{\overline{SD}}$ = 0.28V	-5	0.4	1.0	µA
			$V_{\overline{SD}}$ = 5V		30	50	µA

BLOCK DIAGRAM

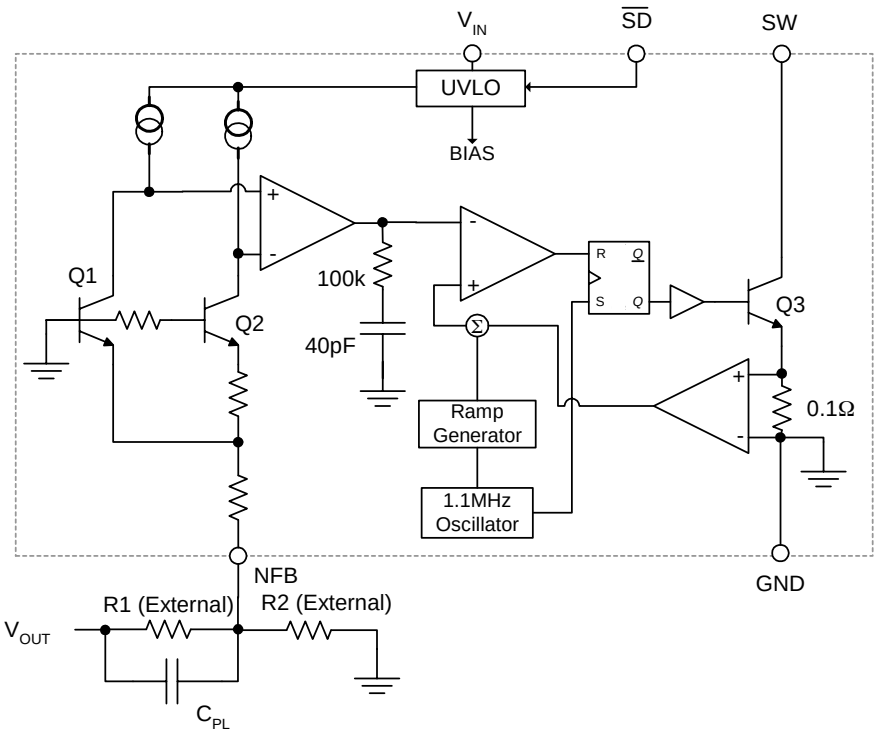

Figure 2 – Simplified Block Diagram

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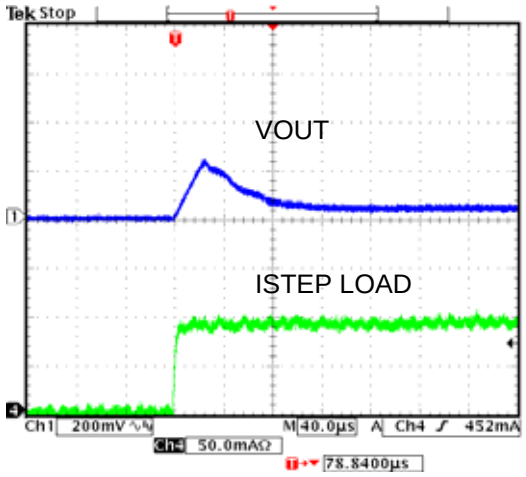
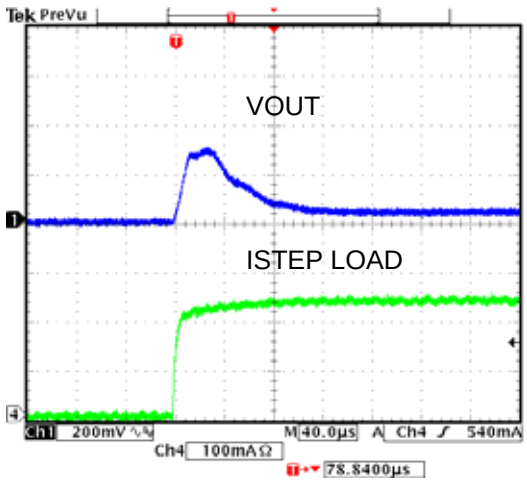
CONDITIONS: V_{IN} @ 5V, V_{OUT} @ -5V, C_{IN}=C_{OUT}=10uF Ceramic, L1=L2=10uH

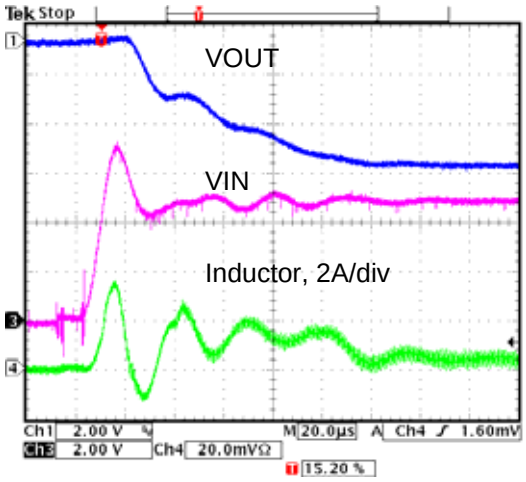
STEP LOAD RESPONSE 0 – 100mA



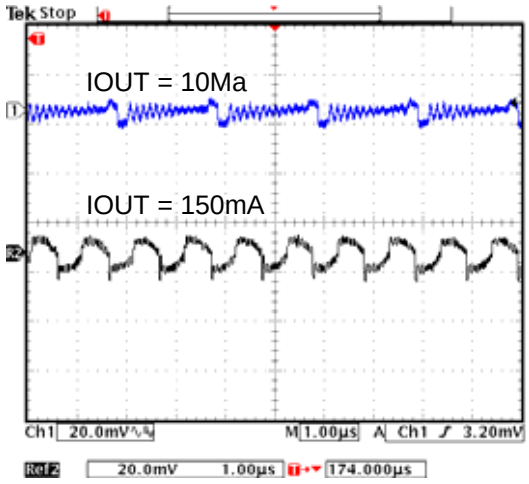
STEP LOAD RESPONSE 0 – 250mA



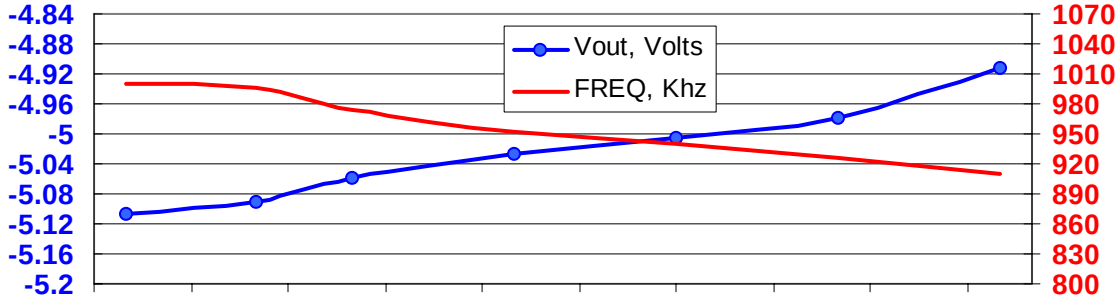
POWER ON RESPONSE, IOUT @ 200mA



OUTPUT VOLTAGE RIPPLE, IOUT @ 10mA and 150 mA



LX1734 TEMPERATURE STABILITY
IL = 132mA



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THEORY OF OPERATION

The LX1734 is a fixed frequency current mode controller designed to develop a negative output voltage from a positive input voltage. The switching transistor and current sense resistor are integrated into the part. The PWM functions in a peak current regulation mode using the amplified error signal to determine the peak switch current each cycle. Slope compensation is added to provide stable operation at high duty cycles. A current limit detector overrides the regulation loop and prevents the switch current from exceeding the over current threshold level.

The bandgap control circuit keeps Q1 biased on and produces a reference current (I_{REF}) that produces a voltage drop across the internal resistance that has a positive temperature coefficient.

When this resistor voltage drop is added to the negative temperature coefficient of the base-emitter voltage drop of Q1, the result is a temperature compensated reference voltage (V_{REF}) at the NFB pin. The summing node from the external feedback network is connected directly to NFB pin, which is relatively high impedance (typically 150k). The feedback loop minimizes the error current, (I_{ERROR}) which effectively regulates the voltage at the NFB pin. As with a conventional error amplifier, the error signal is proportional to the difference between the temperature compensated reference voltage (V_{REF}) and the summing node voltage. A slight correction factor is necessary to account for the added summing node voltage due to the reference current (I_{REF}, typically 4µADC) flowing through the Thevenin equivalent summing node external resistance.

APPLICATION NOTE

The LX1734 can be used in several topologies that generate a negative output voltage from a positive input voltage. The LX1734 can be used in a dual inductor converter with coupled or uncoupled inductors (see Figure 1); this topology is required if the absolute value of the output voltage is less than or equal to the input voltage but can also be used for higher voltage outputs. The following components or their equivalents can be used to implement the converter in Figure 1, which produces a –5V output at 150mA from a +5V input. The reference design has an efficiency of greater than 72% and an input ripple voltage of less than 6mV_{P-P} and an output ripple voltage of less than 300µV_{P-P}.

Ref	Description	Part Number	Manufacturer
C1	Ceramic, 4.7uF, 6.3V (0805)	JMK212BJ475MG	Taiyo Yuden
C2	Ceramic, 1uF, 16V (0805)	GRM40X7R105M16	Murata
C3	Ceramic, 22uF, 6.3V (1210)	JMK325BJ226MM	Taiyo Yuden
C4	Ceramic, 470pF, 50V (0402)	GRM36X7R471K050	Murata
D1	Diode, 0.5A, 30V	UPS530	Microsemi
L1	Inductor, Coupled, 22uH	CLS62-220NC	Sumida

Table 1 - Part List for Figure 1 (All Parts Are Surface Mount).

Separate inductors (not on a common core) can be used in place of the coupled inductor (L1) of Figure 1. In this case the only component that changes in the parts list is L1, which now would be two separate inductors (L1, formerly L1A, and L2, formerly L1B). With the separate inductors the peak-to-peak voltage ripple on the input the output were less the 2mV_{P-P} and less than 500µV_{P-P}, respectively.

Table 2 - Part List For Alternative Inductors

Ref. Designator	Description	Part Number	Manufacturer
L1, L2	Inductor, 47uH, (1812)	LQH4C470K04M00	Murata

Inductor Selection

When the LX1734 is used in a dual inductor converter with coupled inductors, a parallel winding inductor value of 22µH works well for a 5V input and a -5V output at 150mA. The inductor value can be scaled to the particular set of operating conditions based on the input voltage, output voltage, and output current. The new value of coupled inductor parallel inductance can be calculated using the following equation:

$$L_{NEW} = 22\mu H \times \left(\frac{V_{IN}}{5\,V}\right) \times \left(\frac{150\,mA}{I_{OUT}}\right) \times \left(\frac{-5\,V}{V_{OUT}}\right)$$

The inductor value should be rounded to the nearest available value. The parallel saturation current rating of a coupled inductor should be sized to carry the summation of the peak input and peak output inductor currents.

When the LX1734 is used in a dual inductor converter with two separate (uncoupled) inductors or when using the boost converter with an inverting charge pump output configuration, the inductance value for each inductor should be about twice the value recommended for a coupled inductor.

The peak current in the inductor is the DC current plus ½ of the peak-to-peak ripple current. The saturation current rating of the inductors should be sized to carry the peak inductor current. The peak-to-peak ripple current can be calculated based on the inductor value, the terminal voltage (input or output), and the duty cycle. The DC inductor current is the same as the DC output current on the output inductor. The DC input current includes the power for the LX1734, but is still a good approximation for the DC inductor current for higher power applications. For simplicity, the calculations below ignore the voltage drops of the switch and diode.

The duty cycle, D, for the dual inductor topology (assuming continuous inductor current mode operation) is approximately:

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APPLICATION NOTE (CONTINUED)

$$D = \frac{V_{OUT}}{(V_{OUT} - V_{IN})} \quad \text{where } V_{OUT} < 0$$

For example, the duty cycle for +5V = VIN and –3.3V = VOUT is 40%.

The duty cycle for the Inverting Charge Pump Output topology (assuming continuous inductor current mode operation) is approximately:

$$D = 1 + \left(\frac{V_{IN}}{V_{OUT}}\right) \quad \text{where } V_{OUT} < 0$$

For example, the duty cycle for +5V = VIN and –12V = VOUT is 58%.

The peak-to-peak ripple current in the input inductor is approximately:

$$I_{RIPPLEpp} = \frac{(V_{IN} \times D)}{(L_{IN} \times Fsw)}$$

where Fsw = 1.0MHz (the switching frequency)

For example, with a +5V input and a-12V output in an Inverting Charge Pump Output topology with a 47µH inductor, the peak-to-peak input ripple is 52mA.

In the dual inductor topology with separate inductors, the peak-to-peak ripple current in the output inductor is approximately:

$$I_{RIPPLEpp} = \frac{[-V_{OUT} \times (1 - D)]}{(L_{OUT} \times Fsw)}$$

For example, with a +5V input and a -3.3V output in a dual inductor topology with a 47µH output inductor, the peak-to-peak output ripple is 35mA.

There are many inductor models from many different manufacturers that work well with the LX1734. Some sources are listed in Table 5. Ferrite core inductors are recommended to reduce core losses due to the high operating frequency of the LX7134. Using inductors with low DC resistance will further reduce efficiency losses.

Vendor	Phone	URL	Part	Comments
Sumida	(847) 956-0666	www.sumida.com	CLS62-22022 CD43-470	22µH Coupled 47µH
Murata	(404) 436-1300	www.murata.com	LQH3C-220	22µH, 2mm Height
Coiltronics	(407) 241-7876	www.coiltronics.com	CTX20-1	20µH, Coupled, Low DCR

Table 5 – List of Inductor Vendors

Capacitor Selection

To minimize ripple voltage, only capacitors with low series resistance (ESR) are recommended. Mutli-layer ceramic capacitors with X5R or X7R dielectric are an excellent choice featuring small size, very low ESR, and a temperature stable dielectric. The level shifting capacitor, C2 (of Figure 1), should have a value of 1µF and a voltage difference between the input and output voltages. The input and output capacitors (C1 and C2, respectively) should have values in the range of 1µF or larger. If the inductor ripple current is known, the ripple voltage can be estimated by the following equation:

$$V_{PP(RIPPLE)} = \frac{(I^2_{PPRIPPLE} \times L)}{(2 \times C \times V)}$$

Since ripple voltage is inversely proportional to the capacitor value, larger value ceramic capacitors will result in lower ripple voltages. When using a ceramic capacitor for the output capacitor, it is recommended that a phase lead network be inserted in the feedback loop to improve the transient response. This can be accomplished by placing a capacitor in parallel with resistor R1 (see Figure 1). The corner frequency for the phase lead zero is between 20KHz and 60KHz. C4 can be calculated using the following equation:

$$fz = \frac{1}{(2\pi \times R1 \times C4)}$$

Electrolytic capacitors such as solid tantalum or OS-CON types can also be used with consideration for the ESR. Since ESR adds to the capacitor reactive impedance, ESR will increase the ripple voltage. The electrolytic output capacitor impedance has a built in zero, so adding C4 is usually not required when using an electrolytic capacitor.

Diode Selection

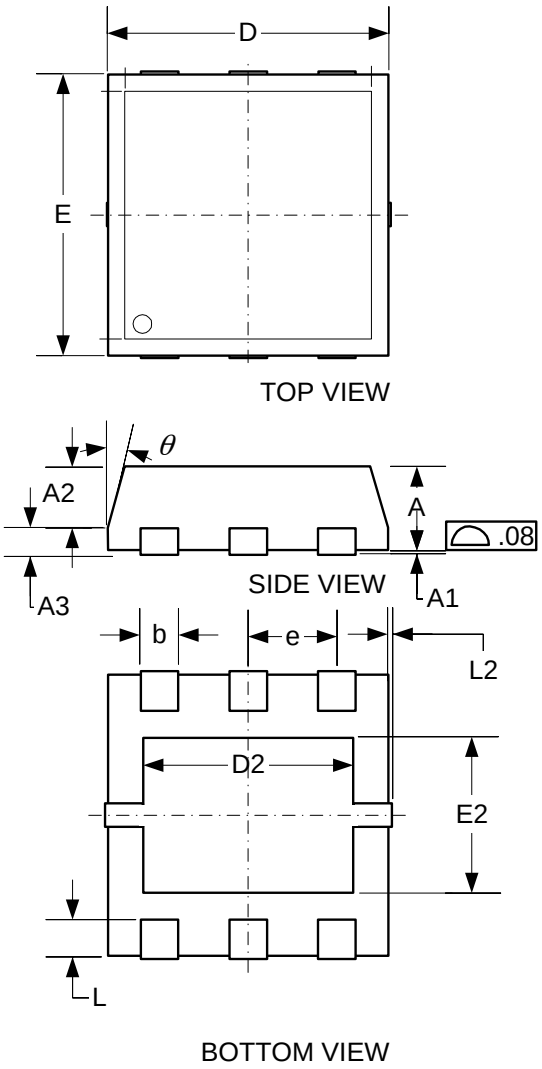
A Schottky diode is recommended for use with the LX1734. The Microsemi UPS530 (30V @ 0.5A) or Microsemi UPS5817 (20V @ 1A) are good choices.

Layout Considerations

In operation, current is transferred between the LX1734 and D1 so to minimize ground noise it is recommended that the D1 cathode be connected directly to the ground pin pad for the LX1734 (refer to figure 1). When laying out the converter, to minimize EMI, it is important to minimize the area enclosed within the main current loops. It is also important to minimize the length of etch connecting to pin 3 (NFB) and to minimize the total trace area on both sides of C2. A ceramic bypass capacitor should be connected between pin 5 (VIN) and pin 2 (GND) and located in close proximity to the LX1734.

PACKAGE DIMENSIONS

LM 6-Pin Plastic Exposed Pad JEDEC MO-229 Reference



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.05	0.031	0.041
A1	*	0.05		0.002
A2	0.65	0.75	0.025	0.295
A3	0.15	0.25	0.006	0.010
b	0.33	0.45	0.012	0.017
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.95 BSC		0.037 BSC	
D2	1.78	2.34	0.070	0.092
E2	1.01	1.57	0.039	0.061
L	0.20	0.45	0.007	0.017
L2	---	0.13	---	0.005
K	0.20	*	0.007	*
θ	0°	12°	0°	12°

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES

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