Microsemi

LX3301A

Inductive Sensor Interface IC with Embedded MCU

Description

The LX3301A is a highly integrated programmable data conversion IC designed for interfacing to and managing of inductive sensors. The device includes an integrated oscillator circuit for driving the primary coil of an inductive sensor, along with two independent analog conversion paths for conditioning, converting, and processing of sine and cosine analog signals from the secondary coils of the sensor. Each path includes an EMI filter, demodulator, anti-alias filter, programmable amplifier, and a 13-bit sigma-delta analog-to-digital converter.

Each analog signal path includes digital calibration capability which allows the complete analog path (including the external sensors) to be calibrated during the system manufacturing process. The calibration information is written to internal EEPROM resulting in improved production yields, and in-line system upgrades.

The LX3301A integrates a 32-bit RISC processor which provides programmable digital filtering and signal processing functions. The MCU resources include 12 kilo bytes of program memory, 128 bytes of SRAM, and 32 bytes of user programmable EEPROM. The program memory is available as mask-programmed ROM.

System interfaces include programmable PWM output and a 12-bit digital-to-analog converter analog buffed output.

The LX3301A is offered in TSSOP14, the device is specified over a temperature range of -40°C to +125°C making it suitable for a wide range of commercial, industrial, medical, and/or automotive sensor applications.

Features

- Built-in Oscillator for Driving Primary Coil
- Two Independent Analog Channels With Demodulation
- 32-Bit RISC MCU with 12k Bytes of Program Memory
- 128 Bytes SRAM
- 32 Bytes EEPROM
- Two Programmable Gain Amplifiers
- Two Anti-alias Filters
- Two 13-bit ADCs
- Selection of SINC and FIR Digital Filters
- One 12-bit DAC
- One 16-bit PWM
- Multiple Faults Detection and Protection
- Reverse Power Protection
- Digital Calibration with Non-volatile Configuration Storage (EEPROM)
- Protected Watchdog Timer
- Low Temperature Drift
- -40°C to 125°C Operation
- TD, PWM(push-pull), PWM (OD) Output
- Excellent Long Term Stability
- AEC-Q100 Certification
- ISO26262 Compliant

Applications

- Automotive Control
- Medical Equipment
- ATE Equipment
- Industrial Process Control
- Smart Energy Saving Control

Typical Application

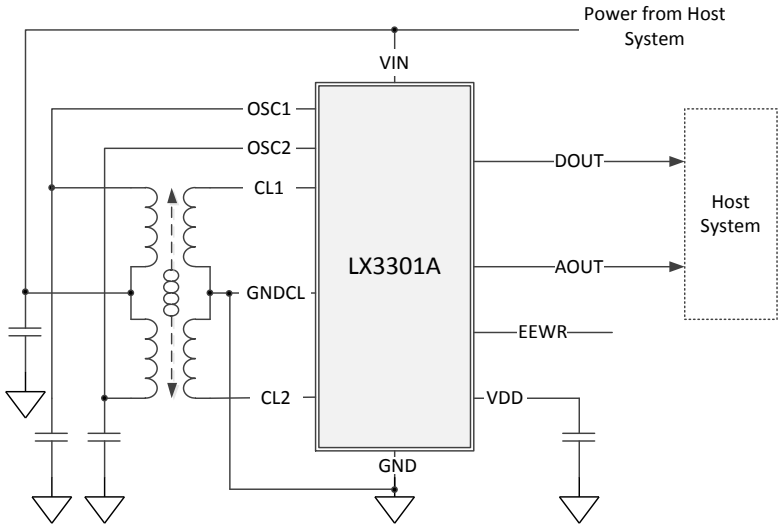


Figure 1 · Typical Application System Diagram: LX3301AQPW

Block Diagram

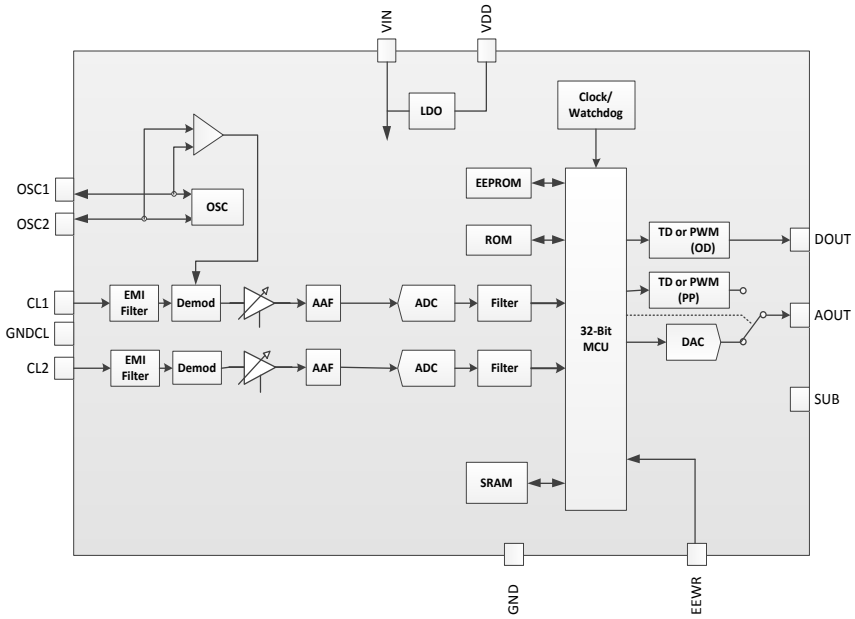
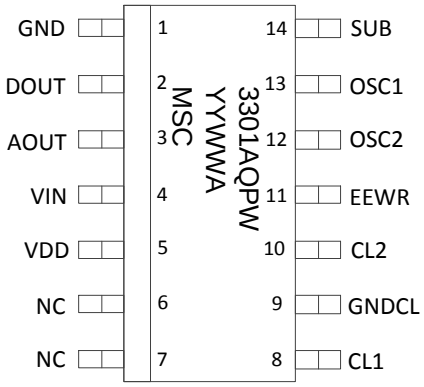


Figure 2 · LX3301A Block Diagram

Pin Configuration



14-Pin TSSOP

Figure 3 · Pinout (Top View)

Matte Tin Lead Finish / MSL 1

YYWWA = Year/ Week/Lot Code

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 125°C	RoHS2 compliant, Pb-free	14-TSSOP	LX3301AQPW	Bulk / Tube
			LX3301AQPW-TR	Tape and Reel

Thermal Data

Parameter	Value	Units
Thermal Resistance-Junction to Ambient, θ_{JA}	103.7	°C/W

Note: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta J_A)$. In particular, θJ_A is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Pin Description

PIN#	Pin Designator	Description
1	GND	Analog and digital power ground
2	DOUT	Digital Out. This pin can be programmed to Open-drain PWM with current limit, or the threshold detector output.
3	AOUT	Analog Out. This pin can be programmed to provide an analog output (DAC), TD or a PWM output. PWM will be push-pull operation. This pin can be used as address pin for EEMODE
4	VIN	Power supply and internal EEPROM program pin. DC input power is applied to this pin for normal operation. Also used for EEPROM programming (refer to application information). Bypass this pin to GND pin with a low ESR capacitor of 100nF. Note that larger capacitance will affect the EEPROM programming.
5	VDD	Regulator output. This is the output of the internal voltage regulator providing power to the analog and digital blocks. Bypass this pin to GND pin with a low ESR capacitor of not less than 1µF.
6	NC	Reserved for factory testing. Connect it to GND
7	NC	Reserved for factory testing. Connect it to GND
8	CL1	Sensor signal from secondary coil 1 of inductive sensor.
9	GNDCL	Reference ground for CL1 and CL2. Connect CL1 & CL2 coil to GNDCL and connect the GNDCL to GND directly.
10	CL2	Sensor signal from secondary coil 2 of inductive sensor.
11	EEWR	EEWR is active low. When EEWR is low, it prohibits change to the internal EEPROM contents.
12	OSC2	Oscillator pin 2. Connects to the second side of the primary inductor coil. An external capacitor is connected between this pin and GND as part of the LC tank circuit.
13	OSC1	Oscillator pin 1. Connects to the first side of the primary inductor coil. An external capacitor is connected between this pin and GND to as part of the LC tank circuit.
14	SUB	Substrate pin it is used for ground failure protection. It should not be connected to GND, for normal application, leave this pin open

Absolute Maximum Ratings

Parameter	Value	Units
Supply Input Voltage (VIN)	-7 to 20	V
Load Current on VDD	-1 to 15	mA
Voltage on OSC1, OSC2	-0.3 to 16	V
Voltage on CL1, CL2, EEWR	-0.5 to 3.6	V
Voltage on AOUT, DOUT	-0.5 to 16	V
Operating Humidity (non-condensing)	0 to 95	%
Operating Temperature	-40 to 125	°C
Storage Temperature	-40 to 150	°C
Lead Temperature (Soldering 10 seconds)	300	°C
Package Peak Temp. for Solder Reflow (40 seconds exposure)	260	°C
ESD, Human Body Model (HBM) AEC-Q100-002D	±2	kV
ESD, Charge Device Model (CDM) AEC-Q100-011	750	V

Note: Stresses in excess of these absolute ratings may cause permanent damage. The device is not implied to be functional under these conditions. All voltages are with respect to GND.

Recommended Operating Range

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage	VIN	For normal operating	4.4	5	5.6	V
EEPROM Program High	VIN_PH				17	V
Supply Current	I_IN	For normal operating, excluding oscillator tail current			10	mA
Output Current	I_{AOUT0}	AOUT = 0V	-15		-8	mA
Output Current	I_{AOUT5}	AOUT = 5V	6		15	mA
Output Current	I_{DOUT0}	DOUT = 0V			28	mA
Internal Clock Frequency	F_{OSC}		8.0	8.2	8.4	MHz
Operating Temperature	T_{OP}		-40		125	°C

Electrical Characteristics

Unless otherwise defined, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ 125°C, and the following test conditions: VIN = 5V, VDD=3.5V, IDD=5mA, II/O=0mA – Typical values are at 25 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
POWER						
Supply Voltage	VIN	For normal operating	4.4	5	5.6	V
Supply Current	IIN	For normal operating , excluding oscillator tail current ,IDD = 0mA, II/O = 0mA, f = 8.2MHz		8	10	mA
VIN UVLO High Threshold	VIN_UVLO_HI		4.1		4.3	V
VIN UVLO Low Threshold	VIN_UVLO_LO	AOUT goes low	3.6	3.75	4.1	V
VOLTAGE REFERENCE						
Output Voltage	VDD	IDD = 10mA, Trimmed	3.45	3.5	3.55	V
VDD UVLO	VDD_UVLO	Rising edge	2.9		3.4	V
Output Current	IDD	Additional current sourced to external load(s)			10	mA
OSCILLATOR						
Middle Tap Voltage	VTAP			5		V
Total Tank DC Driving Current	ITK	VTAP = 5V	0		10	mA
Swing Voltage of OSC1&2	VOSC	VTAP = 5V	3		9.5	Vpp
Reference Frequency Range	FOSC	VTAP = 5V	1		5	MHz
Frequency Variation	FOSCTOL	VTAP = 5V	-5		5	%
Reference Inductance	LOSC	VTAP= 5V, Inductor connected to OSC1,2 pins		6		µH
Tank Circuit Quality Factor	QOSC	VTAP = 5V	15	25		
Harmonics	HOSC	VTAP = 5V, GBNT			2	%
Resistance between OSC1 & VIN	ROSC1_VIN	VIN = 5V, OSC1 = GND, Measure Current from OSC1 to GND	1			MΩ
Resistance between OSC2 & VIN	ROSC2_VIN	VIN = 5V, OSC2 = GND, Measure Current from OSC2 to GND	1			MΩ
Resistance between OSC1 & GND	ROSC1_GND	VIN = 0V, OSC1 = 5V, Measure Current from OSC1 to 5V	1			MΩ
Resistance between OSC2 & GND	ROSC2_GND	VIN = 0V, OSC2 = 5V, Measure Current from OSC2 to 5V	1			MΩ
Resistance Between OSC1&OSC2	ROSC1&2_HI	OSC1 = 1Vpp, OSC2 = GND	500			kΩ
CL1 & CL2						
Peak to Peak Sensor Signal	Vpp_CL	VTAP = 5V,	50	100	150	mV
EMI FILTER 1 & 2						
Cut-off Frequency	EF01	GBNT	13.5			MHz
DEMODULATOR AND FRONT-END AMPLIFIER 1, 2						
Demodulator Gain	DAA01	GBNT		7		V/V
Front-End Gain Range	DAA02	GBNT, Front End = 0000b to 1111b	2.375	3.125	3.781	V/V
Front End Gain Step	DAA03			3		%
ANTI ALIAS FILTER 1 & 2						

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Cut-off Frequency	AAF01	GBNT		24		kHz
Attenuation	AAF02	GBNT		-60		dB/dec
ADC1 & 2						
ADC Resolution	ADC01		13			bits
Offset Drift	ADC02	GBNT	-5	0	5	mV
Integral Non-Linearity	ADC03	GBNT	-1		1	LSB
Absolute Offset Error	ADC04	GBNT			8	mV
SINC, SINC+FIR Filter 1 & 2						
Pass band	PB00	REFRESH=00,(SINC,SINC+FIR)		1		kHz
Pass band	PB01	REFRESH=01, (SINC,SINC+FIR)		500		Hz
Pass band	PB03	REFRESH=10, (SINC,SINC+FIR)		250		Hz
Pass band	PB04	REFRESH=11, (SINC,SINC+FIR)		125		Hz
Stop band	SB000	REFRESH=00, FILTER=0		2		kHz
Stop band	SB001	REFRESH=01, FILTER=0		1		kHz
Stop band	SB002	REFRESH=10, FILTER=0		500		Hz
Stop band	SB003	REFRESH=11, FILTER=0		250		Hz
Stop band	SB100	REFRESH=00, FILTER=1		1.4		kHz
Stop band	SB101	REFRESH=01, FILTER=1		700		Hz
Stop band	SB102	REFRESH=10, FILTER=1		350		Hz
Stop band	SB103	REFRESH=11, FILTER=1		175		Hz
Stop Band Attenuation	SBA	Stop band			1	%
Delay	Delay000	REFRESH=00, FILTER=0		0.25		ms
Delay	Delay001	REFRESH=01, FILTER=0		0.5		ms
Delay	Delay002	REFRESH=10, FILTER=0		1		ms
Delay	Delay003	REFRESH=11, FILTER=0		2		ms
Delay	Delay100	REFRESH=00, FILTER=1		0.5		ms
Delay	Delay101	REFRESH=01, FILTER=1		1		ms
Delay	Delay102	REFRESH=10, FILTER=1		2		ms
Delay	Delay103	REFRESH=11, FILTER=1		4		ms
Data Update Rate	DUR00	REFRESH=00,(SINC,SINC+FIR)		2		kHz
Data Update Rate	DUR01	REFRESH=01, (SINC,SINC+FIR)		1		kHz
Data Update Rate	DUR02	REFRESH=10, (SINC,SINC+FIR)		500		Hz
Data Update Rate	DUR03	REFRESH=11, (SINC,SINC+FIR)		250		Hz
Filter SNR	FLTRSNR	GBNT		-86	-73	dB
Cross Talk Rejection	CTR	GBNT		-44		dB
Power supply rejection ratio	PSRR	GNBT		-86		dB
Internal Clock						
Clock Frequency	FCLK	After Trimming	8	8.2	8.4	MHz
Processing Resources						
MCU Data bus	MCU01			32		bit
MCU Instruction size	MCU02		16		32	bit
ROM Size	MCU03	32-bit words		12		KB
SRAM Size	MCU04	Application data, 32-bit words		128		byte

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
EEPROM Write Endurance	MCU05		10000			cycles
EEPROM Size	MCU06	(16-bit words)		16		words
Watchdog Timer						
Watchdog time, PUST	TPUST	Timer for Power Up Self- test (PUST)		16.3		ms
Watch dog time,	TOP	Timer after completion PUST		10		ms
Watchdog time, EEMode	TEE	Timer for EE Mode, after receiving command and matching address bits		100		ms
DOUT (PWM, OPEN DRAIN)						
Frequency	DOUT01	Refresh= 2kHz, after trimming, 25°C	1.945	2	2.055	kHz
Minimum PWM duty	DOUT02	HCLMP=1023, LCLMP=0, ORIGIN=0, frequency = 2kHz		0.125		%
Maximum PWM duty	DOUT03	No Clamped Output			100	%
PWM Jitter	DOUT04			0.2		%D
Max Sink Current	DOUT05	DOUT = OD PWM, or TD	-27		28	mA
AOUT (AS ADDRESS SELECTION)						
Hi-level Input Voltage	AOUT_VIH		2.0			V
Low-level Input Voltage	AOUT_VLO				0.3	V
AOUT (ANALOG OUTPUT)						
AOUT Analog Range	AOUT_R		0		VIN	V
AOUT Low Voltage	VAOUT_LO	RL_AOUT = 10kΩ to VIN			4	%VIN
AOUT High Voltage	VAOUT_HI	RL_AOUT = 10kΩ to GND	96			%VIN
AOUT Output load	RL_AOUT		1	10		kΩ
AOUT Sink current	IAOUT0	AOUT = 0V	-15		-10	mA
AOUT Source Current	IAOUT5	AOUT = 5V	6		15	mA
AOUT Slew Rate	AOUTSR1	C_{LOAD} = 22nF		0.2		V/µs
AOUT Slew Rate	AOUTSR2	C_{LOAD} = 100nF		0.1		V/µs
Ratiometric Error	VRatioErr		-0.2	0	0.2	%VIN
FAULT Output Low Level	VAOUT_FL10K	RL_AOUT = 10kΩ to VIN			1	%VIN
FAULT Output Low Level	VAOUT_FL1K	RL_AOUT = 1kΩ to VIN			1.5	%VIN
FAULT Output High Level	VAOUT_FH10K	RL_AOUT = 10kΩ to GND	98			%VIN
FAULT Output High Level	VAOUT_FH1K	RL_AOUT = 1kΩ to GND	97			%VIN
Ground Off Output low Level	VAOUT_GF10K	Broken GND, RL_AOUT ≤ 10kΩ to GND			4	%VIN
Ground Off Output High Level	VAOUT_GF1K	Broken GND, RL_AOUT ≥ 1kΩ to VIN	99	100		%VIN
VIN Open output Low Level	VAO_VIN1K	Broken VIN, RL_AOUT ≥ 1kΩ to GND		0	1	%VIN
AOUT (PWM Output)						
High level output voltage	VOH	Duty =50%, 10kΩ Pull-down to GND	95		100	%VIN
Low level output voltage	VOL	Duty=50%, 10kΩ Pull Up to VIN	0		200	mV
Rise time	AOUT_TR	Duty=50%		10		µs
Fall time	AOUT_TF	Duty=50%		10		µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Min Duty	Dmin_Aout	PWM(PP)			4	%
Max Duty	Dmax_Aout	PWM(PP)	94			%
Max Drive/Sink Current	IAOUTP	AOUT=PWM	-25		25	mA
Output CLAMP						
Clamp High Output Level	HCLMP	Pull Output up to VIN	0		100	%VIN
Clamp High Output Level	LCLMP	Pull Output up to VIN	0		100	%VIN
EEPROM Programming						
Program Low	VIN_PL	For EEPROM programming mode	9.5	10	10.5	V
Program Idle	VIN_PI	For EEPROM programming mode	11.75	13	13.5	V
Program High	VIN_PH	For EEPROM programming mode	14.75	16	17	V
Duration time	td	Duration time each voltage state	10			µs

Configuration EEPROM

The LX3301A integrates a 16 Words X 16bits (256bits), user programmable EEPROM for storing calibration and configuration parameters. The calibration parameters enable the production sensor assembly to be customer-factory calibrated assuring consistent unit to unit performance. The following FIG1 shows LX3301AQPW EEPROM configuration map and table 1 itemizes the LX3301A configuration EEPROM contents:

Name	Description	Size (bit)	Word & Bits (MSB:LSB)	Sign	Min Value	Max Value	Default Value
ID	Customer Part ID	18	W0[15:0]W1[15:14]	No	0	3FFFF	
REFRESH	Refresh rate	2	W1[13:12]	No	0	3	0
FACTORY	Microsemi Factory programming	12	W1[11:0]	No			
CHKSUM	4bit checksum value	4	W2[15:12]	No	0		
S5	Slope of 6th segment	12	W2[11:0]	No	0	4095	511
OUTSEL	Output Set up	4	W3[15:12]	No			1011B
S0	Slope of 1st segment	12	W3[11:0]	No	0	4095	511
ORIGIN	Origin	12	W4[15:12]W5[15:12] W6[15:12]	No	0	4095	0
Y5		12	W4[11:0]	No	0	4095	3413
X5		12	W5[11:0]	No	0	4095	3413
Y3		12	W6[11:0]	No	0	4095	2047
OSCOMP	OSC voltage Compensation	8	W7[15:12]W8[15:12]	No	0	255	255
X3		12	W7[11:0]	No	0	4095	2047
Y1		12	W8[11:0]	No	0	4095	683
FILTER	Select digital filter	1	W9[15]	No	0	1	1
TDHYST	Threshold Detect hysteresis	3	W9[14:12]	No	0	112	111B
X1		12	W9[11:0]	No	0	4095	683
TD	Threshold Detect	12	W10[15:10]W11[15: 10]	No	0	4095	3685
LCLMP	Low Clamp	10	W10[9:0]	No	0	1023	0
HCLMP	High Clamp	10	W11[9:0]	No	0	1023	1023
Y2	Y2 with Sign	6	W12[15:10]	Yes	-31	31	0
DSIN	Dynamic Sine Offset	10	W12[9:0]	Yes	-511	511	0
Y4	Y4 with Sign	6	W13[15:10]	Yes	-31	31	0
SSIN	Static Sine Offset	10	W13[9:0]	Yes	-511	511	0
IOSC	Osc current Source	2	W14[15:14]	No	0	3	0
DEBUG	Debug	1	W14[13]	No	0	1	0
TDPOL	TD Polarity	1	W14[12]	No	0	1	0
CLSEL	CL1,2 input select	1	W14[11]	No	0	1	0
EELOCK	EEPROM Write Protection	1	W14[10]	No	0	1	0
DCOS	Dynamic Cosine Offset correction	10	W14[9:0]	Yes	-511	511	0
GMTCH	Gain Match	6	W15[15:10]	Yes	-12.09%	12.09%	0
SCOS	Static Cosine offset Correction	10	W15[9:0]	Yes	-511	511	0

Table 1 - LX3301AQPW Configuration EEPROM

	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
WORD0	ID[17..2															
WORD1	ID[1..0]		REFRESH		FACTORY[11..0]											
WORD2	CHKSUM[3..0]				S5[11..0]											
WORD3	OUTSEL[3..0]				S0[11..0]											
WORD4	ORIGIN[11..8]				Y5[11..0]											
WORD5	ORIGIN[7..4]				X5[11..0]											
WORD6	ORIGIN[3..0]				Y3[11..0]											
WORD7	OSCOMP[7..4]				X3[11..0]											
WORD8	OSCOMP[3..0]				Y1[11..0]											
WORD9	FILTER	TDHYST[2..0]			X1[11..0]											
WORD10	TD[11..6						LCLMP[9..0]									
WORD11	TD[5..0]						HCLMP[9..0]									
WORD12	Y2[5..0]						DSIN[9..0]									
WORD13	Y4[5..0]						SSIN[9..0]									
WORD14	IOSC[1..0]		FMSK	TDPOL	CLSEL	EELOCK	DCOS[9..0]									
WORD15	GMTCH[5..0]						SCOS[9:0]									

FIG. 1 - LX3301AQPW Configuration EEPROM MAP

- **ID**

  This is ID field. The Customer Part ID is a 18-bit field containing customer part identification information.

- **CHKSUM**

  This 4bit value is a 4bit CRC(cyclic redundancy check) to check the rest of content reliability through lifetime. The CRC calculation is based on the following code:

```
#define GENPOLY 0x0013U /* x^4 + x + 1 */
uint32_t makecrc4(uint32_t b);


uint32_t makecrc4(uint32_t b)
/*
  * Takes b as input, which should be the information vector
  * already multiplied by x^4 (ie. shifted over 4 bits), and
  * returns the crc for this input based on the defined generator
  * polynomial GENPOLY
  */
{
   uint32_t i;

   i=1U;
  while (b>=16U) { /* >= 2^4, so degree(b) >= degree(genpoly) */
     if ((((b >> (20U-i))) & 0x1U) == 1U)
     {
       b ^= GENPOLY << (16U-i); /* reduce with GENPOLY */
     }
```

```
    i++;
  }
  return b;
}

      /*  Cacluate EEPROM checksum */
      sum1=0U;
      for(counter=1U; counter<=16U; counter++)
            {
                  if (counter!=3U)
                  {
                        sum1+=*EEPROM_address;
                  }
                  else
                  {
                        sum1+=*EEPROM_address&0x0FFFU;
                  }

                  current_address+=4U;
                  EEPROM_address=current_address;
            }
      sum2 = makecrc4(((sum1 >> 16)^(sum1&0xFFFFU)) << 4);
```

- **FACTORY**

  This parameter is used to trim the VDD, internal clock frequency and analog front-end amplifier gain. The FACTORY bits contain factory trimmed information. Recommend not to change. Always read first and preserve these factory values for future reuse.

Oscillator Trim

The Bit W1[11:7] of the EEPROM is used to set internal clock frequency. This is factory trimmed. Please keep this value as original value before writing the EEPROM.

VDD Trim

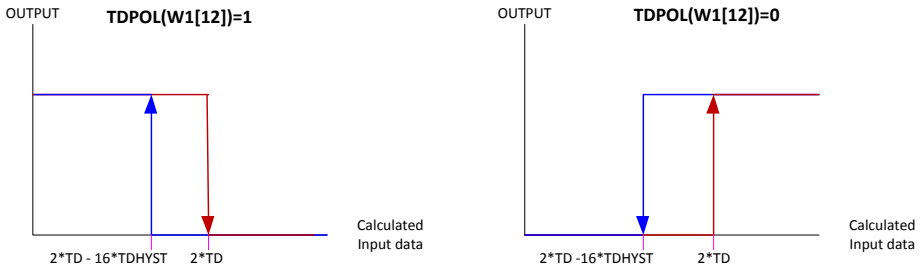
The Bit W1[2:0] of the EEPROM is used to set VDD voltage. This is factory trimmed. Please keep this value as original value before writing the EEPROM.

Front-End Gain AMPLIFIER

The Bit W1[6:3] of the EEPROM is used to adjust the FRONT-END GAIN AMPLIFIER gain. The bit W1 [6] is polarity bit, rest three bits(5:3) adjust gains. Default gain [00000b] is 3.125. Each step changes approximately 3% gain. Smallest number is 1000, largest number is 0111.

- **TD ,TDHYST and TDPOL**

  The TD output is enabled using “OUTSEL”. Output polarity of TD is set by “TDPOL”. When TDPOL is set to 1, then the output pin goes low when the input signal exceeds the 2*TD value, and output pin goes high when the input signal exceeds the (2*TD-16*TDHYST) value. If TDPOL is set to 0, then the output pin goes high when the input signal exceeds the 2*TD value and output pin goes low when the input signal lower than the (2*TD-16*TDHYST) value. TDHYST is used to set the hysteresis value of TD level.



- **FILTER**

  This bit selects the digital filter type. If the bit =0, then SINC and if the bit =1 then SINC+FIR.

Filter Bit	Filter Type
0	SINC
1	SINC+FIR

Table 2 - Filter Configuration

- **REFRESH**

  This parameter sets the value of the refresh rate of ADC update. If the PWM output is selected the PWM frequency is always equal to the ADC update rate.

Bit Value	Refresh Rate
0	2kHz
1	1kHz
2	500Hz
3	250Hz

Table 3 - Refresh Bits Configuration

- **IOSC**

  These two bits set the Oscillator Tail Current value.

IOSC Bits	Tail Current	Feedback
0	Full Range	Enabled
1	1/2	Enabled
2	1/4	Enabled
3	1/8	Enabled

Table 4 - IOSC Bits Configuration

- **EELOCK**

  There are two control signals, one is from the EEWR pin (Active Low – disable to Write EEPROM at EEMODE), and other is the EELOCK bits on the configuration EEPROM(W14[10]). If the EELOCK bit is set to 1 and EEWR pin is pulled to low, then EEPROM cannot be written. Default value of W14[10] is 0.

- **OUTSEL**

  The OUTSEL bits provide the various output selection option. Table 5 shows the OUTSEL bits versus output option.

Output Configuration				Remarks
Bit 1, Bit 0	AOUT	Bit 3, Bit 2	DOUT	
00	TD	00	TD	
01	PWMB(PP)	01	OD_PWMB	Inverted PWM
10	PWM(PP)	10	OD_PWM	PP=Push Pull, OD=Open Drain
11	Analog	11	Reserved	

Table 5 - OUTSEL Bits Configuration

- **SCOS**

  Static Offset Correction of CL1 input channel used in inputs correction calculation.

- **DCOS**

  Dynamic Offset Correction of CL1 input channel used in inputs correction calculation.

- **SSIN**

  Offset Correction of CL2 input channel used in inputs correction calculation.

- **DSIN**

  Dynamic Offset Correction of CL2 input channel used in inputs correction calculation.

- **GMTCH**

  Value of the input channel gain mismatch correction gain used in inputs correction calculation.

- **OSCOMP**

  Maximum amplitude of the oscillator swing used in the inputs correction calculation. The maximum value of the OSCOMP is 255, step 1. Multiplied by 4 to convert as internal OSCOMP data.

- **ORIGIN**

  Offset value of the system origin relative to fore-and-after position. This is not a DC output offset adjustment. Verify LCLMP and HCLMP parameters are not limiting the output range. Multiplied by 2 to convert as internal ORIGIN data.

- **HCLMP**

  This parameter is set to high clamp level of output. Output will be clamped at this value if output swing can go above this level. The HCLMP value used in calculation is 8*value on W11[9:0]. It reduces the maximum output swing. Maximum level is achieved with HP = 1023.

- **LCLMP**

  This parameter sets the low clamp level of output. The output is clamped at this level if output swing can go below this level. The LCLMP value raises the minimum output value from zero. The LCLMP value used in calculation is 8*value on W10[9:0]. An output value of “zero” is achieved with LCLMP = 0. LCLMP setting value will overrides the HCLMP setting if both setting are crossed over.

- **S0**

  Slope of first linearization segment.

- **X1 and Y1**

  Value of the X and Y coordinates for the first linearization point. Multiplied by 2 to convert as internal data.

- **X3 and Y3**

  Value of the X and Y coordinates for the third linearization point. Multiplied by 2 to convert as internal data.

- **X5 and Y5**

  Value of the X and Y coordinates for the fifth (and last) linearization point. Multiplied by 2 to convert as internal data.

- **S5**

  Slope of the last linearization segment.

- **Y2**

  Value of the X2 is calculated by X1, X3 parameters as X2= (X1+X3)/2. Y2 value is the value that can adjust the coordinates for the second linearization point. Y2 value has polarity and calculated value of second coordinate (y) at X2 is y= (Y1+Y3)/2 + Y2. Multiplied by 2 to convert as internal data.

- **Y4**

  Value of the X4 is calculated by X3, X5 parameters as X4= (X3+X5)/2. Y4 value is the value that can adjust the coordinates for the fourth linearization point. Y4 value has polarity and calculated value of fourth coordinate (y) at X4 is y= (Y3+Y5)/2 + Y4. Multiplied by 2 to convert as internal data.

- **CLSEL**

  CLSEL bit selects CL1 or CL2 inputs as sine or cosine input. When CLSEL set to 1, then CL1 input is selected as sine value and CL2 input is selected as cosine input. When CLSEL=0, then CL1 input is selected as cosine value and CL2 input is selected as sine value.

Theory of Operation

Oscillator

The on-chip oscillator provides a carrier signal for driving the primary coil of the inductive sensor via pins OSC1 and OSC2. The carrier signal is generated by an internal current source which resonates with the primary inductors and external capacitors (which forms a tank circuit). The oscillator operates over a frequency range from 1MHz to 5MHz according to the following equation:

$$f = \frac{1}{2\pi\sqrt{LC}}, \quad \text{where L} = \text{Inductance of coil, C} = \text{Tanking capacitance}$$

The value of the inductor L is the most critical element in cross-coupled LC tank oscillator. Because the inductance is relatively small, the parasitic resistance of L can dominate and impact the ability to maintain oscillation. As such, the value of inductor L should be as large as possible and with a high Q factor.

In most applications, the inductor L is implemented as traces on a printed circuit board. Depending upon the processing of the PCB, the height and width of the trace will vary, resulting in a variation of the inductance L and the parasitic resistance. Because these variations will change from PCB to PCB, it is necessary to calibrate each sensor PCB independently. Care should be taken to select a PCB source which can achieve manufacturing tolerances required by a given set of system requirements.

The amplitude of the carrier signal is a function of the primary coil tank circuit configuration and feedback of the secondary coil signals from the CL1 and CL2 inputs. The shoulder signals of the tank circuit are detected by an internal circuit. It will distort the sinusoidal waveform if the tank circuit and secondary coil feedback signal is not within design limits.

In order to detect system faults, the IC monitors the amplitude of the carrier signal on pin OSC1. When the amplitude is above, or below the specified amplitude (reference electrical spec 'OSCILLATOR: V_{OS}, Swing Voltage of OSC1&2') the AOUT output pin will be forced to 0V. This output level indicates a system fault. When initially calibrating a sensor, the voltage on OSC1 should be monitored in order to verify that the amplitude is within the specified range. If the OSC1 voltage is too high, this indicates that the signal levels at CL1 and CL2 may be too low. If the OSC1 voltage is too low, this indicates that the signal levels at CL1 and CL2 may be too high.

An internal feedback circuit adjusts the current drive of the oscillator in order to maintain the signal relationship $a^2 \sin^2\theta + b^2 \cos^2\theta = k^2$; wherein 'k' is the function of the current source amplitude and coefficients 'a' and 'b' are the relative areas of the two secondary coils whose signals are applied to CL1 and CL2. The $a^2 \sin^2\theta$ and $b^2 \cos^2\theta$ are obtained by squaring the two input signals CL1 and CL2. In order to reduce the computation complexity, a and b are typically designed to be matched/equal. When the secondary coils are designed to be equal, the equation becomes $a^2 \sin^2\theta + a^2 \cos^2\theta = a^2$. The letter 'a' in the equation is the fixed amplitude of the sensor signals. In another words, the oscillator circuit adjusts that carrier amplitude such that the input signals into CL1 and CL2 are maximized. This effectively cancels out non-linearity and variations in the sensor design.

Input Amplifier and Signal Conditioning

Pins CL1 and CL2 are the inputs to two analog signal processing paths. The initial block in each path is a first-order EMI filter which has a low pass cut-off frequency of 13.5MHz. Following the EMI filter is a demodulator circuit which removes the carrier such that the relative amplitudes of the CL1 and CL2 signals may be measured. In addition to demodulation, the circuit includes a phase detector which determines the phase of the input signal relative to the oscillator signal. This phase detection effectively generates a sign bit which allows for full 360° resolution in angular measurement applications.

The output of demodulator is fed to the programmable front-end gain amplifier that can be controlled by “Front-End Gain AMPLIFIER Gain” in the configuration EEPROM. The amplifier can be programmable with 4 bits, where the 0000b is default gain value that is 3.125. Bit value percentage changes can be done as shown:

Bit	Function
BIT0	Amplification: +3%
BIT1	Amplification: +6%
BIT2	Amplification: +12%
BIT3	Amplification: -24%

The output of the FRONT-END GAIN AMPLIFIER is then passed through an anti-aliasing filter prior to input to the sigma-delta ADC.

Sigma-Delta ADC with Digital Filters

Each analog path includes a 4th-order 13-bit sigma-delta analog-to-digital converter (ADC) with precision internal voltage reference which produces true 12-bit measurement results. The sampling frequency for the ADC is derived from the main clock and selected by “Refresh” in the configuration EEPROM. The sampling clock for the ADC is derived from the main clock and selected as following table:

Refresh	Function
00	ADC clock=Main clock /8
01	ADC clock=Main clock /16
10	ADC clock=Main clock /32
11	ADC clock=Main clock /64

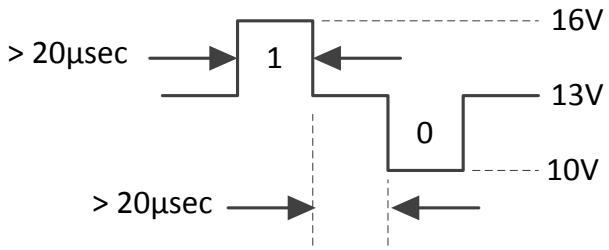
The ADC decimation filter includes a SINC filter and a half-band FIR filter. The SINC filter provides -40dB of stop-band attenuation. Because the SINC filter does not provide the same sharp response as a finite/infinite filter response, a half-band FIR filter is also provided. The drawback of the FIR filter is that it adds delay to the input signal and this delay depends upon the number of coefficients and the output data rate. The filter can be selected by “Filter” in the configuration EEPROM.

Embedded MCU

The LX3301 includes an embedded 32-bit microcontroller core which is used to perform filtering and math functions on the digitized samples from the ADC. The device includes a set of pre-programmed filtering and math functions which can be selected by setting the appropriate bits in the on-chip configuration EEPROM. Also included in the on-chip configuration EEPROM are system calibration and linearization coefficient bits.

Configuration EEPROM

The LX3301A includes a user programmable 16 x 16bits EEPROM for storing configuration parameters into non-volatile memory. The device is placed into EEPROM programming mode (EEMode) by increasing the voltage on the VIN pin to 13V. Note that a delay of 10ms from power-on must be observed before EEPROM programming mode can be entered. Data is represented by one of two voltage levels on the VIN pin: a '1' is represented by increasing the VIN voltage to 16V, while a '0' is represented by decreasing the VIN voltage to 10V. The voltage for a given bit must be held for a minimum duration of 10µsec and between each bit the voltage must return to 13V for a minimum of 20µsec (see diagram below):



The first 3bits sent in EEMode are the command followed by the address bit which is corresponds to the logic level of AOUT. The programming commands are only executed if the address bit and the AOUT logic level match.

For detailed programming, refer to AN-S1410 Application Note for LX3301AQPW EEPROM Programming Guide.

PWM Controller

A 16-bit digital PWM controller is implemented on chip. It can generate a pulse width modulated signal of varying period and duty cycle. The PWM module has a 2 bit pre-scalar to divide down the MCU clock signal. PWM frequency is selected by “Refresh” on configuration EEPROM. PWM mode can be set by “OUTSEL”. When the DOUT PWM is selected, the pull up resistor between DOUT and VIN or VDD is needed, 10kΩ is recommended. PWM frequency is trimmed at factory.

AOUT

AOUT has three functions that it can be programmed to provide either an analog output (amplified from DAC output), TD or a PWM output. PWM will be push pull operation. Also it is used as address pin for EEMODE. For analog output, a 12-bit digital to analog converter is implemented on the chip. The internal DAC supply voltage is VDD. The AOUT is amplified from DAC output and its supply voltage is from VIN. Therefore, AOUT output range is limited by the VIN voltage.

Protection

A versatile set of system diagnostic and protection functions are incorporated on the LX3301A to provide reliable protection of the device and the system. Key fault conditions and outputs status are shown as below table.

Fault condition	Outputs Status	Remarks
VIN under voltage	Tristate	UVLO
VDD under voltage	Forced low	UVLO
VDD unstable or oscillating	Forced low	VDD noise or improper decoupling
CL1,2 disconnected	Forced low	
CL1,2 signal over voltage	Forced low	Re-acquire inputs values at next refresh cycle
CL1,2 signal too low	Forced low	Re-acquire inputs values at next refresh cycle
OSC1 connection fail	Forced low	
OSC1 over voltage	Forced low	
OSC1 under voltage	Forced low	
ROM or RAM test failure at startup	Forced low	Restart by µP
EEPROM reading error or RAM writing failure	Forced low	Restart by µP
Periodic ROM checksum failure	Forced low	Restart by µP
Software does not follow intended execution flow	Forced low	Restart by µP
CPU test vector failure	Forced low	Restart by µP

Reverse Power & GROUND OFF Protection

The LX3301A implements the reverse power protection feature when VIN and GND connections are reversed. When the power is connection are reversed, then internal circuits are disconnected from the supply and the outputs are pulled to ground. Also LX3301A implements the ground off protection feature when the ground is disconnected.

High Voltage LDO

A high voltage, low temperature drift, low-dropout, precision voltage regulator is implemented on chip. The regulator provides the internal power to the chip and also provides power for external components such as pull-up resistors. Decoupling caps is required to ensure high performance analog measurements; recommended value is 1µF. VDD is pre-trimmed at factory.

Reference Schematics

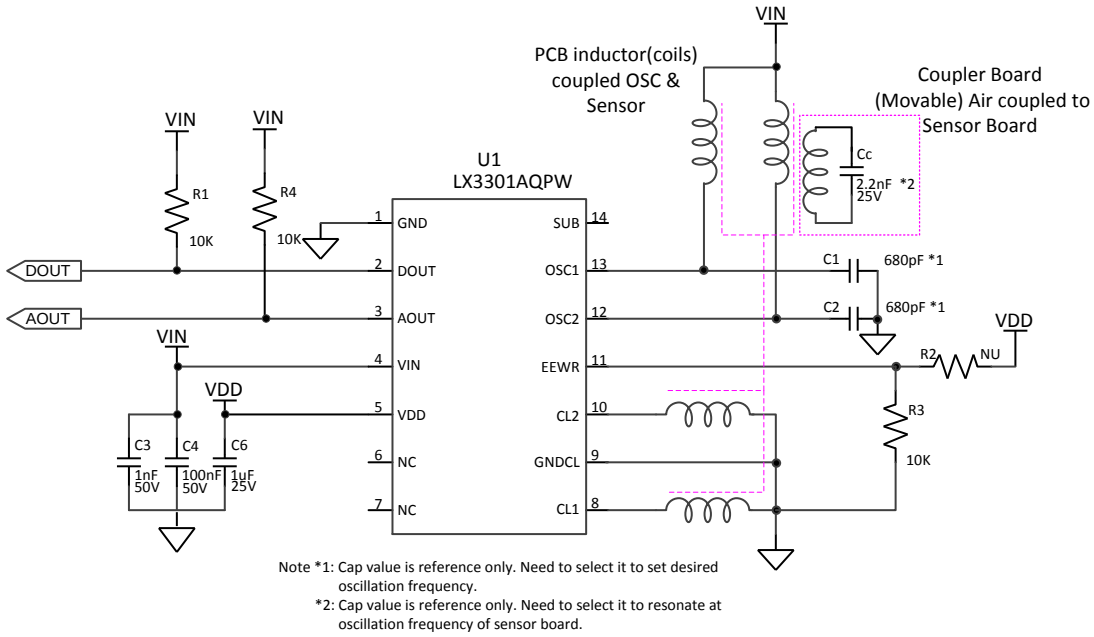
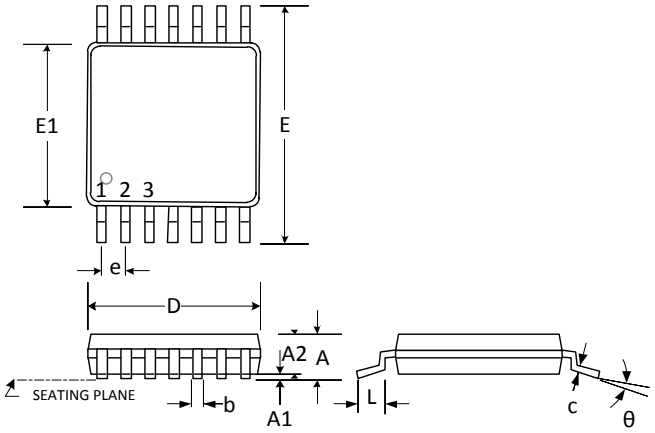


Figure 4 · LX3301A 14-Pin Reference Schematic

Package Outline Dimensions

Controlling dimensions are in millimeters, inches equivalents are shown for general information.



Dim	MILLIMETERS		INCHES	
	MIN	**MAX**	**MIN**	**MAX**
A	–	1.10	–	0.043
A1	0.05	0.15	0.002	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	4.90	5.10	0.193	0.201
E	6.4 BSC		0.252	
E1	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.017	0.030
Θ	0°	8°	0°	8°

*Lead Coplanarity

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage

Figure 6 · PW 14-Pin TSSOP Package Dimensions

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