LX3302

Inductive Sensor Interface IC with Embedded MCU

Description

The LX3302 is a highly integrated programmable data conversion IC designed for interfacing to and managing of inductive sensors. The device includes an integrated oscillator circuit for driving the primary coil of an inductive sensor, along with two independent analog conversion paths for conditioning, converting, and processing of two analog signals from the secondary coils of the sensor. Each path includes an EMI filter, demodulator, anti-alias filter, programmable amplifier, and a 13-bit sigma-delta analog-to-digital converter.

Each analog signal path includes digital calibration capability which allows the complete analog path (including the external sensors) to be calibrated during the system manufacturing process. The calibration information is written to internal EEPROM resulting in improved production yields, and in-line system upgrades.

The LX3302 integrates a 32-bit RISC processor which provides programmable digital filtering and signal processing functions. The MCU resources include 12k bytes of program memory, 128 bytes of SRAM, and 64 bytes of user programmable EEPROM.

System interfaces include a SENT or PSI5 serial port, programmable PWM output and a 12-bit digital-to-analog converter analog buffed output.

The LX3302 is offered in a TSSOP14 package. The device is specified over a temperature range of -40°C to +150°C making it suitable for a wide range of commercial, industrial, medical, and/or automotive sensor applications.

Features

- Built-in Oscillator for Driving Primary Coil
- Two Independent Analog Channels With Demodulation
- 32-Bit RISC MCU with 3k 32-bit Words of ROM
- Two Programmable Gain Amplifiers
- Two Anti-alias Filters
- Two 13-bit ADCs
- Selection of SINC and SINC+FIR Digital Filters
- One 12-bit DAC
- One 16-bit PWM
- Output Ground Fault Detection and Protection
- Digital Calibration with Non-volatile Configuration Storage (EEPROM)
- Protected Watchdog Timer
- Low Temperature Drift
- Wide Range Supply Voltage(4.0V to 11.0V)
- -40°C to 150°C Operation
- Excellent Long Term Stability
- SENT Output
- Asynchronous PSI5 Output
- AEC-Q100 certification
- ISO 26262 Compliant

Applications

- Automotive Control
- ATE Equipment
- Industrial Process Control
- Smart Energy Saving Control

System Block Diagram

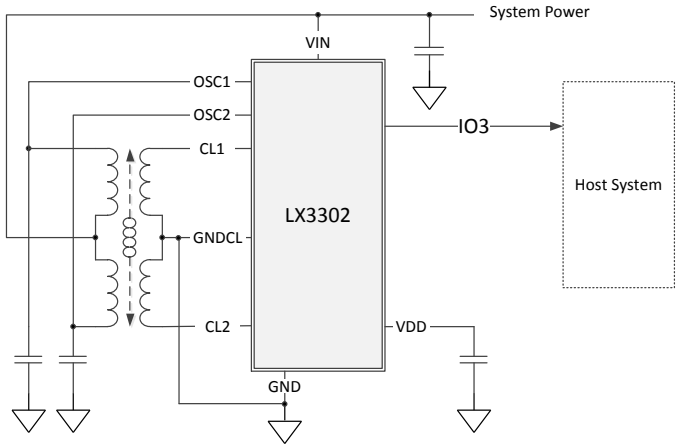


Figure 1 · System Block Diagram: LX3302

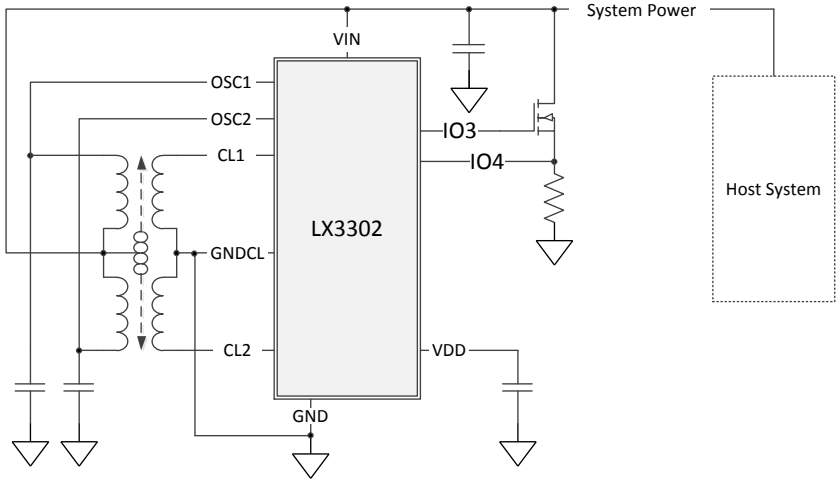


Figure 2 · System Block Diagram with PSI5 Output: LX3302

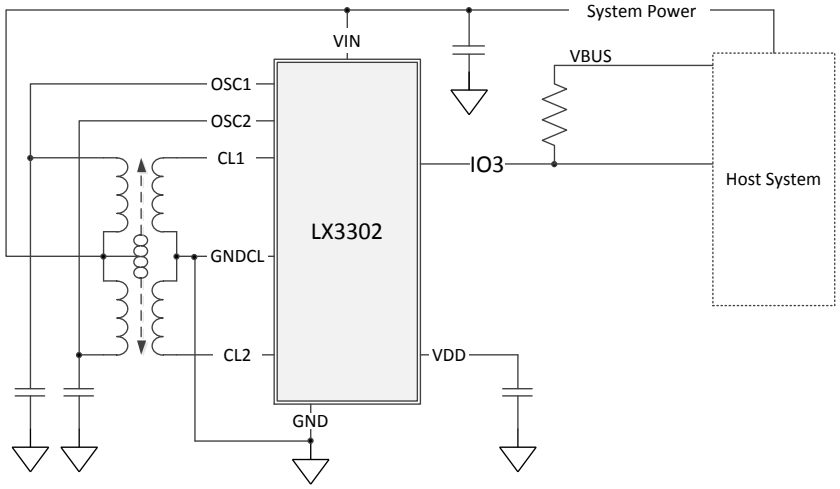


Figure 3 · System Block Diagram with Open Drain PWM Output: LX3302

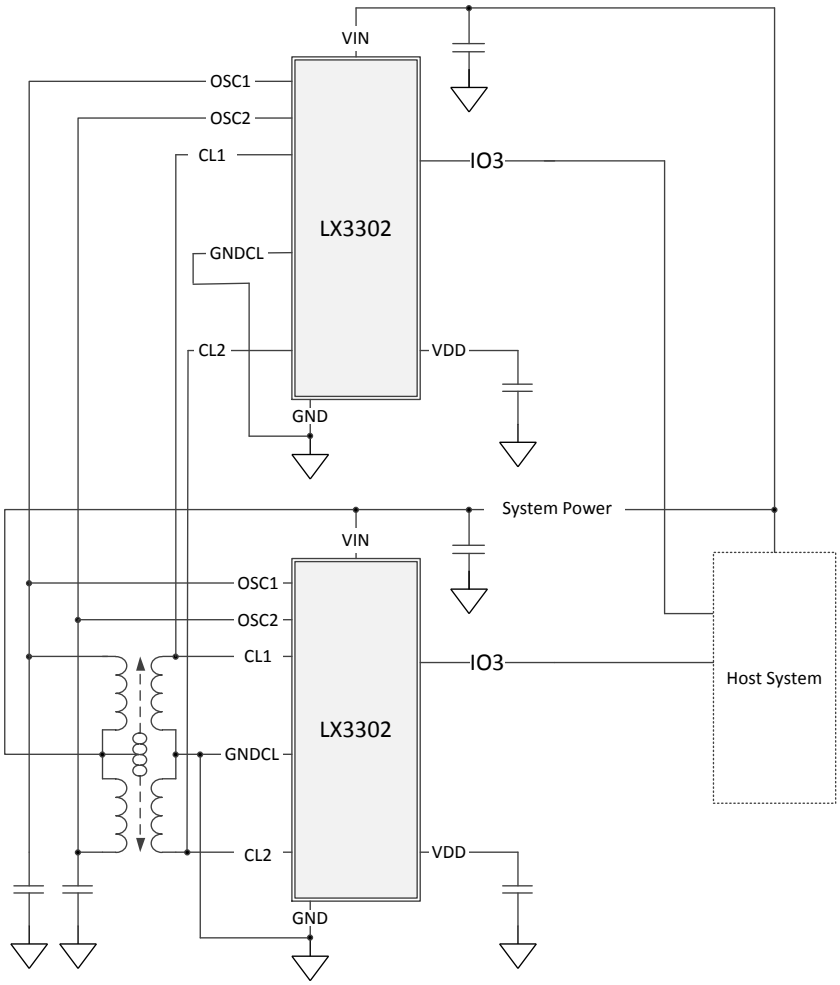


Figure 4 · System (Redundancy) Block Diagram: LX3302

Block Diagram

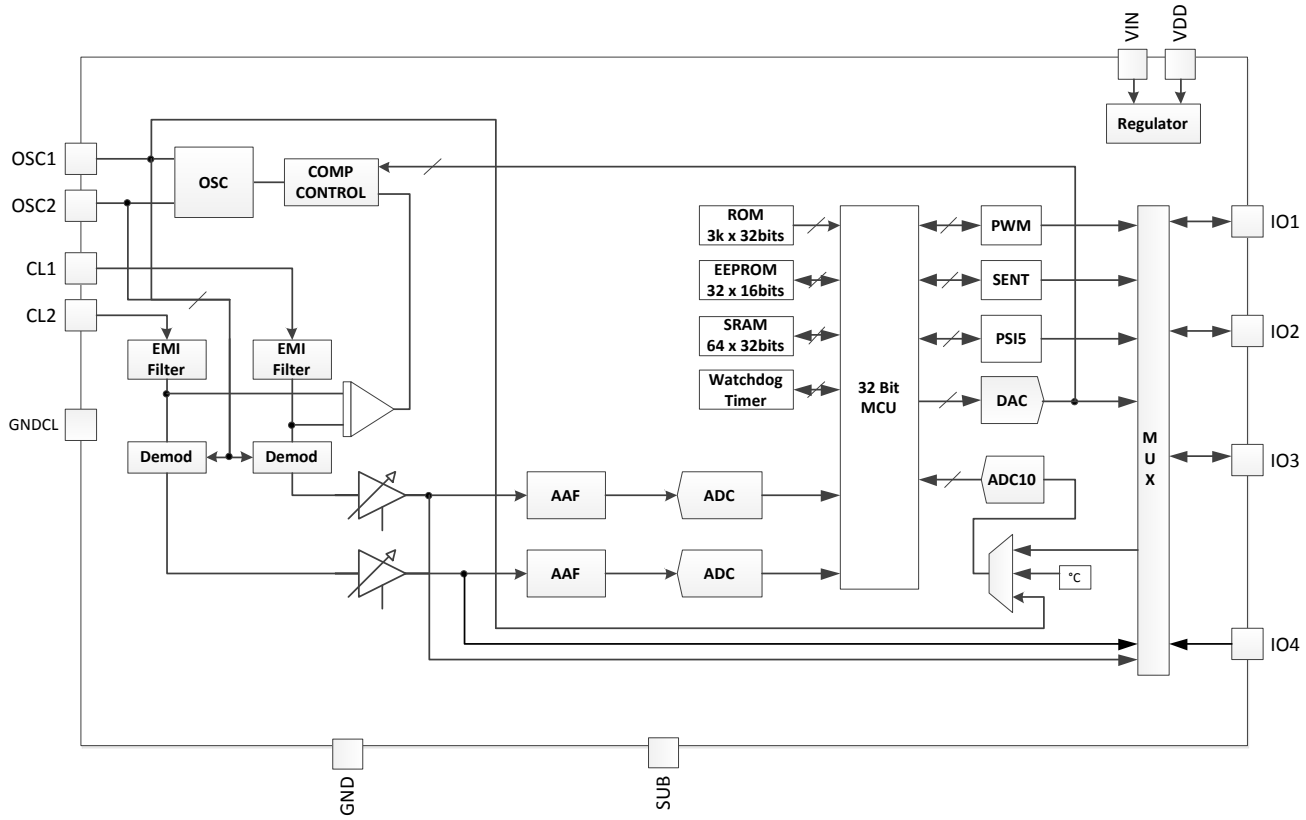
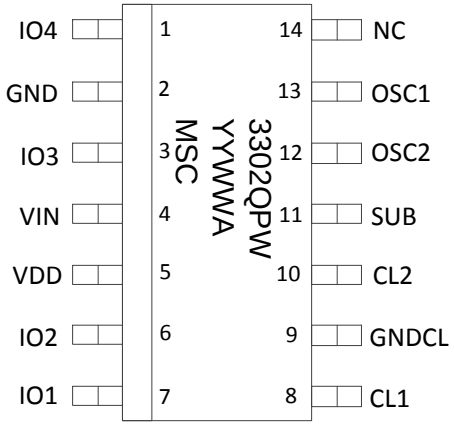


Figure 5 · LX3302 Block Diagram

Pin Configuration



14-Pin TSSOP

Figure 6 · Pinout (Top View)

Matte Tin Lead Finish / MSL 1

YYWWA = Year/ Week/Lot Code

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 150°C	RoHS2 compliant, Pb-free MSL1, AEC-Q100 Grade 0	14-TSSOP	LX3302QPW	Bulk / Tube
			LX3302QPW -TR	Tape and Reel

Pin Description

14-QSOP	Pin Designator	Description
1	IO4	IO pin4. General purpose analog/digital input for OSCDAC conversion, External FET current limit sensing, EEPROM retention test pin VS
2	GND	Ground
3	IO3	IO pin3. This pin can be programmed to provide DAC output, PWM output, reverse PWM output, SENT output, PSI5 external FET drive, µP digital output or general purpose digital input.
4	VIN	Power supply and internal EEPROM program pin. DC input power is applied to this pin for normal operation. Also used for EEPROM programming (refer to application information). Bypass this pin to GND pin with a low ESR capacitor not less than 100nF.
5	VDD	Regulator output. This is the output of the internal voltage regulator providing power to the analog and digital blocks. Bypass this pin to GND pin with a low ESR capacitor not less than 100nF. Less than 5mA load is allowed.
6	IO2	IO pin2. When configured as output: PGA1 or PGA2 analog output, digital push-pull output (PWM / PWMB / SENT / µP GPO), or open-drain output (PWM / PWMB / µP GPO). When configured as input: EEPROM retention test pin VCG, digital GPI or analog voltage for OSCDAC conversion.
7	IO1	IO pin1. When configured as output: PGA1 or PGA2 analog output, digital push-pull output (PWM / PWMB / SENT / µP GPO), or open-drain output (PWM / PWMB / µP GPO). When configured as input: digital GPI or analog voltage for OSCDAC conversion.
8	CL1	Sensor signal from secondary coil 1 of inductive sensor.
9	GNDCL	Reference ground for CL1 and CL2. Connect directly to GND on board, via a star connection.
10	CL2	Sensor signal from secondary coil 2 of inductive sensor.
11	SUB	Substrate; it is used ground failure protection. It should not be connected to GND, for normal application, leave this pin open
12	OSC2	LC oscillator pin: connects to the second side of the primary inductor coil. An external capacitor is connected between this pin and GND to as part of the LC oscillator tank circuit.
13	OSC1	LC oscillator pin: connects to the first side of the primary inductor coil. An external capacitor is connected between this pin and GND to as part of the LC oscillator tank circuit.
14	NC	Not used. Connect to GND

Thermal Data

Parameter	Value	Units
Thermal Resistance-Junction to Ambient, θ_{JA}	103.7	°C/W
Thermal Resistance-Junction to Case, θ_{JC}	40	°C/W

Note: Note: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51-7 (JEDEC) with thermal vias on VIN, IO3, GND pins.

Absolute Maximum Ratings

Parameter	Value	Units
Supply Input Voltage (VIN)	-7 to 20	V
Load Current on VDD	-1 to 15	mA
Voltage on OSC1, OSC2 and IO3	-0.3 to 20	V
Voltage on IO3	-0.3 to 17	V
Current on OSC1, OSC2 and IO3	-20 to 20	mA
Voltage on IO1 & IO2	-0.5 to 6.5	V
Current on IO1 & IO2	-10 to 10	mA
Voltage on IO4, VDD, CL1 and CL2	-0.5 to 3.6	V
Operating Humidity (non-condensing)	0 to 95	%
Operating Temperature	-40 to 150	°C
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering 10 seconds)	300	°C
Package Peak Temp. for Solder Reflow (40 seconds exposure)	260	°C
ESD, Human Body Model (HBM) AEC-Q100-002D	±2	kV
ESD, Charge Device Model (CDM) AEC-Q100-011 for IO1, IO4, CL1	±750	V
ESD, Charge Device Model (CDM) AEC-Q100-011 for mid pins	±500	V
ESD, Machine Model (MM) AEC-Q100-003	±200	V

Note: Stresses in excess of these absolute ratings may cause permanent damage. The device is not implied to be functional under these conditions. All voltages are with respect to GND. All voltages on ESD are with respected to SUB.

Recommended Operating Range

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage	VIN	For normal operating	4.0	5.0	6.0	V
EEPROM Program High	VIN_PH				18	V
Supply Current	IIN	For normal operating, excluding oscillator tail current			10	mA
Output Current	I_IO3_AN0	IO3=Analog mode, 0V	-15		-8	mA
Output Current	I_IO3_AN5	IO3=Analog mode, 0V	6		15	mA
Output Current	I_IO3_OD	IO3=OD mode, 0V			28	mA
Internal clock frequency	F_{OSC}		8.0	8.2	8.4	MHz
Operating Temperature	T_{OP}		-40		150	°C

Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Unless otherwise defined, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ 150°C, and the following test conditions: VIN = 5V, f=8.2MHz, IDD=1mA, II/O=0mA – Typical values are at 25 °C.						
Power						
VIN Input Voltage	VIN1	For normal operation, IO3=Analog	4.0	5.0	11	V
	VIN2	For normal operation, IO1,2,3=PWM	4.0	5.0	6	V
VIN Supply Current	IIN	For normal operating , excluding oscillator tail current ,IDD = 0mA, IO1,2,3,4 = 0mA, f = 8.2MHz		12.3	13	mA
VIN threshold Disabling of IO1&IO2 push-pull buffers	VIN_DIS_IO		6	6.4	7	V
VIN Hysteresis of VIN_DIS_IO	VIN_DIS_IOhys			0.25		V
VIN UVLO High Threshold	VIN_UVLO_HI	VIN POR Error enabled	3.7	3.8	3.9	V
VIN UVLO Hysteresis	VIN_ HYST			0.05		V
EEPROM Programming						
Programming mode Threshold	VIN_TH_EE	For EEPROM mode	11.5	12	12.5	V
Program Low	VIN_PL	For EEPROM programming mode	12.6	13	13.6	V
Program Idle	VIN_PI	For EEPROM programming mode	14.9	15.3	15.8	V
Program High	VIN_PH	For EEPROM programming mode	16.9	17.5	18.0	V
Duration time	td	Duration time each voltage state	20			µs
Rise time	tr	To enter EEPROM mode, VIN=15.3V, 10-90%			2.5	ms
VDD Reference Voltage						
Output Voltage	VDD	IDD = 5mA, after trimming	3.265	3.3	3.335	V
Output Current	IDD	Additional current sourced to external load(s)			5	mA
VDD POR threshold	VDD_POR	Monitor VDD, rising edge		2.9		V
VDD UVLO Hysteresis	VDD_Hyst	VDD UVLO Hysteresis		0.20		V
Short Current VDD to GND	IDD_SC_5V	Shorted to GND, VIN = 5V, 25°C		120		mA
Short Current VDD to GND	IDD_SC_6.5V	Shorted to GND, VIN = 6.5V, 25°C		160		mA
VDD Over Ripple Threshold	VDD_RIPPLE	Noise freq > 10MHz		300		mVpp
Oscillator OSC1 & OSC2						
Center Tap Voltage	VTAP	VIN=5V		5		V
Center Tap Voltage Offset From VIN	VTAP_OFFSET		-0.7	0		V
Center Tap Open Voltage Detection Threshold	VTAP_OPEN	VIN=5V		3.3		V
IO1,IO2, IO3 voltage from OSC1,OSC2 Pins	VTRANS	VIN=0V and OSC Pins Driven by External Signal,		0		V
OSC AC Swing Peak Over Voltage Detection	VOSC_OV	AC coupled	10			Vpp
OSC AC Swing Peak Under Voltage Detection	VOSC_UV	AC Coupled			3	Vpp
Total Tank DC Tail Current	ITK	VTAP = 5V	0		10	mA
Amplitude of OSC1&2	VOSC	VTAP = 5V	3		10	Vpp
Oscillation Frequency Range	FOSC_R	VTAP = 5V	1		6	MHz
Frequency Variation	FOSCTOL	VTAP = 5V	-5		5	%
Oscillator Inductance	LOSC	VTAP = 5V	3	6	12	µH

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Unless otherwise defined, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ 150°C, and the following test conditions: VIN = 5V, f=8.2MHz, IDD=1mA, II/O=0mA – Typical values are at 25 °C.						
Tank Circuit Quality Factor	QOSC	VTAP = 5V, (|X|/R)	10	22	30	
Harmonics	HOSC	VTAP = 5V, GBNT			2	%
Resistance Between OSC1&OSC2	ROSC1&2_HI	OSC1=1Vpp, OSC2=GND	500	1000		kΩ
Resistance Between OSC1&GND	ROSC1_GND	VIN=0V, OSC1 =5V, Measure Current from OSC1 to 5V	500	2000		kΩ
Resistance Between OSC2&GND	ROSC2_GND	VIN=0V, OSC2 =5V, Measure Current from OSC2 to 5V	500	2000		kΩ
Resistance Between OSC1&VDD	ROSC1_VDD		500	1000		kΩ
Resistance Between OSC2&VDD	ROSC2_VDD		500	1000		kΩ
Oscillator Tail Current Analog Close Loop Control Compensator						
Cross Frequency	Fc_OSC			6.5		kHz
DC gain	G_OSC			∞		
Oscillator Tail Current Digital Control OSCDAC						
OSCDAC resolution				12		Bit
OSCDAC allowable max tail current	Imax	Over process and temperature range			18	mA
Zero-code Error Current	Izero			25		µA
Step current	IStep	IOSCDAC/VALOSCDAC	6	6.9	7.8	µA
Current source temperature coefficient	TC_CS			660		ppm/°C
Settling Time	Ts_oscdac			0.5		µs
CL1 & CL2						
Peak to Peak Sensor Signal Range	VPP_CL	VTAP = 5V	80	100	120	mV
Error Signal for Open Circuit Detection Voltage	VOPEN		1			V
Source Coil Impedance	ZS	VIN =5 V, VTAP = 5V, VDD = 3.3V			100	Ω
EMI Filter 1 & 2						
Input Resistance of CL1&2	Rin_CL		1			MΩ
Input Capacitance of CL1&2	Cin_CL				5	pF
Cut-off Frequency	Fc_CL			13		MHz
Attenuation	ATT_CL	f=135MHz		-20		dB
Gain	G_CL	f=135kHz		0		dB
Demodulator and Programmable Gain Amplifier (PGA) 1 & 2						
Demodulator Frequency Range	FDem		1		6	MHz
PGA maximum bandwidth	PGABW		5			kHz
Absolute Gain Nonlinearity	AGN				0.15	%
Channel Gain Error Matching	CGEM	Match two inputs	-0.5		0.5	%
Demodulator Gain	DAA01			7		V/V
PGA Gain Range	PGA01		2.375	3.125	3.781	V/V
Gain Error	PGA02		-10		10	%
Total Gain Drift	GDrift	For all gain options		10	15	%
Zero Reference Voltage	V0_REF	VCL1=0 or VCL2=0, VDD=3.3V	1.642	1.65	1.658	V
Output Voltage Range	VO_PGA		0.65		2.65	V
Anti-Alias Filter 1 & 2						
Cut-off Frequency Range	AAF01	GBNT		24		kHz
Group Delay Time	AAF02	GBNT		13		µs
Attenuation	AAF03	f = 10*Cut-off Frequency		-60		dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Unless otherwise defined, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ 150°C, and the following test conditions: VIN = 5V, f=8.2MHz, IDD=1mA, II/O=0mA – Typical values are at 25 °C.						
Gain	AAF04	f = 0.1*Cut-off Frequency		0		dB
ADC1 & 2						
Resolution	ADC_Res			13		Bits
Absolute Offset Error	ADC_AOErr	GBNT			8	mV
Offset Error Temperature Drift	ADC_Tdoerr		-5		5	mV
Gain Error	ADC_GE	T=25°C		1.5	2	LSB
ADC Clock	ADC_clk		125		8200	kHz
Differential Nonlinearity	ADC_DNL	GBNT	-1		1	LSB
Integral Non-Linearity	ADC_INL	GBNT	-1		1	LSB
Channel Gain Matching	ADC_CGEM	Two ADCs	-1		1	LSB
Signal to Noise Ratio	ADC_SNR	At up to 1kHz BW and 2kHz data rate	86			dB
Signal to Noise ratio plus distortion	ADC_SNRD	At up to 1kHz BW and 2kHz data rate	75		86	dB
Latency of Sampling	ADC_LSmpl	Delay time for analog input to steady state			10	Cycle
Conversion Cycle	ADC_CC				1	Cycle
SINC or SINC+FIR Filter 1 &2						
Pass-band	FLTR_PB			1024		Cycle
Stop-band of SINC	SINC_SB			512		Cycle
Stop-band of SINC+FIR	SFIR_SB			732		Cycle
Output Data Rate	FLTR_ODR			512		Cycle
Digital Filter Group Delay of SINC	SINC_DFGD			256		Cycle
Digital Filter Group Delay of SINC+FIR	SFIR_DFGD			512		Cycle
Stop-band Attenuation	FLTR_SBA			1		%
Cross Talk Rejection	FLTR_CTR				-44	dB
PSRR	FLTR_PSRR	GBNT			-50	dB
OSCDAC						
Maximum resolution	OSCDAC_MR			10		Bit
Full scale voltage range	OSCDAC_FS	Reference is VDD		3.3		V
Differential Nonlinearity	OSCDAC_DNL	GBNT	-1.5		1.5	LSB
Integral Non-Linearity	OSCDAC_INL	GBNT	2		2	LSB
Signal to Noise Ratio	OSCDAC_SNR	GBNT		62		dB
Effective number of the bits	OSCDAC_ENB	GBNT		10		Bit
OSCDAC Clock	OSCDAC_CLK	Main Oscillator f=8.2MHz (Divider=8)		1.025		MHz
Conversion Cycle	OSCDAC_CC				12	Cycle
Temperature Sensor						
Temperature Range	TSR		-40		175	°C
Absolute Accuracy	TSAAcc			1.5	3	°C
Room Temperature Sensor Voltage	TSRTV			1.538		V
Temperature Coefficient	TSTC1	-40°C <T<175°C		5.52		mV/°C
	TSTC2	-40°C <T<175°C		1.714		LSB/°C
Digital to Analog Converter (DAC)						

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Unless otherwise defined, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ 150°C, and the following test conditions: VIN = 5V, f=8.2MHz, IDD=1mA, II/O=0mA – Typical values are at 25 °C.						
DAC resolution	DACR			12		Bit
DAC Reference Voltage, VIN	DACVREF			VIN/2.75		V
Relative Accuracy	DACRAcc		-0.25		0.25	%
Zero-code Error	DACZCErr				5	mV
Temperature Drift	DACTD				10	ppm/°C
Settling Time	DACST				10	µs
Slew Rate	DACSLRate		0.1			V/µs
IO1, IO2 Analog output						
Voltage Gain	G12_VDD	VREF=VDD/2		1		V/V
Voltage Gain	G12_VIN	VREF=VIN/2		1.5		V/V
Low Level Output Voltage	VOLA	Pull-up load ≥10 kΩ to VIN	0		0.3	V
High Level Output Voltage	VOHA	Pull-down load ≥10 kΩ to GND, Gain= VIN/VDD	VIN – 0.3		VIN	V
Output rising slew rate	SRATE_R12A	COUT=1nF		0.45		V/µs
Output falling slew rate	SRATE_F12A	COUT=1nF		0.45		V/µs
Output short circuit current	ISHORT_12A	Short to 0 or short to 5V	10		20	mA
IO1, IO2 Digital output						
Low Level Output Voltage	VOLD	Pull-up load ≥10 kΩ to VIN			3	% VIN
High Level Output Voltage	VOHD	Pull-down load ≥10 kΩ to GND	97			% VIN
Propagation Delay Time	PDT_12D			0.4	0.7	µs
Output rising slew rate	SRATE_R12D	COUT=1nF, OD_PWM, Pull Up to VIN=10kΩ		0.182		V/µs
Output falling slew rate	SRATE_F12D	COUT=1nF, OD_PWM		6		V/µs
Output short circuit current	ISHORT_12D	Short to 0 or short to 5V	10		20	mA
IO1, IO2 Digital input						
High level Input Voltage	VIHD		2.5			V
Low level Input Voltage	VILD				0.8	V
Input Impedance	RIN_12		200			kΩ
Input Capacitance	CIN_12				5	pF
IO3 Analog output						
Voltage Gain	G_3			2.75		V/V
Output Load	RL_3		0.9	10		kΩ
Propagation Delay Time	IO3_PDT				50	µs
Buffer input offset	IO3_offset				10	mV
Output short circuit current	SHORT1_3A	Short to GND or short to VIN		12	15	mA
Output short circuit current	SHORT2_3A	Short to14V			45	mA
Output slew rate	SLrate_3A	COUT=100nF		0.1		V/µs
VIN Ratiometric Error	RaErr_3A	Over full VIN voltage range	-0.2	0	0.2	% VIN
Thermal Drift	TD_ 3A	Clamped output(isolated DAC &buffer)	-0.3	0	0.3	% VIN
IO3 Digital output						

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Unless otherwise defined, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ 150°C, and the following test conditions: VIN = 5V, f=8.2MHz, IDD=1mA, II/O=0mA – Typical values are at 25 °C.						
High level Output Voltage	VOH_3	Pull-up load ≥10 kΩ to VIN			2	% VIN
Low level Output Voltage	VOL_3	Pull-down load ≥10 kΩ to GND	98			% VIN
Propagation Delay Time	PDT_3D				0.1	µs
Output rising slew rate	Srate_R3D	COUT=2.2nF, OD_PWM, Pull-up 10KΩ to VIN		0.07		V/µs
Output falling slew rate	Srate_F3D	COUT=2.2nF, OD_PWM		5.75		V/µs
Output rising/falling slew rate @PWM	Srate_3D	COUT=2.2nF, PWM, Pull-up 10KΩ to VIN		5.7		V/µs
Output short circuit current	IO3_SHORTD	Short to 0V or short to 5V		25	30	mA
IO3 Input						
High level Input Voltage	VIH_3IN	Pull-up load ≥10 kΩ to VIN	2.5			V
Low level Input Voltage	VIL_3IN	Pull-down load ≥10 kΩ to GND			0.8	V
Input Impedance	RIN_3		90			kΩ
Input Capacitance	CIN_3				5	pF
Output short circuit current	IO3_SHORTD	Short to 0V or short to 5V		25	30	mA
IO4 Digital input						
High level Input Voltage	VIH_4	Pull-up load ≥10 kΩ to VIN	2.5			V
Low level Input Voltage	VIL_4	Pull-down load ≥10 kΩ to GND			0.8	V
Input Impedance	RIN_4		450			kΩ
Input Capacitance	CIN_4				5	pF
IO1, IO2, IO3 FAULT OUTPUT (where x=1,2,3)						
Ground Off Output low Level	VOL_IOxGF1	Broken GND, RL_IOx=10kΩ to GND			4	%VIN
Ground Off Output low Level	VOL_IOxGF2	Broken GND & RL=1kΩ to GND, With RL=1kΩ VIN and GDC			4	%VIN
Ground Off Output High Level	VOH_IOxGF1	Broken GND, RL_IOx=1kΩ to VIN	99	100		%VIN
VIN Open output Low Level	VOL_IOx_IN	Broken VIN, RL_IOx=1kΩ to GND		0	1	%VIN
VIN Open output High Level	VOH_IO3_VIN1	Broken VIN, RL_IO3≥3kΩ to VIN	97	99		%VIN
VIN Open output High Level	VOH_IO3_VIN2	Broken VIN & Pull-up load to VIN, 1kΩ≤RL≤3 kΩ With 3KΩ VIN and GDC	97	99		%VIN
FAULT Output Low Level	VIO3_FL10K	RL_IO3=10kΩ to VIN			1	%VIN
FAULT Output Low Level	VIO3_FL1K	RL_IO3=1kΩ to VIN			1.5	%VIN
Main Oscillator						
Main Oscillator Frequency	FCLK			8.2		MHz
Tolerance	FCLK_TOL	TA=25°C	-1.5		1.5	%
Absolute Temperature Drift	FCLK_TD		-6		6	%
Window Watchdog Timer with Key Protection						

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Unless otherwise defined, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ 150°C, and the following test conditions: VIN = 5V, f=8.2MHz, IDD=1mA, II/O=0mA – Typical values are at 25 °C.						
Clock	WD_CLK			8.2		MHz
Window_LO Counter	WD_WLO			10		bit
Resolution	WD_WLOR			4		µs
Window_HI Counter	WD_WHI			21		bit
Resolution	WD_WHIR			3.9		µs
Processor Resources						
Data bus	PR_DBUS			32		bit
Instruction size	PR_INSS			32		bit
ROM Size	PR_ROMS	32-bit words		3072		words
SRAM Size	PR_SRMS	Application data, Stack, Heap, 32-bit words		64		words
EEPROM Size	PR_EEPRMS	16-bit words		32		words
Number of EEPROM Erase/Write Cycles	PR_NEEWC1	TA=25°C, GBNT	100000			Cyc
Number of EEPROM Erase/Write Cycles	PR_NEEWC2	TA=125°C, GBNT	10000			Cyc
Max temperature for erase / write EEPROM	PR_TmaxEW			125		°C
EEPROM data Retention	PR_DataR1	TA=85°C	10			Years
EEPROM data Retention	PR_DataR2	TA=125°C	1			Years
EEPROM data Retention	PR_DataR3	TA=150°C	0.3			Years
PWM Controller						
Clock Pre-scale Bit	PWM_CPSB	Divider=1,2,4,8		2		bit
PWM Clock	PWM_CLK			8.2		MHz
Period	PWM_PER			16		bit
Duty	PWM_Duty			16		bit
PWM Jitter	PWM_Jitter	No Clamped Output		0.2		%D
SENT (Single Edge Nibble Transmission) Interface and Driver						
Low state Voltage	SENTVOL	IL= 5 mA			0.5	V
High state Voltage	SENTVOH	IL= 5 mA, VIN=5V	4.1			V
Average current consumption	SENTIS	Average current consumption from Receiver supply over one message			15	mA
Supply current ripple	SENTISCR	Peak to peak variation			9	mApp
Square wave Rising time	SENTTR	From 1.1 V to 3.8V. Load= 5 mA, Cout=1nF, TCT=3µs		0.3*	TBD	µs
Square wave Falling time	SENTTF	From 3.8 V to 1.1V. Load= 5 mA, Cout=1nF, TCT=3µs		0.3*	TBD	µs
Edge to edge jitter with static environment for any pulse period	SENTJIT	For 3µs nominal clock tick including clock accuracy. For higher clock tick times need to be increased proportionally			0.1*	µs
Nominal clock period(Tick)	SENTtick	By 2 program bits	3.0		24.0	µs
Clock Accuracy	SENTCLKAC		-10		+10	%
Clock jitter and drift error	SENTCLKJIT	variation of maximum nibble time compared to the expected time derived from the calibration pulse time at a 3 µs clock tick			0.05*	µs
* For 3µs nominal clock tick including clock accuracy. For higher clock tick times need to be increased proportionally						

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Unless otherwise defined, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ 150°C, and the following test conditions: VIN = 5V, f=8.2MHz, IDD=1mA, II/O=0mA – Typical values are at 25 °C.						
PSI5 (Asynchronous Mode Only)						
Absolute Bit Time Range	ATBitR1	125kbps	7.6	8.0	8.4	µs
	ATBitR2	189kbps	5.0	5.3	5.6	µs
Absolute Gap time	ATGAP1	125kbps, TGAP> TBit	8.4			µs
	ATGAP2	189kbps, TGAP> TBit	5.6			µs
Current Regulation Ref.	VREF	For PSI5 operation	390	412.5	435	mV
Fall/Rise Time Driver Voltage Slope	PSI5_Tr_Tf	20% to 80%, RL=12.5Ω, CL=100nF, L=0µH	0.33		1	µs
Total Overshoot Time Per Cycle	PSI5_TOTPC	Voltage Over 10%, RL=2.5Ω, CL=47nF, L=8.7µH			0.52	µs
Total Undershoot Time Per Cycle	PSI5_TUTPC	Voltage Under 10%, RL=2.5Ω, CL=47nF, L=8.7µH			0.52	µs
Overshoot Voltage	PSI5_OV	RL=2.5Ω, CL=47nF, L=8.7µH			10	%
Undershoot Voltage	PSI5_UV	RL=2.5Ω, CL=47nF, L=8.7µH	-10			%

Configuration EEPROM

The LX3302 integrates a 32 Words X 16bits (512bits), user programmable EEPROM for storing calibration and configuration parameters. The calibration parameters enable the production sensor assembly to be customer-factory calibrated assuring consistent unit to unit performance. The following Figure.7 shows LX3302 EEPROM configuration map and table 1 itemizes the LX3302 configuration EEPROM contents:

Name	Description	Size (bit)	Word & Bits (MSB:LSB)	Sign	Min Value	Max Value	Step	Default From MSC
ID	Customer Part ID	18	W0[15:0]W1[15:14]	No	0	3FFFF	1	
Reserved		1	W1[13:]					
Reserved		2	W1[12:11]					
GADJ	PGA Gain	4	W1[10:7]	Yes	1000b	0111b	1	0
IOSC	Oscillator tail current	2	W1[6:5]	No	0	3	1	0
TEST1	Reserved	1	W1[4]	No				0
OSCDIS	Oscillator Disable	1	W1[3]	No				0
REFRESH	ADC Clock & PWM Clock	3	W1[2:0]	No	1	7	1	0
FILTER	Select Digital Filter	1	W2[15]	No				0
CLSEL	Select CL1& CL2	1	W2[14]					0
GMTCH	Channel gain mismatch correction	7	W2[13:7]	Yes	-12.1%	12.1%	0.39%	0
DCOS	Cosine channel dynamic offset correction	10	W2[6:0]W3[15:13]	Yes	-511	511	1	0
SCOS	Cosine channel offset correction	10	W3[12:3]	Yes	-511	511	1	0
DSIN	Sine channel dynamic offset correction	10	W3[2:0]W4[15:9]	Yes	-511	511	1	0
SSIN	Sine channel offset correction	10	W4[8:0]W5[15]	Yes	-511	511	1	0
OSCOMP	Max Oscillator swing	10	W5[14:5]	No	0	255	1	
DEBUG	Debugging data	5	W5[4:0]					
ORIGIN	Origin	12	W6[15:4]	No	0	4095	1	0
HCLMP	High Clamp	12	W6[3:0]W7[15:8]	No	0	4095	1	0
LCLMP	Low Clamp	12	W7[7:0]W8[15:12]	No	0	4095	1	0
S0	Initial slope	12	W8[11:0]	No	0	4095	1	TBD
X1	Linearization point 1 x-coordinate	12	W9[15:4]	No	0	4095	1	TBD
X2	Linearization point 2 x-coordinate	12	W9[3:0]W10[15:8]	No	0	4095	1	TBD
X3	Linearization point 3 x-coordinate	12	W10[7:0]W11[15:12]	No	0	4095	1	TBD
X4	Linearization point 4 x-coordinate	12	W11[11:0]	No	0	4095	1	TBD
X5	Linearization point 5 x-coordinate	12	W12[15:4]	No	0	4095	1	TBD
X6	Linearization point 6 x-coordinate	12	W12[3:0]W13[15:8]	No	0	4095	1	TBD
X7	Linearization point 7 x-coordinate	12	W13[7:0]W14[15:12]	No	0	4095	1	TBD
Y1	Linearization point 1 y-coordinate	12	W14[11:0]	No	0	4095	1	TBD
Y2	Linearization point 2 y-coordinate	12	W15[15:4]	No	0	4095	1	TBD
Y3	Linearization point 3 y-coordinate	12	W15[3:0]W16[15:8]	No	0	4095	1	TBD

Y4	Linearization point 4 y-coordinate	12	W16[7:0]W17[15:12]	No	0	4095	1	TBD
Y5	Linearization point 5 y-coordinate	12	W17[11:0]	No	0	4095	1	TBD
Y6	Linearization point 6 y-coordinate	12	W18[15:4]	No	0	4095	1	TBD
Y7	Linearization point 7 y-coordinate	12	W18[3:0]W19[15:8]	No	0	4095	1	TBD
S7	Final slope	12	W19[7:0]W20[15:12]	No	0	4095	1	TBD
TD	Threshold Detect	13	W20[11:0]W21[15]	No	0	8192	1	0
TDPOL	TD output logic Polarity	1	W21[14]	No				
DIAGMK	Diagnostic error Mask	12	W21[13:2]	No	0			
SENTCLKT	SENT Clock Tick	2	W21[1:0]	No				
SENTFCM	SENT Protocol Select	4	W22[15:12]	No				
SENTREFR	SENT Constant clock ticks sync with Pause Pulse	11	W22[11:1]	No				
SENTPPE	SENT Pause Pulse	1	W22[0]	No				
SENTSCM	SENT Serial Message	2	W23[15:14]	No				
MSGMUX	Message Mux	1	W23[13]	No				
DIAGPOL	Diagnostic Polarity	1	W23[12]	No				
PSI5FR	PSI5 Frame	3	W23[11:9]	No				
PSI5STS	PSI5 Status	2	W23[8:7]	No				
PSI5SMSG	PSI Serial Message	2	W23[6:5]	No				
PSI5ERRCS	PSI5 Error Check Selection	1	W23[4]	No				
PSI5DRB	PSI5 Data Region B	4	W23[3:0]	No				
PSI5DRA	PSI5 Data Region A	4	W24[15:12]	No				
PSI5REFR	PSI5 Refresh Rate	11	W24[11:1]	No				
PSI5BR	PSI5 Bit Time Rate	1	W24[0]	No				
IOSEL	Input/Output selection	15	W25[15:1]	No				
OSCDFB	OSCDAC Feedback	1	W25[0]	No				
OSCDAC	Oscillator DAC Data	12	W26[15:4]	No				
TDMASK	TD input source Select	2	W26[3:2]	No				
EELOCK	Control EEPROM Write	2	W26[1:0]	No				
MESSAGE	Message	16	W27[15:0]	No				
MSGID	Message ID	8	W28[15:8]	No				
TDHYST	Threshold Detect hysteresis	8	W28[7:0]	No	0	255	1	0
TEST2	Reserved	1	W29[15]	No				
CLCHK	RANGE Check	1	W29[14]					
WDSCALE	WD_SCALE	3	W29[13:11]					
TESTMOD	TST_MOD	9	W29[10:2]					
RSVD	RSVD	2	W29[1:0]					
RSVD	Reserved	16	W30[15:0]	No				
RSVD	Reserved	16	W31[15:0]	No				

Table 1 - LX3302 Configuration EEPROM

	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
WORD0	ID{17..02															
WORD1	ID[1..0]		Reserved			GADJ				OTC		CHOP	OSCDIS	REFRESH		
WORD2	FILTER	CLSEL		GC[6..0]						OCS[9..3]						
WORD3	OCS[2..0]				OCC[9..0]									OSS[9..7		
WORD4	OSS[6..0]							OSC[9..1								
WORD5	OSC[0]	IMAX[9..0]										DEBUG				
WORD6	ORIGIN[11..0]												HP[11..8			
WORD7	HP[7..0]								LP[11..4							
WORD8	LP[3..0]				S0[11..0]											
WORD9	X1[11..0]												X2[11..8			
WORD10	X2[7..0]								X3[11..4							
WORD11	X3[3..0]				X4[11..0]											
WORD12	X5[11..0]												X6[11..8			
WORD13	X6[7..0]								X7[11..4]							
WORD14	X7[3..0]				Y1[11..0]											
WORD15	Y2[11..0]												Y3[11..8			
WORD16	Y3[7..0]									Y4[11:4						
WORD17	Y4[3..0]				Y5[11..0]											
WORD18	Y6[11:0]												Y7[11..8			
WORD19	Y7[7..0]									S7[11..4						
WORD20	S7[3..0]				TD[12..1]											
WORD21	TD[0]	TD LEVEL		DIAGMASK[11..0]											SENT CLKT	
WORD22	SENT PROTOCOL SEL[3..0]				SENT CONSTCLKT[10:0]											SENT PausePLS
WORD23	SENT SERIALMSG [1..0]		MSGMUX	DIAGLVL	PSI5 FRAME[2..0]			PSI5 STATUS[1..0]		PSI5 SER MSG[1..0]		PSI5 ECSEL	PSI5DATAREGB			
WORD24	PSI5 DATA REG A				PSI5REFRESH [10..0]											PSI5 Bittime
WORD25	OUTPUTCONFIG[14..0]															OSCFB
WORD26	DAC[11..0]												TDMASK		EELOCK	
WORD27	MESSAGE[15..0]															
WORD28	MESSAGE_ID [7..0]								TD_HYST [7..0]							
WORD29	RESERVED															
WORD30	TEMPCAL[9..0]										RSVD					
WORD31	RSVD															

Figure 7 · LX3302 Configuration EEPROM MAP

- **ID** (18bits, W0[15:0]W1[15:14])

  This is ID field. The Customer Part ID is a 18-bit field containing customer part identification information.

- **GADJ** (4bits,W1[10:7])

  This parameter is used to adjust the gain of Programmable Gain Amplifier (PGA). The bit W1[10] is polarity bit, rest three bits(9:7) adjust gains. Default gain [00000b] is 3.125. Each step changes approximately 3% gain. Smallest number is 1000, largest number is 0111.

- **IOSC** (2bits,W1[6:5])

  These two bits set the Oscillator Tail Current value.

IOSC Bits	Tail Current	Feedback
00	Normal mode	Enabled
01	1/2	Enabled
10	1/4	Enabled
11	1/8	Enabled

Table 2 - IOSC Configuration

- **TEST1** (1 bit, W1[4])

  Reserved

- **OSCDIS** (1bit, W1[3])

  This bit set enable or disable the oscillator over voltage detection. If the bit is set to 1, it disables OSC operation when the OSC1 peak value is exceeding 9.5Vpk. If the bit is set to 0, it allows to operate OSC1 & OSC2.

- **REFRESH** (3bits, W1[2:0])

  This parameter sets the value of the refresh rate of ADC update. If the PWM output is selected the PWM frequency is always equal to the ADC update rate.

Bit Value	ADC1 & ADC2 Sampling Clock	PWM Frequency
000	FMCLK	
001	FMCLK/2	
010	FMCLK/4	
011	FMCLK/8	
100	FMCLK/16	
101	FMCLK/32	
110	FMCLK/64	
111	FMCLK/64	

Table 3 - REFRESH Bits Configuration

- **FILTER** (1bit, W2[15])

  This bit selects the digital filter type. If the bit =0, then SINC and if the bit =1 then SINC+FIR

Filter Bit	Filter Type
0	SINC
1	SINC+FIR

Table 4 - FILTER Configuration

- **CLSEL** (1bit, W2[14])

  When the CLSEL is set to 1, it swaps the Sine and Cosine input (CL1 & CL2).

- **GMTCH** (7bits, W2[13:7])

  Value of the input channel gain mismatch correction gain used in inputs correction calculation.

- **DCOS** (10bits, W2[6:0]W3[15:13])

  Dynamic Offset Correction of CL1 input channel used in inputs correction calculation.

- **SCOS** (10bits, W3[12:3])

  Offset Correction of CL1 input channel used in inputs correction calculation.

- **DSIN** (10bits,W3[2:0]W4[15:9])

  Offset Correction of CL2 input channel used in inputs correction calculation.

- **SSIN** (10bits, W4[8:0]W5[15])

  Dynamic Offset Correction of CL2 input channel used in inputs correction calculation.

- **OSCOMP** (10 bits, W5[14:5])

  Maximum amplitude of the oscillator swing used in the inputs correction calculation. The maximum value of the OSCOMP is 1023, step 1. Multiplied by 2 to convert as internal OSCOMP data.

- **DEBUG** (5bits, W5[4:0])

  This parameter sets to enable internal data reading for debugging purpose.

Bit Value	Parameter	Remarks
00000	Disable	
00001	ADC1	
00010	ADC2	
00011	Reserved	
00100	SIN(ADJ)	
00101	COS(ADJ)	
00110	Theta	Calculated angle
00111	OSCDAC	
01000	Temperature	
01001-11111	Reserved	

Table 5 - DEBUG Bits Configuration

- **ORIGIN** (12bits, W6[15:4])

  Offset value of the system origin relative to fore-and-after position. This is not a DC output offset adjustment. Verify LCLMP and HCLMP parameters are not limiting the output range.

- **HCLMP** (12bits, W6[3:0]W7[15:8])

  This parameter is set to high plateau level of output. Output will be clamped at this value if output swing can go above this level. It reduces the maximum output swing. Full scale swing is achieved with HCLMP = 4095.

- **LCLMP** (12bits, W7[7:0]W8[15:12])

  This parameter sets the low plateau level of output. The output is clamped at this level if output swing can go below this level. The LCLMP value raises the minimum output value from zero. An output value of “zero” is achieved with LCLMP = 0. LCLMP setting value will overrides the HCLMP setting if both setting are crossed over.

- **S0** (12bits, W8[11:0])

  Slope of first linearization segment.

- **Xn and Yn (n=1 to 7)** (12bits each, Refer to EEPROM Map)

  Value of the X and Y coordinates for the “n” th linearization point.

- **S7** (12bits, W19[7:0]W20[15:12])

  Slope of the last linearization segment.

- **TD** (13bits, W20[11:0]W21[15])

  This parameter sets the Threshold Detection(TD) level. The output(s) programed as TD output is toggled the level depends on the TDPOL and TDHYST parameters. TD HYST parameter is set to the hysteresis value (TD-TDHYST).

- **TDHYST** (8bits, W28[7:0])

  TDHYST is used to set the hysteresis value of TD when output drops.

- **TDPOL** (1bit, W21[14])

  This bit selects TD output active low or high. If the bit is set to 0, then when the data is lower than TD, then output is set to high, and if the bit is set to 1, then when the data is higher than TD, then programmed as TD output(s) is set to high

Bit Value	Condition	Output
0	Data < TD	High
0	Data > TD	Low
1	Data < TD	Low
1	Data > TD	High

Table 6 – TDPOL Bit operation

- **DIAGMK** (12bits, W21[13:2])

  This parameter sets to enable to detect the fault when the bit is set to 1. When the bit is set to 0, it masks off the result.

Bit #	Diagnostic Mask	Remarks
0	TD	
1	Flow Check, EEPROM Error, MCU integrity check, ROM checksum, peripheral test, RAM test	
2	Reserved	
3	ADC1, ADC2 signal too low	
4	ADC1, ADC signal too high	
5	Reserved	
6	VIN POR error	Default=1
7	VDD Fail	
8	CL1, CL2 open	
9	OSC1, OSC2 open	
10	OSC1 over voltage	
11	OSC1 under voltage	

Table 7 – DIAGMK Bits configuration

- **SENTCLK** (2bits, W21[1:0])

  This parameter sets SENT clock tick time period.

Bits Value	Tick Clock	Remarks
00	3µs	
01	6µs	
10	12µs	
11	24µs	

Table 8 – SENTCLK Bits configuration

- **SENTFCM**(4bits, W22[15:12])

  This parameter sets SENT clock tick time period.

Bits Value	Protocol	Remarks
0000	Standard SENT	
0001	A1-individual sensor with feature that error sets data nibble	
0011	A1-individual sensor without feature that error sets data nibble	
1000	A3 or A4 with counter and invert copy of Data nibble 1 at data nibble 6	
1001	A4 with counter and “0” at Data nibble 6	

1010	A4 with no counter and invert copy of Data nibble 1 at data nibble 6	
1011	A4 with no counter “0” at Data nibble 6	
1100	A3 with counter and data nibble 6 as is 15- n1; slow channel send out ram_DIAG	

Table 9 – SENTFCM Selection Bits configuration

- **SENTREFR** (11bits, W22[11:1]) **,** **SENTPPE** (1bits, W22[0])

  SENTREFR and SENTPPE parameters are SENT Constant clock ticks sync with Pause Pulse. W22[0] is used to set Pause Pulse. If the bit is set to 0, it disables SENT Pause Pulse. If the bit is set to 1, SENT Pause pulse is enabled. SENT message is synced with a selectable constant period of clock ticks. SENT message syncs with selectable length based on clock ticks, is defined in 11bits on SENTREFR.

  Bit[10:0] is set the number of clock ticks. All 0s set 0 clock ticks, and all 1s set 2023 clock ticks.

  Valid SENT message without pause pulse is from 154 to 270 clock ticks. Pause pulse is extra 12 to 768 clock ticks. If pause pulse is enabled, a valid SENT message is from 166 to 1038 clock ticks. Hardware compensates the SENT message with pause pulse.

- **SENTSCM**(2bits, W23[15:14])

  This parameters are SENT Serial Message.

Bits Value	Configuration	Remarks
00	Serial Message is OFF	
01	Serial Message is ON, with short format	
10	Serial Message is ON, with enhanced format, 12 bit data + 8 bit ID	
11	Serial Message is ON, with enhanced format, 16 bit data + 4 bit ID	

Table 10 – SENTSCM Bits configuration

- **MSGMUX**(1bit, W23[13])

  If the bit is set to 0, then no action, or set this bit to 1 if PSI5 and SENT serial channel message is enabled,

- **DIAGPOL** (1bit, W23[12])

  This bit sets the fault mode output level.

  0: Fault mode outputs logic low

  1: Fault mode outputs logic high

- **PSI5FR**(3bits, W23[11:9])

  This parameter sets PSI5 Frame.

Bit Value	Frame	Remarks
000	Disable PSI5 Frame	
001	Enable PSI5 Frame and set size of 1	
010	Enable PSI5 Frame and set size of 2	
011	Enable PSI5 Frame and set size of 3	
100	Enable PSI5 Frame and set size of 4	
101	Reserved	
110	Reserved	
111	Reserved	

Table 11 – PSI5FR Bits Configuration

- **PSI5STS** (2bits, W23[8:7])

  This parameter sets PSI5 status.

Bit Value	Status	Remarks
00	Disable PSI5 Status	
01	Enable PSI5 Status and set size of 1	
10	Enable PSI5 Status and set size of 2	
11	Reserved	

Table 12 – PSI5STS Bits Configuration

- **PSI5SMSG**(2bits, W23[6:5])

This parameter is PSI5 Serial Message.

Bits Value	Configuration	Remarks
00	Serial Message is OFF	
01	Serial Message is ON, Size of 2	
10	Serial Message format, 12 bit data + 8 bit ID	
11	Serial Message format, 16 bit data + 4 bit ID	

Table 13 – PSI5SMSG Bits configuration

- **PSI5ERRCS**(1bits, W23[4])

This parameter is PSI5 Error Check Selection bit.

Bits Value	Error check	Remarks
0	3-bit CRC	
1	1 bit parity	

Table 14 – PSI5ERRCDS selection

- **PSI5DRB**(4bits, W24[3:0])

This parameter is set the DATA Region B as below table;

Bit Value	Description	Remarks
0000	Disable PSI5 data region B	
0001	Enable PSI5 data region B and set the size to 1 bit	
0010	Enable PSI5 data region B and set the size to 2 bit	
0011	Enable PSI5 data region B and set the size to 3 bit	
0100	Enable PSI5 data region B and set the size to 4 bit	
0101	Enable PSI5 data region B and set the size to 5 bit	
0110	Enable PSI5 data region B and set the size to 6 bit	
0111	Enable PSI5 data region B and set the size to 7 bit	
1000	Enable PSI5 data region B and set the size to 8 bit	
1001	Enable PSI5 data region B and set the size to 9 bit	
1010	Enable PSI5 data region B and set the size to 10 bit	
1011	Enable PSI5 data region B and set the size to 11 bit	
1100	Enable PSI5 data region B and set the size to 12 bit	
1101	Reserved	
1110	Reserved	
1111	Reserved	

Table 15 – PSI5DRB bits configuration

- **PSI5DRA**(4bits, W24[15:12])

This parameter is set the DATA Region A as below table;

Bit Value	Description	Remarks
0000	PSI5 data region A size of 10 bits	
0001	PSI5 data region A size of 11 bits	
0010	PSI5 data region A size of 12 bits	
0011	PSI5 data region A size of 13 bits	
0100	PSI5 data region A size of 14 bits	
0101	PSI5 data region A size of 15 bits	
0110	PSI5 data region A size of 16 bits	
0111	PSI5 data region A size of 17 bits	
1000	PSI5 data region A size of 18 bits	
1001	PSI5 data region A size of 19 bits	
1010	PSI5 data region A size of 20 bits	

1011	PSI5 data region A size of 21 bits	
1100	PSI5 data region A size of 22 bits	
1101	PSI5 data region A size of 23 bits	
1110	PSI5 data region A size of 24 bits	
1111	Reserved	

Table 16 – PSI5DRA bits configuration

- **PSI5REFR** (11bits, W24[11:1])

  This parameter is set the PSI5 Refresh Rate. Bit[10:0] is set the number of bit time. All 0s set 0 bit times, and all 1s set 2023 bit times. Single PSI5 frame length is from 13 bit times to 33bit times, plus at least 3 bit time for gap time. Refresh rate is the user selection of single PSI5 frame length including gap time. Hardware take this number, minus user selection format length, and minimum gap time as 3 bit times, then compensate the rest as gap time.

- **PSI5BR**(1bits, W24[0)

  This bit sets the PSI5 bit time rate.

Bits Value	Bit time	Remarks
0	125kbps	
1	189kbps	

Table 17 – PSI5BR bits configuration

- **IOSEL**(15bits, W25[15:1])

  The IOSEL bits provide the various output selection option. Table 16 shows the IOSEL bits versus output option.

IO1 OUTPUT		**IO2 OUTPUT**		**IO3 OUTPUT**	
Bits	**Remarks**	**Bits**	**Remarks**	**Bits**	**Remarks**
Bit14	1: IO1 Fault mode Enabled, 0: IO1 on normal output mode	Bit13	1: IO2 Fault mode Enabled, 0: IO2 on normal output mode	Bit12	1: IO3 Fault mode Enabled, 0: IO3 on normal output mode
Bit[3:0]		**Bit[7:4]**		**Bit[11:8]**	
1111	Reserved	1111	Reserved	1111	Reserved
1110	Reserved	1110	Reserved	1110	Reserved
1101	TD	1101	TD	1101	TD
1100	Reserved	1100	Reserved	1100	OD SENTB
1011	Reserved	1011	Reserved	1011	OD PWMB
1010	OD SENT	1010	OD SENT	1010	OD SENT
1001	OD PWM	1001	OD PWM	1001	OD PWM
1000	Reserved	1000	Reserved	1000	Reserved
0111	PP PWM	0111	PP PWM	0111	PP PWM
0110	PP PWMB	0110	PP PWMB	0110	PP PWMB
0101	PP SENT	0101	PP SENT	0101	PP SENT
0100	PP IO1	0100	PP IO2	0100	PP IO3
0011	Analog, PGA2, VIN/2	0011	Analog, PGA2, VIN/2	0011	Reserved.
0010	Analog, PGA1, VIN/2	0010	Analog, PGA1, VIN/2	0010	PSI5 IO3
0001	Analog, PGA2, VDD/2	0001	Analog, PGA2, VDD/2	0001	PSI5
0000	Analog, PGA1, VDD/2	0000	Analog, PGA1, VDD/2	0000	Analog DAC

Table 18 - IOSEL Bits Configuration

- **OSCDFB** (1 bit, W25[0])

  The Bit W25[0] is used to set oscillator tail current feed-back control loop. If the bit is set to 0, then analog signal is fed to the oscillator circuit, and if the bit is set to 1, then the value on OSCDAC of EEPROM is fed to the oscillator circuit. Not available when analog mode on IO3 is selected.

- **OSCDAC** (12bit, W26[15:4])

  This parameter is used to set the value of oscillator tail current control when OSCDFB bit is set to 1. Not available when analog mode on IO3 is selected. Also it is used to set TD if TDMASK is set 1.

- **TDMASK** (2bits, W26[3:2])

  This parameter is used to set TD input source selection.

Bit Value	Frame	Remarks
00	Off	
01	DAC	
10	ADC1	
11	ADC2	

Table 19 – TDMASK

- **EEWR** (2 bits, W26[1:0])

  There are two lock bits (W26[1:0]). If any of the two lock bits is set to 1, then EEPROM cannot be written unless IO4 is pulled high to overwrite the EEWR.

- **MESSAGE (16bits, W27[15:0])**

  SENT/PSI5 Serial message. Hardware takes data from MSB to LSB. User input Serial Message contents

- **MSGID** (8bits, W28[15:8])

  Serial Message ID for SENT or PSI5 Serial Message. User input Serial Message ID content - from MSB to LSB

- **TEMPCAL** (10bits, W30[15:6])

  Temperature calibration is used to calibrate the temperature. Default value is 456.

- **Reserved**

Theory of Operation

General Information

The LX3302 is a highly integrated programmable data conversion IC designed for interfacing to and managing of inductive sensors. The device includes an integrated oscillator circuit for driving the primary coil of an inductive sensor, along with two independent analog conversion paths for conditioning, converting, and processing of two analog signals from the secondary coils of the PCB sensor. Each path includes an EMI filter, demodulator, anti-alias filter, programmable amplifier, and a 13-bit sigma-delta analog-to-digital converter before the DSP. DSP peripherals include a SENT serial interface, PSI5 serial interface, programmable PWM controller and a 12-bit digital-to-analog converter.

Oscillator

The on-chip oscillator provides a carrier signal for driving the primary coil of the inductive sensor via pins OSC1 and OSC2. The carrier signal is generated by an internal current source which resonates with the primary inductor and external capacitors (which form a tank circuit). The oscillator operates over a frequency range from 1MHz to 5MHz according to the following equation:

$$f = \frac{1}{2\pi\sqrt{\mathrm{LC}}}, \quad \text{where L} = \text{Inductance of coil, C} = \text{Tanking capacitance}$$

The value of the inductor L is the most critical element in cross-coupled LC tank oscillator. Because the inductance is relatively small, the parasitic resistance of L can dominate and impact the ability to maintain oscillation. As such, the value of inductor L should be as large as possible and with a high Q factor. Small clearance of PCB traces of primary coil contributes significant parasitic capacitance to the tank circuit. The resonant frequency is the result of total equivalent capacitance in the circuit.

In most applications, the inductor L is implemented as traces on a printed circuit board. Depending upon the processing of the PCB, the height and width of the trace will vary, resulting in a variation of the inductance L and the parasitic resistance. Because these variations will change from PCB to PCB, it is necessary to calibrate each sensor PCB independently. Care should be taken to select a PCB source which can achieve manufacturing tolerances required by a given set of system requirements.

The amplitude of the carrier signal is a function of the primary coil tank circuit configuration and feedback of the secondary coil signals from the CL1 and CL2 inputs. The shoulder signals of the tank circuit are protected by an internal clamp circuit. It will distort the sinusoidal waveform if the tank circuit and secondary coil feedback signal is not within design limits.

In order to detect system faults, the IC monitors the amplitude of the carrier signal on pin OSC1. When the amplitude is above or below the specified amplitude (reference electrical spec ‘OSCILLATOR: VOS, Swing Voltage of OSC1&2’) the output pin will be forced to 0V. This output level indicates a system fault. When initially calibrating a sensor, the voltage on OSC1 should be monitored in order to verify that the amplitude is within the specified range. If the OSC1 voltage is too high, this indicates that the signal levels at CL1 and CL2 may be too low. If the OSC1 voltage is too low, this indicates that the signal levels at CL1 and CL2 may be too high.

An internal feedback circuit adjusts the current drive of the oscillator in order to maintain the signal relationship $a^2 \sin^2\theta + b^2 \cos^2\theta = k^2$; wherein ‘k’ is the function of the current source amplitude and coefficients ‘a’ and ‘b’ are the relative areas of the two secondary coils whose signals are applied to CL1 and CL2. The $a^2 \sin^2\theta$ and $b^2 \cos^2\theta$ are obtained by squaring the two input signals CL1 and CL2. In order to reduce the computation complexity, a and b are typically designed to be matched/equal to each other by sensor design. Therefore, the equation becomes $a^2 \sin^2\theta + a^2 \cos^2\theta = a^2$. The letter ‘$a$’ in the equation is the fixed amplitude of the sensor signals. In another words, the oscillator circuit adjusts that carrier amplitude such that the input signals into CL1 and CL2 are maximized. This effectively cancels out non-linearity and variations in the sensor system.

Demodulator, Programmable Gain Amplifier and Anti Alias Filter

Pins CL1 and CL2 are the inputs to two analog signal processing paths. The initial block in each path is a first-order EMI filter which has a low pass cut-off frequency of 13.5MHz. The output of EMI filter is then processed by a demodulator circuit

which removes the carrier such that the relative amplitudes of the CL1 and CL2 signals are retained. In addition to demodulation, the circuit includes a phase detector which determines the phase of the input signal relative to the oscillator signal. This phase detection shifts the demodulated signal to a new reference voltage, $\frac{V_{DD}}{2}$. Demodulator amplifies the signal with gain 7. The output of the demodulator is then passed through a programmable gain amplifier with four bits of range, where the 0000 bit default value is 3.125 (total gain is 21.875). Bit value percentage changes that can be applied to the 3.125 default gain value are show in the following table:

Bit	Function
BIT0	Amplification: +3%
BIT1	Amplification: +6%
BIT2	Amplification: +12%
BIT3	Amplification: -24%

The output of amplifier goes through a low pass anti-aliasing filter prior to input to the sigma-delta ADC. The filter bandwidth is 24kHz. ADC input voltage is the function of receiving coil modulation voltage and its phase shifts to the excitation signal. The following equation describes the calculation of $V_{ADC1}(x)$.

$$V_{ADC1}(x)=\begin{cases} GV(x)+\frac{V_{DD}}{2}, when\ CL1\ phase\ same\ as\ OSC1\ phase \\ \frac{V_{DD}}{2}-GV(x), when\ CL1\ phase\ opposite\ of\ OSC1\ phase \end{cases}$$

- $V(x)$**:** coupling voltage at coupler position x
- V_{DD}: ADC reference voltage
- G: demodulator and amplifier total gain (16.625~26.468) programed by 4 bits in internal EEPROM

Sigma-Delta ADC with Digital Filters

Each analog path includes a 4th-order 13-bit sigma-delta analog-to-digital converter (ADC) with precision internal voltage reference. The sampling frequency for the ADC is derived from the main clock by “REFRESH” in the configuration EEPROM.

The ADC decimation filter includes a SINC filter and a half-band FIR filter. The SINC filter provides -40dB of stop-band attenuation. Because the SINC filter does not provide the same sharp response as a finite/infinite filter response, a half-band FIR filter is also provided. The drawback of the FIR filter is that it adds delay to the input signal and this delay depends upon the number of coefficients and the output data rate. The half-band FIR filter can be selected by “FILTER” in the configuration EEPROM.

The ADC_SYNC provides an output signal which indicates the status of each ADC conversion. When this signal is low, the ADC is either inactive or in the process of performing data conversion. When this signal goes high the present data conversion activity is complete. The ADC_ACK is normally low. After the ADC_SYNC goes active, the DSP may perform post-processing on the data from the ADC. When the post-processing is complete, the ADC_ACK is driven high in order to reset the ADC_SYNC.

Embedded CPU

The LX3302 includes an embedded 32-bit microcontroller core which is used to perform filtering and math functions on the digitized samples from the ADCs. The core operates at one instruction per cycle providing 8MIPS of processing bandwidth. The device includes a watchdog, sets of pre-programmed filtering and math functions which can be selected by setting the appropriate bits in the on-chip configuration EEPROM. Also included in the on-chip configuration EEPROM are system calibration and linearization coefficient bits. The LX3302 has internal 3k-word ROM, 32 word data RAM, and 32x16 bits EEPROM for factory and application calibration.

Configuration EEPROM

The LX3302 includes a user programmable 32 x 16bits EEPROM for storing configuration parameters into non-volatile memory. The device is placed into EEPROM programming mode (EEMode) by increasing the voltage on the VIN pin to 15.3V. Note that a delay of 200µs from power-on must be observed before EEPROM programming mode can be entered.

Data is represented by one of two voltage levels on the VIN pin: a '1' is represented by increasing the VIN voltage to 17.5V, while a '0' is represented by decreasing the VIN voltage to 13V. The voltage for a given bit must be held for a minimum duration of 10µsec and between each bit the voltage must return to 15.3V for a minimum of 20µsec (see diagram below):

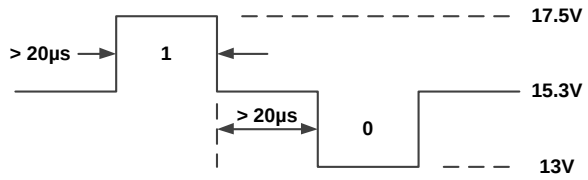


Figure 8 · EEPROM Decoder Block Diagram

The first 5bits sent in EEMode are the command followed by the address bits which is corresponds to the logic level of selected IO pin and reversed 5 bits command. The programming commands are only executed if the address bits and selected IO pin logic level match.

LX3302 employs the watchdog timer, and provides timer for programming write/read or test mode operation. It is required to complete the EEPROM programming or ADC test before the watchdog timer time-out. If the timer is time-out before the programming operation completion, then it will lock the IC operation and it may be unable to access the device due to incomplete data writing.

For detailed programming, refer to AN-S1406 Application Note for LX3302 EEPROM Programming Guide.

PWM Controller

A 16-bit digital PWM controller is implemented on chip. The module allows the user to time and control different events. It can generate a pulse width modulated signal of varying period and duty cycle. The PWM module has a 3bit pre-scalar to divide down the MCU clock signal. PWM frequency is selected by “Refresh” on configuration EEPROM. PWM mode can be set by “IOSEL”. When the PWM is selected, the pull up resistor between IO1/2/3 pin and VIN or VDD is needed, 10KΩ is recommended. PWM frequency is trimmed at factory.

12-Bit DAC

A 12-bit digital to analog converter is implemented on the chip. The module reference voltage is VIN or VDD. Also this DAC is used to set the value of oscillator tail current control and the value of “OSCDAC” in the configuration EEPROM is loaded to this DAC when OSCFB bit is set to 1. Not available when analog mode on IO3 is selected.

SENT (SAE J2716)

SENT is an acronym for Single Edge Nibble Transmission which consists of transmitting 8 nibbles (1 nibble = 4 bits) in sequence. Each nibble is coded using a PWM output referenced to the falling edge. SENT is a point-to-point unidirectional scheme from sensor device to controller. The series of transmitted pulses are measured from falling edge to falling edge (clock tick) with a programmable time granularity of 3µs, 6µs, 12µs, and 24µs,

Each nibble has a defined PWM cycle output. The output is driven low (after the falling edge) for 5 clock ticks first, and then driven high for 7 clock ticks + N clock ticks where N is the decimal value of the nibble. For example, when transmitting a nibble value of 0 (minimum), the output is driven LOW for 5 clock ticks then driven HIGH for 7 clock ticks. The total period for the shortest nibble (n = 0) is therefore 12 clock ticks as shown in the following figure.

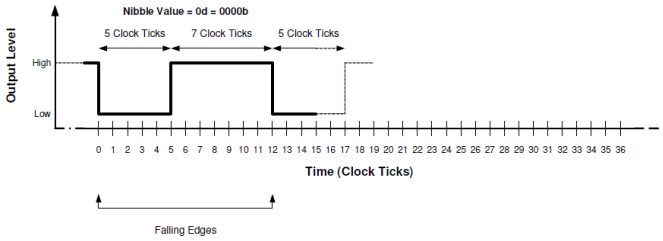


Figure 9 · Timing Diagram for Nibble Value = 0d

For example, when transmitting a nibble value of 15 (maximum), the output is driven LOW for 5 clock ticks then driven HIGH for 22 (7+15) clock ticks. The total period for the longest nibble (n = 15) is therefore 27 clock ticks as shown in the following figure.

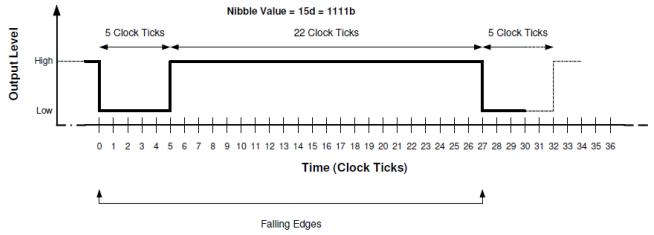


Figure 10 · Timing Diagram for Nibble Value = 15d

Transmission sequence:

1. Calibration/Synchronization pulse period of 56 clock ticks.
2. One 4 bit Status and Serial Communication nibble pulse of 12 to 27 clock ticks.
3. A sequence of six 4-bit Data nibble pulses (12 to 27 clock ticks each) representing the values of the signal(s) to be communicated.
4. One 4 bit Checksum nibble pulse of 12 to 27 clock ticks.

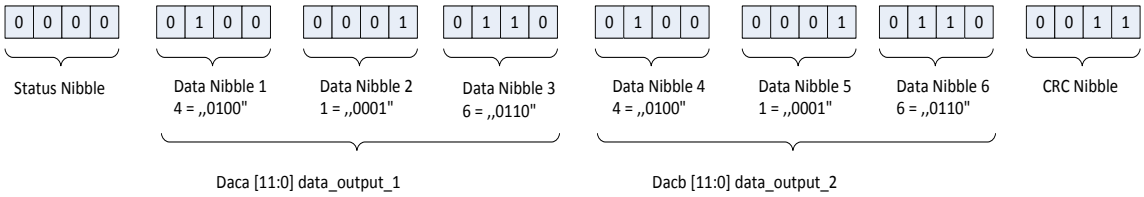


Figure 11 · Encoded SENT Format for 0x416

Without pause pulse, one transmission consists of 154 to 270 clock ticks. The transmission rate depends on firmware operation.

Calibration pulse:

1. 56 clock ticks period consists of 5 clock ticks driven low plus 51 clock ticks driven high
2. The period is measured by receiving module to calibrate/synchronize the clock time

Status nibble:

1. Bit0 is reserved as 0 for the standard protocol. For A.3 and A.4 appendix protocols, “0” represents the sensor no error, and “1” represents the sensor error. For A.1 appendix protocol, “0” represents the throttle 1 no error, and “1” represents the throttle 1 error. For A.2 appendix protocol, “0” represents the mass air flow signal no error, and “1” represents the mass air flow signal error.

2. Bit1 is reserved as 0 for the standard protocol. For A.3 and A.4 appendix protocols, bit1 is always “0”. For A.1 appendix protocol, “0” represents the throttle 2 no error, and “1” represents the throttle 2 error. For A.2 appendix protocol, “0” represents the pressure at mass air flow signal no error, and “1” represents the pressure at mass air flow signal error.
3. Bit 2: Serial Data message bit. For standard protocol and A.1, A.3, A.4 appendix protocols, this bit is reserved as “0”. A.2 appendix protocol optionally uses this bit to transmit temperature, humidity and barometric pressure signal.
4. Bit 3 (MSB): Message start=1, otherwise=0, or serial data message bit. For standard protocol and A.1, A.3, A.4 appendix protocols, this bit is reserved as “0”. A.2 appendix protocol optionally uses this bit to transmit temperature, humidity and barometric pressure signal.

If A.2 protocol is selected and serial message is needed, LX3302 is able to support two serial message formats:

1. Short serial message format

Serial data is transmitted in a 16-bit sequence in status nibble bit 2 as shown in Figure 12. The starting bit of a serial message is indicated by a “1” in bit 3, and then next 15 frames bit 3= “0”.

The 16-bit message consists of a 4-bit Message ID nibble, 8-bit of data, and a 4-bit CRC checksum. The CRC checksum is derived for the Message ID and 8-bit data and is the same checksum algorithm as used to calculate the SENT CRC nibble. The Message ID is used to identify the type of data being communicated in the 8-bit data. Please refer to appendix for detail.

Data transmitted in the bit 2 is sent from Most Significant Bit to Least Significant Bit.

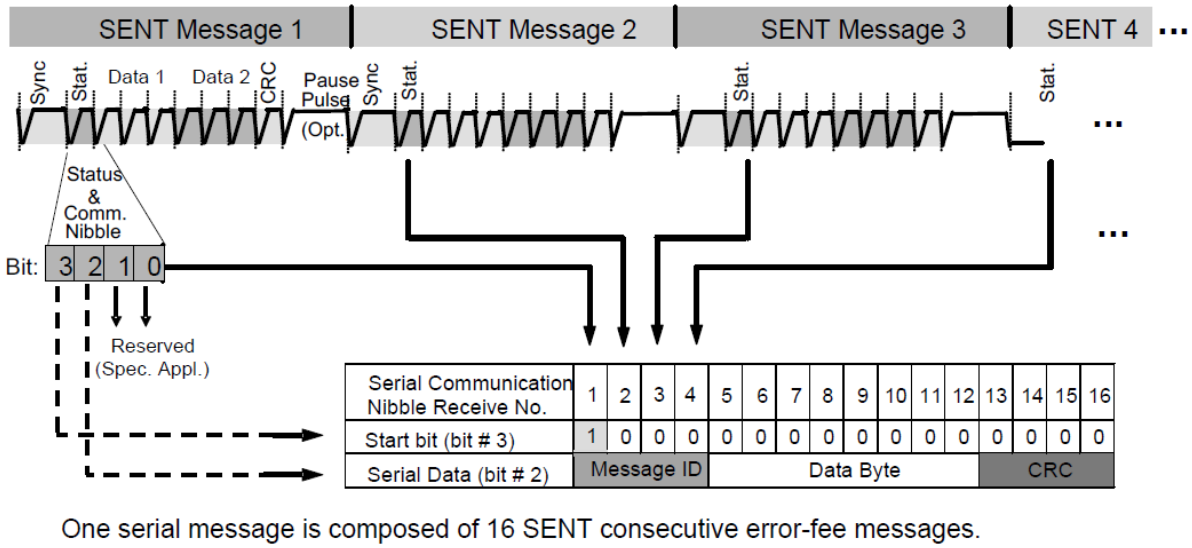


Figure 12 · Short serial message format

2. Enhanced serial message format

The other serial message format optional is Enhance serial message format. It is used for lager data field and larger ID message. Both bit 2 and bit 3 are used for this format. It stretches over 18 consecutive SENT messages as shown in Figure 13.

This 18 consecutive message starts with fixed pattern “1111110” in bit 3. The bit 3 of 7th, 13th and 18th message frame are set to “0”. All data transferred from MSB to LSB.

The serial message frame contains 21 bits of payload data. Two different configurations can be chosen determined by bit 3 of frame 8th.

- 12-bit data and 8-bit message ID (configuration bit = 0, Fig. 17)
- 16-bit data and 4-bit message ID (configuration bit = 1, Fig. 18)

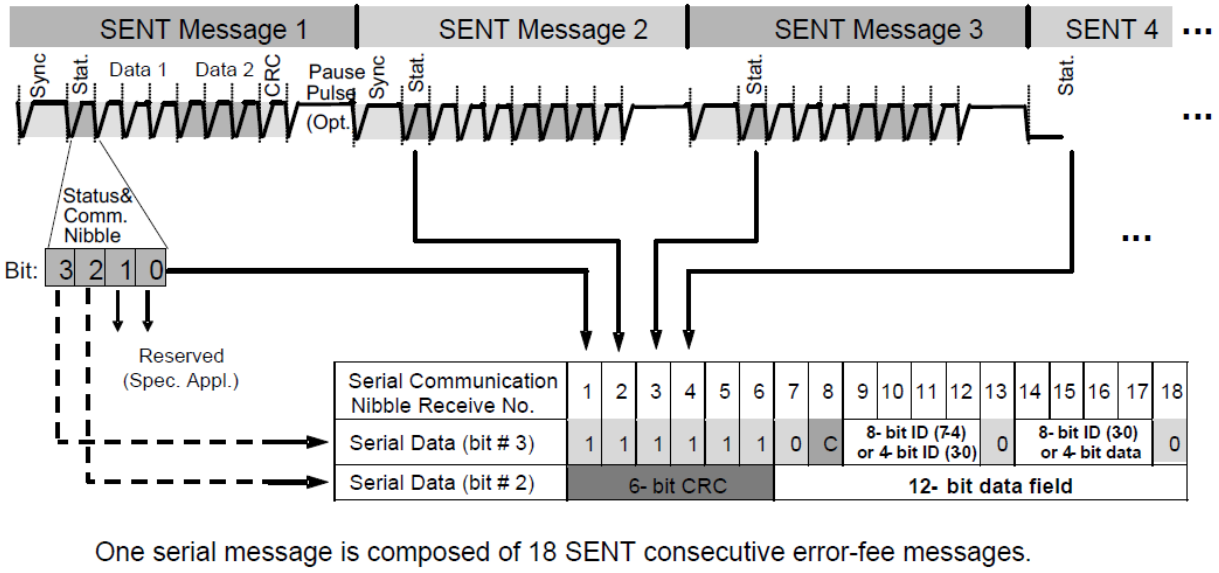


Figure 13 · Enhanced serial message format

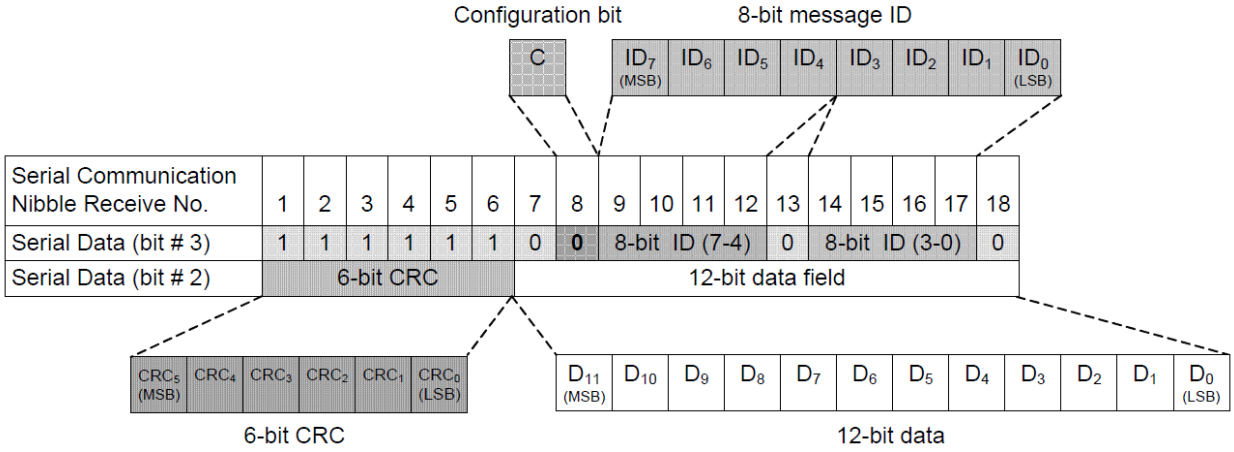


Figure 14 · 12-bit data and 8-bit message ID

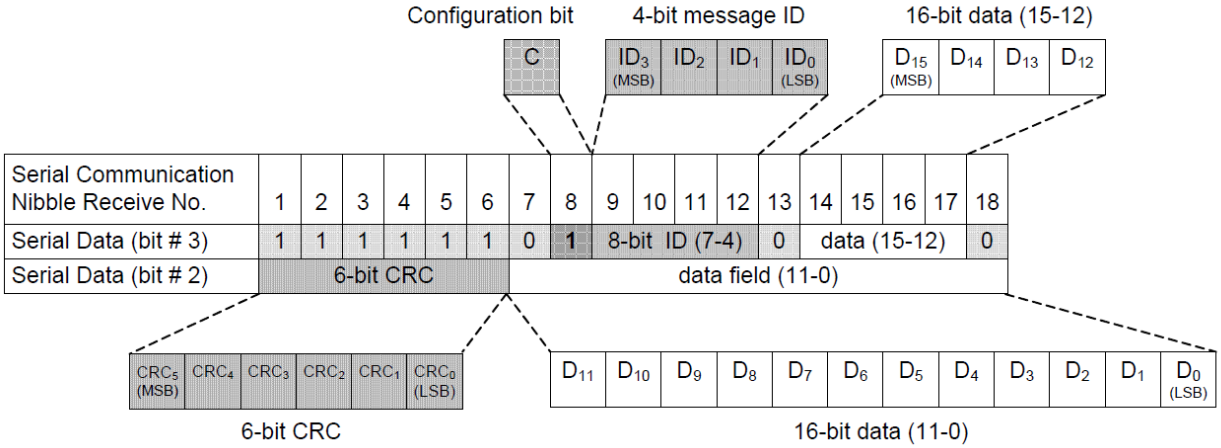


Figure 15 · 16-bit data and 4-bit message ID

CRC for enhanced serial message format:

This CRC-value is computed as a function of the contents of Serial data message bits #2 and #3 for frames 7th - 18th. See Fig 19 for CRC order and detail

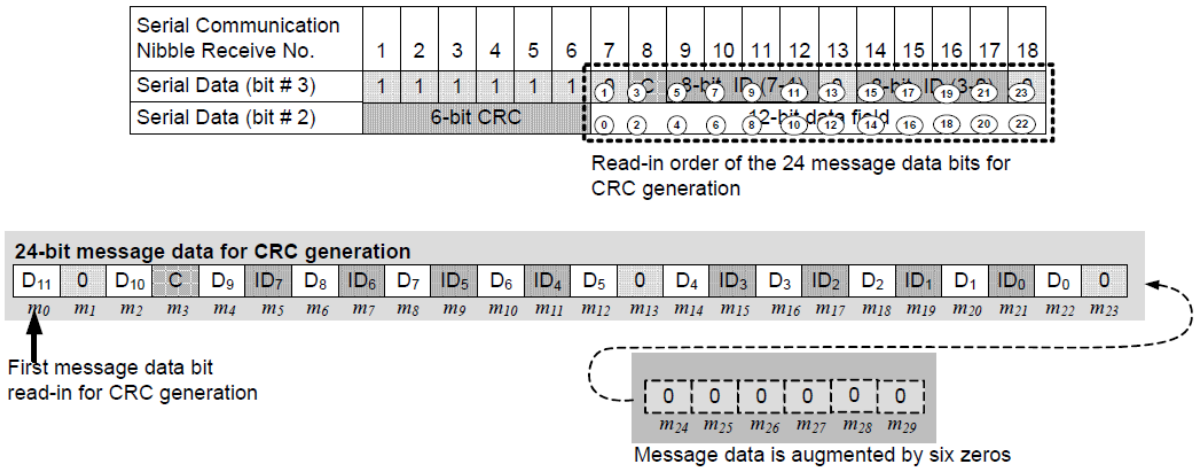


Figure 16 · CRC for enhanced serial message

The encoding is defined by the generating polynomial. G(x) = x6+x4+x3+1 with seed value 010101. For CRC generation, the message will be augmented by six zeros. Mcrc = [m0 m1 m2 ……. M21 m22 m23 0 0 0 0 0 0].

Data nibble:

SENT has 6 data nibbles. Register SENT_data1 content is sent out as data nibble 1 to 3, register SENT_data2 content is sent out as data nibble 4 to 6.

For standard SENT protocol, 12-bit sensor position information can be stored in SENT_data1 register, and the same data is replicated in SENT_data2 of register. The most significant nibble of each data is transmitted first. After status nibble pulse, the first data nibble is transmitted starting with 5 ticks driven low, followed by 7 ticks driven high, then extended by the data nibble decimal ticks. The rest of data nibbles are transmitted in the same manner.

LX3302 supports SENT A3 and A4 protocol. It meets following requirements:

1. Sensor value is transmitted as a 12 bit value in this nibble order:
   data nibble 1: MSN,
   data nibble 2: MidN,
   data nibble 3: LSN.
2. Data nibbles 4 and 5 are an 8 bit rolling counter 0 to 255 with rollover back to 0. Data nibble 4 is the MSN and data nibble 5 is the LSN of the counter value. There is a register bit in internal EEPROM can manually reset the counter.
3. For A3 protocol, data nibble 6 is the inverted copy of nibble 1 (15 minus nibble 1 value).
4. For A4 protocol, data nibble 6 can be the same format as A3 protocol or reset it to zero. Data nibble4 and 5 is the rolling counter or set to all zero

CRC nibble:

Recommend implementation: It contains a 4 bit CRC of the data nibbles only. The “Status and Communication Nibble” is not included in the CRC calculation. The CRC is calculated using polynomial $x^4 + x^3 + x^2 + 1$ with a binary initialization value of 0101. The augment message data is extended with 4 extra zero bits.

Legacy implementation: The CRC checksum can also be implemented as a series of shift left by 4 followed by a 256 array lookup. (Following table)

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
13 12 15 14 9 8 11 10 5 4 7 6 1 0 3 2
7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8
10 11 8 9 14 15 12 13 2 3 0 1 6 7 4 5
14 15 12 13 10 11 8 9 6 7 4 5 2 3 0 1
3 2 1 0 7 6 5 4 11 10 9 8 15 14 13 12
9 8 11 10 13 12 15 14 1 0 3 2 5 4 7 6
4 5 6 7 0 1 2 3 12 13 14 15 8 9 10 11
1 0 3 2 5 4 7 6 9 8 11 10 13 12 15 14
12 13 14 15 8 9 10 11 4 5 6 7 0 1 2 3
6 7 4 5 2 3 0 1 14 15 12 13 10 11 8 9
11 10 9 8 15 14 13 12 3 2 1 0 7 6 5 4
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
2 3 0 1 6 7 4 5 10 11 8 9 14 15 12 13
8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7
5 4 7 6 1 0 3 2 13 12 15 14 9 8 11 10

Pause Pulse: (optional)

Pause pulse is an extra fill pulse which is transmitted after the CRC nibble. It is mainly used to create a SENT transmission with constant number of clock ticks. Its length is from 12 ticks (5 driven low + 7 driven high) to 768 ticks (5 driven low + 763 driven high).

Once the pause pulse is enabled, two options are used to determine the length of the pause pulse. The first one is to sync the whole single SENT message length to either ADC_SYNC or PWM. The second option is to sync the whole single SENT with certain constant number of clock ticks, rang from 166 to 1038.

Physical layer requirement:

1. Transmission rate:

Transmission bit rate is variable depending on the clock tick period, data value and clock variance. The longest transmission time is 270 clock ticks or 972us at 3us clock time period. This is also the worst transmission rate 24.7kBits/sec. The shortest is 154 message clocks, with a 64.9kBits/sec rate (not includes serial data)

2. Clock Tolerance

Variation of maximum nibble time compared to the expected time derived from the calibration pulse time at a 3 µs clock tick is ≤ 0.05 µs

3. Electrical Interface requirements

SENT signal is seen as a nominal 5V square wave signal, but for low radiated emissions purpose, signal shaping is required. To minimize ground and supply offset effects, the receiving device shall provide a regulated 5 V supply and ground reference to the LX3302 SENT pin.

Example SENT test topology, the transmitter portion of these circuits is examples only and should not be taken as a direct implementation requirement.

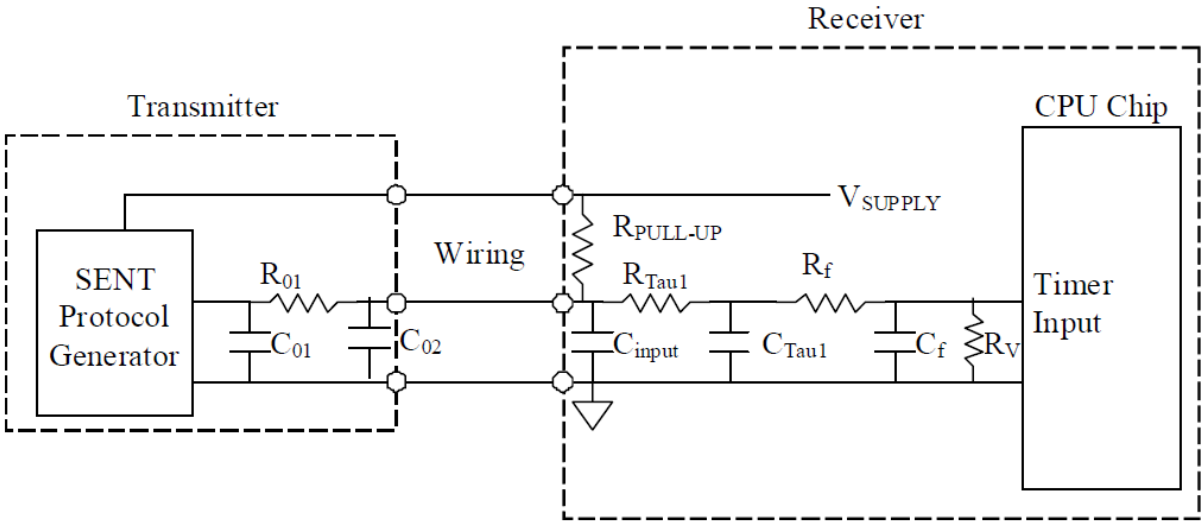


Figure 17 · SENT test topology

4. SENT Driver requirements:

LX3302 SENT need a push pull pin as output pin. The LX3302 SENT driver ensures that the signal rise and fall time requirements are met when driving into the receiver passive load. LX3302 protects damage from over voltage or current conditions. It turns SENT driver OFF to prevent damage.

In addition an EMC filter consisting of a capacitor followed by a resistor in series with the output pin is recommended to attenuate RF energy coupled on the external signal line.

5. Fault Protection Modes:

Short to GND – An impedance of less than 50 ohms between the line and ground is considered a short to ground. Upon removal of the fault, LX3302 resets and resume normal operation

Short to Supply – An impedance of less than 50 ohms between the line and VOUT is considered a short to ground. Upon removal of the fault, LX3302 resets and resume normal operation

PSI5 (Peripheral Sensor Interface)

The Peripheral Sensor Interface (PSI5) is an interface developed for automotive applications. Key features include:

- Two-wire current interface
- Manchester coded digital data transmission
- High EMC immunity and low emissions
- 10 to 28 bit payload data word length
- Asynchronous mode

General requirement:

LX3302 input voltage is from 4V to 11V to compile with PSI5 protocol

Since PSI5 is an open protocol, each section of the frame format, including status, serial messaging channel, frame control, data region B, data region A, need to have its own register to turn on/off the optional section, output any data and be able choose variable length. The goal is to ensure the LX3302 has the most flexibility to meet any requirement within PSI5 protocol.

Transmission sequence:

A “low” level is represented by the normal quiescent current consumption of the sensor. A “high” level is generated by an increased current sink of the sensor. The current modulation is detected within the Electronics Control Unit receiver. Manchester coding represents logic “0” by the rising edge and logic “1” by the falling edge of the sending current. The following figure shows the current level thresholds.

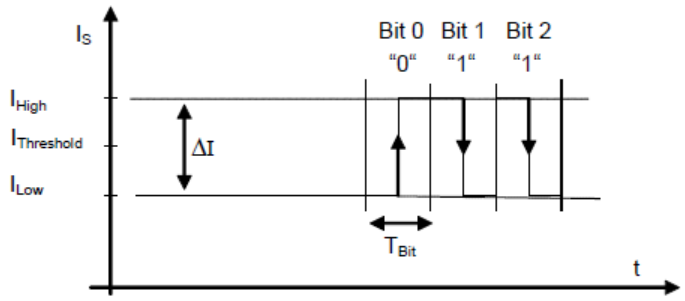


Figure 18 · Bit encoding by Current Modulation

The LX3302 PSI5 asynchronous mode operation consists of the following sequence: (Figure 19.)

- Mandatory two start bits, S1,S2
- Serial messaging channel, M0, M1 (optional 0 or 2bit)
- Frame control, F0,…F[q-1] (optional 0, 1, 2, 3, or 4 bit)
- Status, E0, … E[r-1] (optional, 0, 1 or 2bit)
- Data region B, B0, … B[m-1] (optional 0, or scalable m=1 to 12 with 1-bit increment)
- Mandatory data region A, A0, … A[n-1] (scalable n=10 to 24 with 1-bit increment)
- Mandatory Error check bit (3-bits CRC C2, C1, C3 or 1-bit parity)

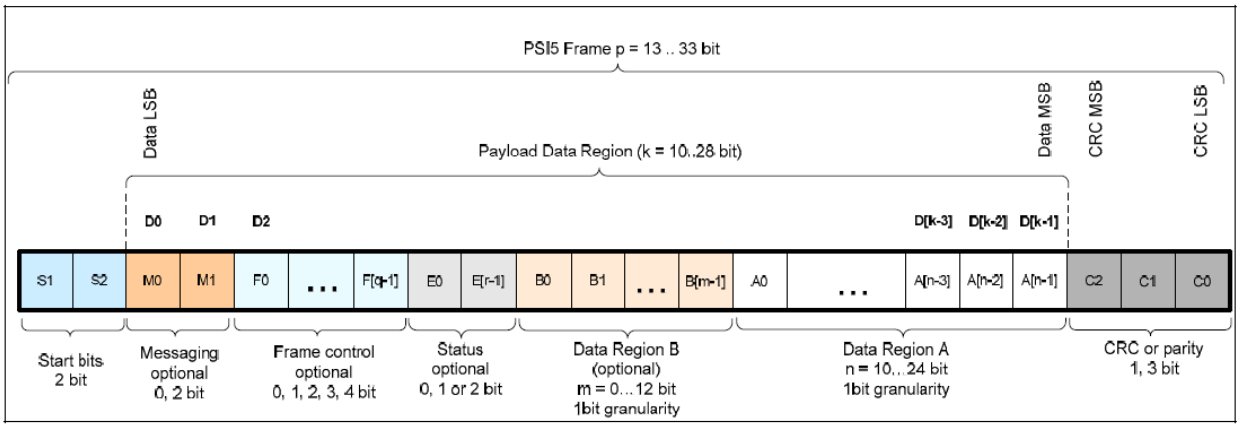


Figure 19 · PSI5 single frame sequence format

The single PSI5 message length is from 13 to 33 bits, including any optional format of payload data region and start bits and CRC/parity. The payload data region length is from 10 to 28 bits. One example shows if optional bits are enabled, how the format looks like. If the sensor position information is 0xB54 (Binary: 1011 0101 0100), it will be encoded as

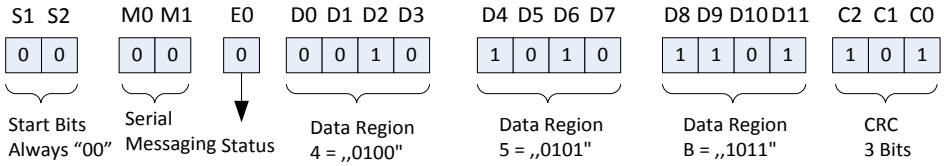


Figure 20 · Encoded PSI5 Format for 0xB54

Start bits:

2 start bits are defined as 00b all the time. It is transmitted at the beginning of the sequence.

Serial messaging channel:

Serial messaging channel is used to transmit data message over 18 consecutive PSI5 frames. Once it is enabled, it is transmitted following the start bits. Serial messaging channel is optional, it has its own register, can be fully controlled to meeting following requirements.

Figure 21 shows how M1 transient serial data starting from PSI5 frame #1 to #18, and then repeat itself from frame #1. The M1 [8] determines the serial format. If it was set to 0, serial format that has 12bit data field with 8bit ID is selected.

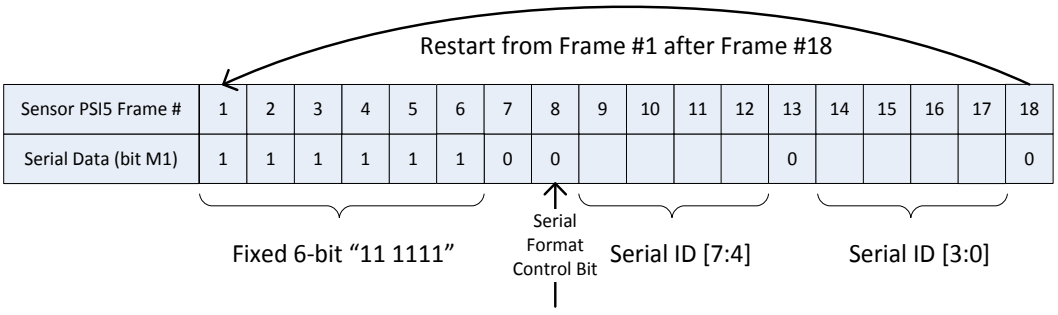


Figure 21 · Serial Data Frame generated by [M1] when M1[8] =0

Figure 22 shows how M0 transient serial data starting from PSI5 frame #1 to #18, and then repeat itself from frame #1.

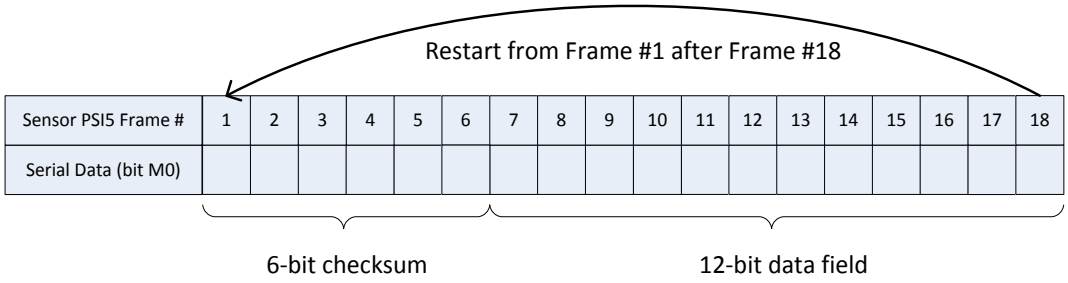


Figure 22 · Serial Data Frame generated by [M0] when M1[8] =0

If M1[8] was set to 1, serial format that has 16bit data field with 4bit ID is selected. Figure 23 and 24 show how M0 and M1 being formatted

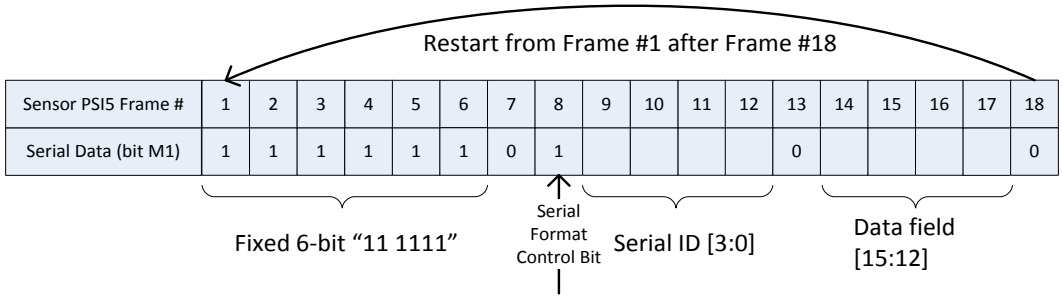


Figure 23 · Serial Data Frame generated by [M1] when M1[8] =1

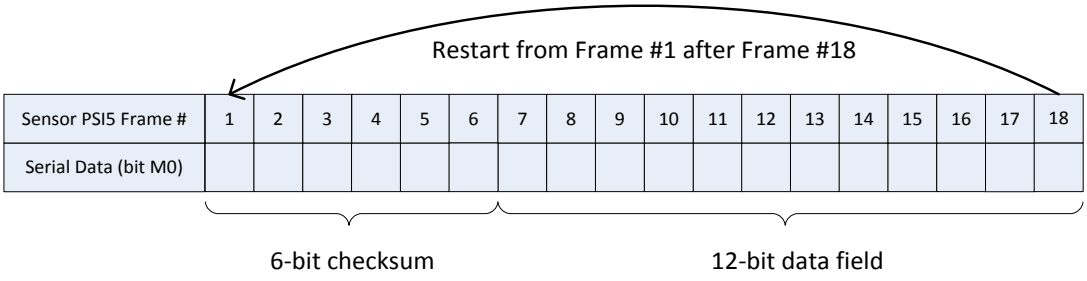


Figure 24 · Serial Data Frame generated by [M0] when M1[8] =1

The generator polynomial of the 6-bit checksum for both above serial formats is g(x)=1+x3+x4+x6 with a binary initialization value “010101” The CRC value is derived from the serial messaging contents of sensor PSI5 frame #7 to #18. The bits are read into a newly generated message data word starting with the serial Data bit M0 of sensor PSI5 frame #7 and ending with the serial data bit M1 of sensor PSI5 frame #18.

For CRC generation the transmitter extends the message data by six zeros, this augmented data word is fed into the shift registers of the CRC check. When the last zero of the augmentation is pending on the input adder, the shift registers contain the CRC checksum. These six check bits is transmitted MSB first. [C5, C4, ... C0] Following figure shows the reading order.

Sensor PSI5 Frame #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Serial Data (bit M1)								*1*	*3*	*5*	*7*	*9*	*11*	*13*	*15*	*17*	*19*	*21*	*23*
Serial Data (bit M0)								*0*	*2*	*4*	*6*	*8*	*12*	*14*	*16*	*18*	*20*	*22*	*24*

Messaging bits for checksum calculation

Figure 25 · Read order of serial data checksum

Please note: the serial data checksum is not the same as 3-bit checksum of total PSI5 frame.

Frame control

Frame control bits are used to indicate type of frame or data content, or identify the sensor. Once it is enabled, it is transmitted following the serial message channel bits. Frame control is optional. It has its own register. Length of the frame control can be selected from 1 bit to 4bit with 1-bit increment.

Status bits

Status bits are used to indicate if there is any error happens on the sensor. Once it is enabled, it is transmitted following the frame control bits. Status bits are optional. It has its own register. Length of the status can be selected from 1 bit to 2 bit

Data region B

Data region B services as additional data region. Once it is enabled, it is transmitted following the status bits, with data order from LSB to MSB. Data region B is optional. It has its own register, Length of the data region B can be selected from 1 bit to 12 bit with 1-bit increment once it is enabled.

Data region A

Data region A is the main data region. It is transmitted following the data region B with data order from LSB to MSB. Data region A is mandatory. It has its own register, Length of the data region A can be selected from 10 bit to 12 bit with 1-bit increment.

Error check

Error detection in PSI5 transmission is realized by a single bit even parity or 3-bit CRC [C2 C1 C0]. It can be selected by toggle register bit.

Once the 3-bit CRC is selected, the generator polynomial of the CRC is x3 + x + 1 with a binary CRC initialization value “111”. The transmitter extends the data bits by three zeros as MSBs. This augmented data word is fed into the shift register CRC check as LSB first. The start bits are ignored in this check. When the last zero of the augmentation is pending on the input adder, the shift registers contain the CRC checksum. These three check bits are transmitted in reverse order (MSB first: C2, C1, C0)

PSI5 Sensor Power-on requirement:

A maximum start up time is specified to make sure LX3302 sinks to quiescent current.

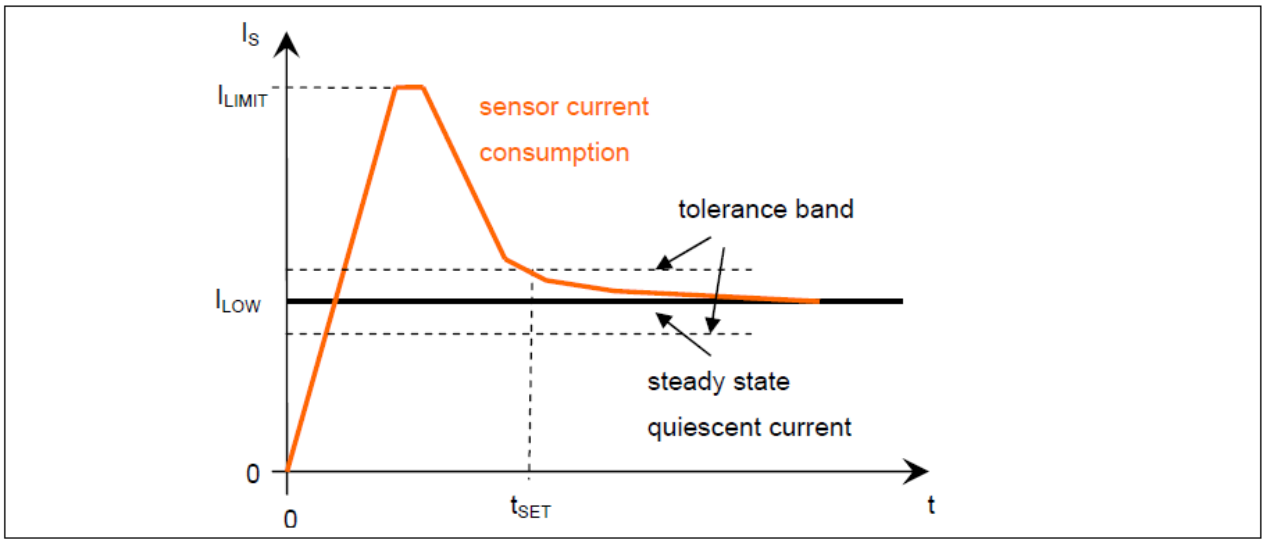


Figure 26 · Current settling during the startup

PSI5 Sensor damping behavior:

The LX3302 PSI5 pin damping behavior is described in following figure. A complex impedance ZS consists of an equivalent resistance $R_{eq,S}$, an equivalent capacitance $C_{eq,S}$ connected in serial, and given frequency range from 10 to 2000 kHz.

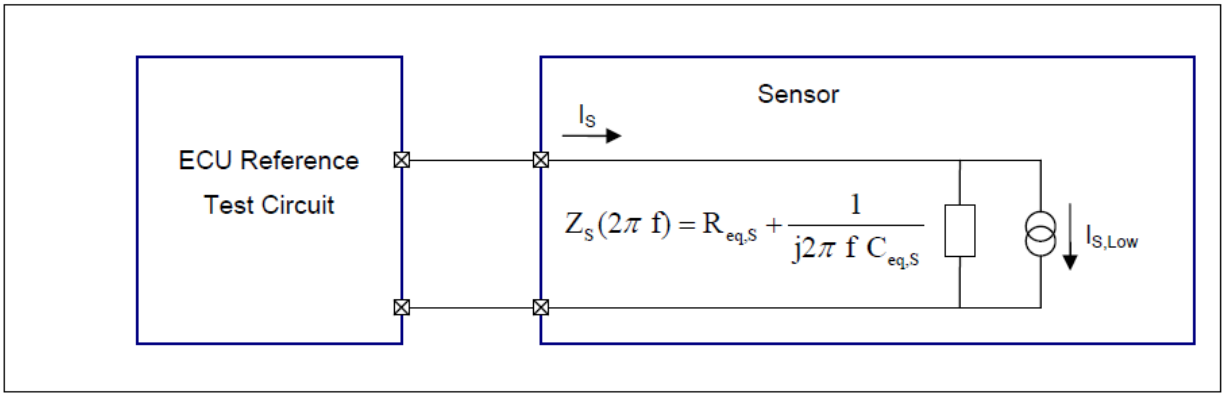


Figure 27 · LX3302 damping behavior model

PSI5 Sensor current requirement:

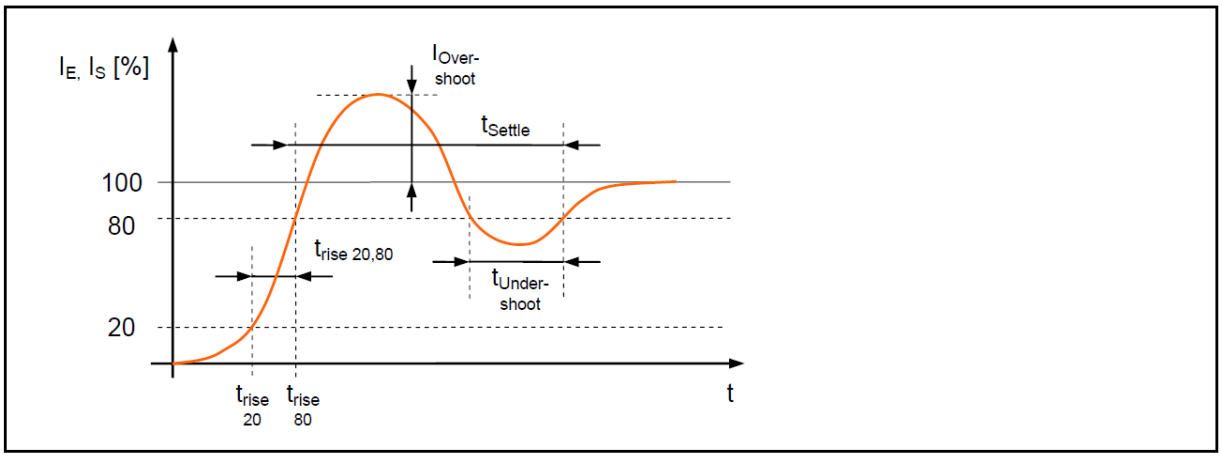


Figure 28 · LX3302 PSI5 current model

High Voltage LDO

The regulator provides the internal power to the chip and also provides power for external components such as pull-up resistors. Over current protection is implemented with the regulator. Decoupling caps is required to ensure high performance analog measurements, minimum 100nF, recommended value is 1µF. VDD is pre-trimmed at factory.

Reference Schematics

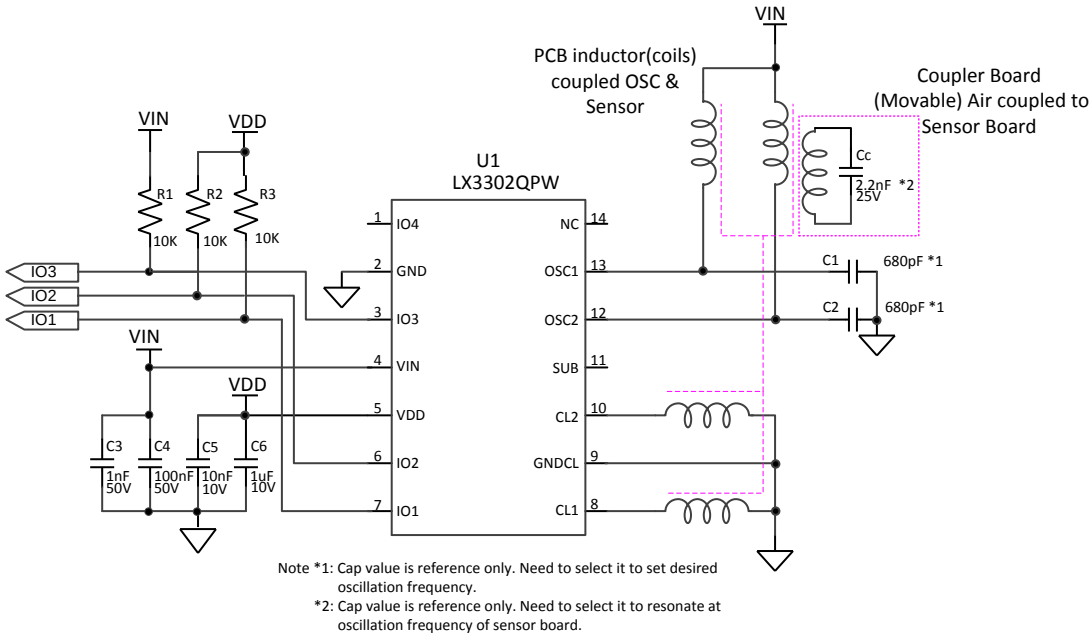
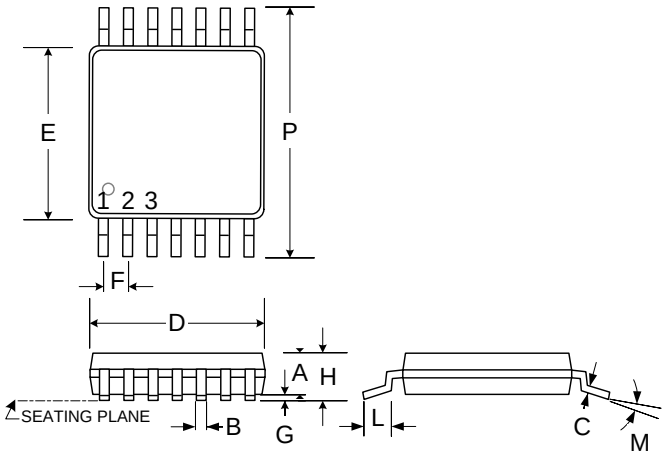


Figure 29 · LX3302 14-Pin Reference Schematic

Package Outline Dimensions

Controlling dimensions are in millimeters, inches equivalents are shown for general information.

PW **14-Pin Thin Small Shrink Outline (TSSOP)**



Dim	Millimeters		Inches	
	MIN	**MAX**	**MIN**	**MAX**
A	0.85	0.95	0.033	0.037
B	0.17	0.27	0.007	0.011
C	0.09	0.20	0.004	0.008
D	4.90	5.10	0.193	0.201
E	4.30	4.50	0.169	0.177
F	0.65 BSC		0.026 BSC	
G	0.05	0.15	0.002	0.006
H	-	1.10	-	0.043
L	0.45	0.75	0.0177	0.030
M	0°	8°	0°	8°
P	6.4 BSC		0.252 BSC	
*LC	-	0.10	-	0.004

*Lead Coplanarity

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006”) on any side. Lead dimension shall not include solder coverage.

Revision	Date	Changes	Comment/Editor
0.0	12/1/14	Preliminary Datasheet	
0.1	12/4/15	Added ESD, revised EC parameters per Eval review result	

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