DATA SHEET

APRIL 1997
Revision 2.1

LXT312 / LXT315

Low Power T1 PCM Repeaters / Transceivers

General Description

The LXT312 and LXT315 are integrated repeater/transceiver circuits for T1 carrier systems. The LXT312 is a dual repeater/transceiver and the LXT315 is a single repeater/transceiver. The LXT312 and LXT315 are designed to operate as regenerative repeaters/transceivers for 1.544 Mbps data rate PCM lines. Each includes all circuits required for a regenerative repeater/transceiver system including the equalization network, automatic line build-out (ALBO), and a state-of-the-art analog/digital clock extraction network tuned by an external crystal.

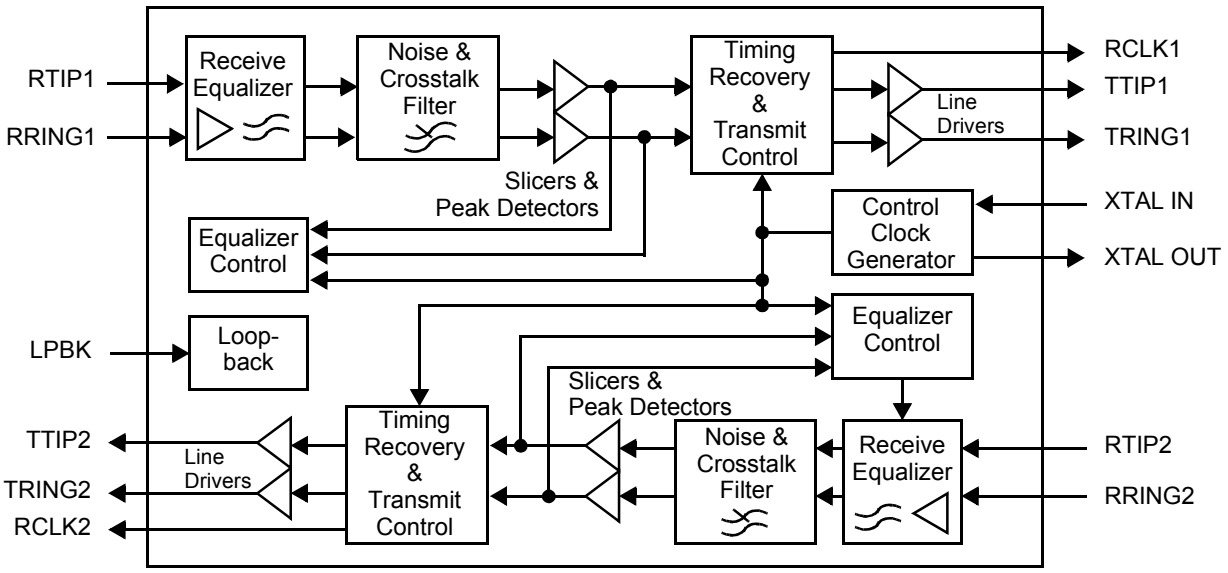
The key feature of the LXT312 family is that it requires only a crystal and a minimum of other components to complete a repeater/transceiver design. Compared with traditional tuned coil-type repeaters/transceivers, they offer significant savings in component and labor costs, along with reduced voltage drop/power consumption, and improved reliability. To ensure performance for all loop lengths, the LXT312 and LXT315 are 100% AC/DC tested using inputs generated by Level One's proprietary transmission line and network simulator.

The LXT312 and LXT315 are advanced CMOS devices which require only a single 5-volt power supply.

Features

- Integrated repeater/transceiver circuit on a single CMOS chip
- On-chip equalization network
- On-chip ALBO
- Low power consumption
- No tuning coil
- On-chip Loopback
- Recovered Clock Output
- 0 to 36 dB dynamic range
- -11 dB interference margin
- Compatible with CB113/TA24 specifications
- Single 5 V only CMOS technology
- Available in 16-pin PDIP and 44-pin PLCC

LXT312 / LXT315 Block Diagram



LEVEL ONE

PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT312 / LXT315 Pin Assignments

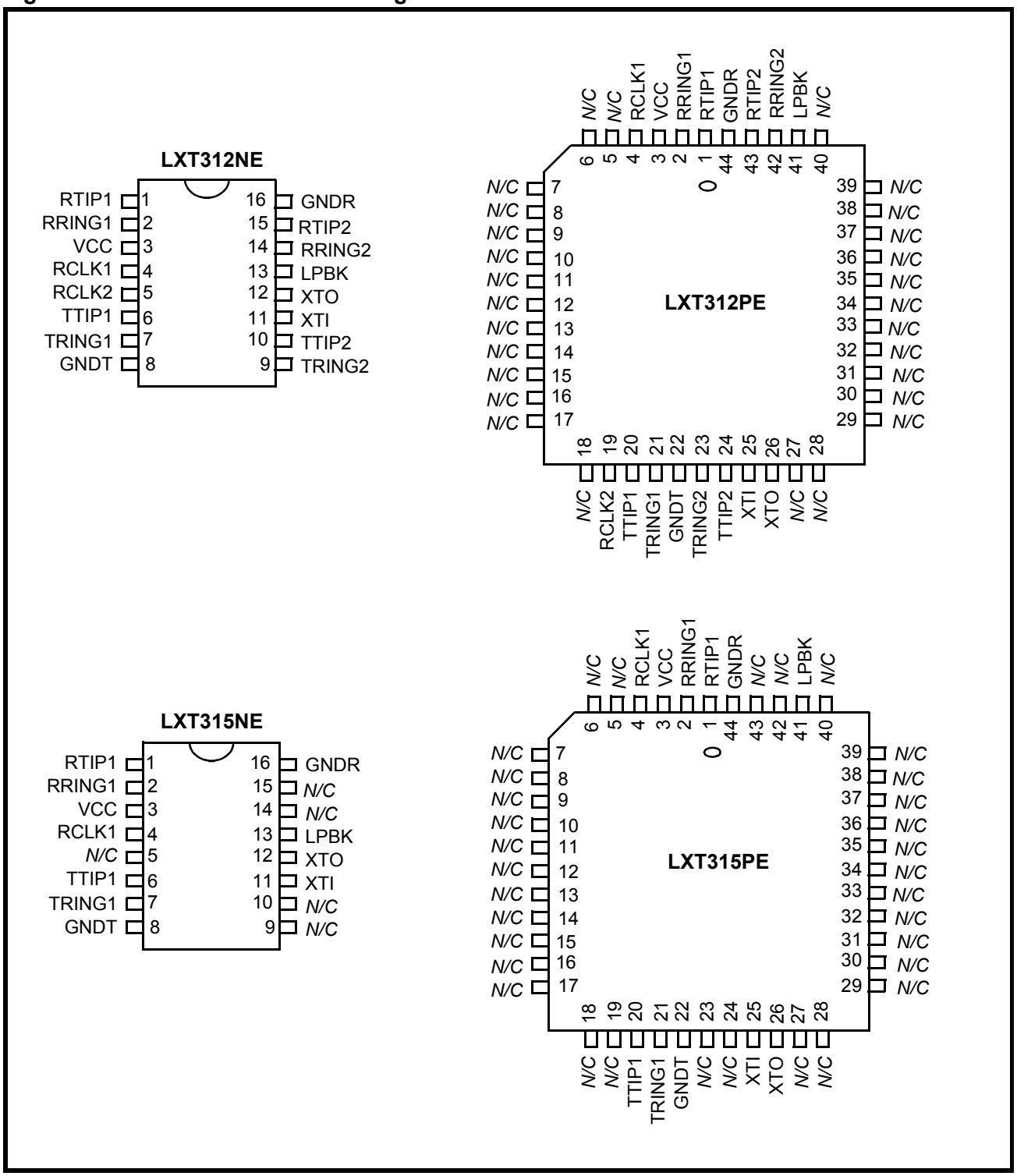


Table 1: LXT 312 / LXT315 Signal Descriptions

Pin #		Symbol	I/O	Description
PDIP	PLCC			
1 2	1 2	RTIP1 RRING1	I I	**Repeater Tip and Ring Inputs.** Tip and ring receive inputs for Channel 1.
4	4	RCLK1	O	**Recovered Clock.** Clock output recovered from Channel 1 receive input.
6 7	20 21	TTIP1 TRING1	O O	**Repeater Tip and Ring Outputs.** Open-drain output drivers for Channel 1.
11 12	25 26	XTI XTO	I O	**Crystal Oscillator Pins.** A 6.176 MHz crystal must be connected across these two pins.
3	3	VCC	–	**Power Supply.** Power supply input for all circuits. +5 V (±0.25 V).
8 16	22 44	GNDT GNDR	– –	**Transmit Ground.** Ground return for transmit circuits. **Receive Ground.** Ground return for receive circuits.
9[1] 10[1]	23[1] 24[1]	TRING2 TTIP2	O O	**Side 2 Ring and Tip Outputs.** On the LXT312 dual repeater/transceiver, these are open-drain output drivers for Channel 2.
14[1] 15[1]	42[1] 43[1]	RRING2 RTIP2	I I	**Side 2 Ring and Tip Inputs.** On the LXT312 repeater/transceiver, these are tip and ring receive inputs for Channel 2.
5[1]	19[1]	RCLK2	O	**Recovered Clock.** On the LXT312 dual repeater/transceiver, this is the recovered clock output for Channel 2.
13	41	LPBK	I	**Loopback Control.** On the LXT312, this pin controls Loopback Selection: High = Loopback side 1 data to side 2. Low = No Loopback. ***On LXT315 single repeater/transceiver, this pin must be connected to GND.***

1. On the LXT315NE and LXT315PE single repeater/transceiver, these pins are not connected (N/C).
2. On the LXT312PE and LXT315PE, pins 5 through 18 and 27 through 40 are not connected (N/C).

FUNCTIONAL DESCRIPTION

Introduction

PCM signals are attenuated and dispersed in time as they travel down a transmission line. Repeaters/transceivers are required to amplify, reshape, regenerate and retime the PCM signal, then retransmit it.

The LXT312 and LXT315 each contain all the circuits required to build a complete PCM repeater/transceiver. The operational range of the repeaters/transceivers is 0 to 36 dB of cable loss at 772 kHz (equal to 6300 feet of 22 gauge pulp-insulated cable between repeaters).

Receive Function

The signal is received through a 1:1 transformer at RTIP and RRING and equalized for up to 36 dB of cable loss. The receive equalizer uses a proprietary on-chip adaptive filter technique which is equivalent to a 3-port ALBO equalizer design. The monolithic structure of the filter and the absence of external components provide excellent ISI and dispersion elimination, and accurate data transfer over temperature.

Receiver noise immunity is optimized by a proprietary crosstalk elimination filter which eliminates the unneeded high-frequency components of the received signal.

Timing Recovery Function

The equalized signal is full wave rectified and used to generate information for the timing recovery circuit. This circuit uses a mixed analog/digital technique to provide a low-jitter PLL similar to a tuned tank with excellent jitter tracking ability. But unlike a tuned tank, the free running frequency of the PLL clock is accurately controlled by the external reference crystal. No adjustment is required. Refer to Application Information for crystal specifications.

Recovered clock signals are available on the RCLK pins for applications that require synchronization to the bit stream.

Transmit Function

Recovered data is re-synchronized to the recovered clock signal by the timing recovery and transmit control section. The data is then retransmitted to the network via two open-drain, high-voltage transistors.

Loopback Function (LXT312 Only)

The LXT312 includes a loopback function for network diagnostics. With the LPBK pin Low, the repeater/transceiver operates in the normal mode. When the LPBK pin is pulled High, the data is looped back from side 1 to side 2.

APPLICATION INFORMATION

Introduction

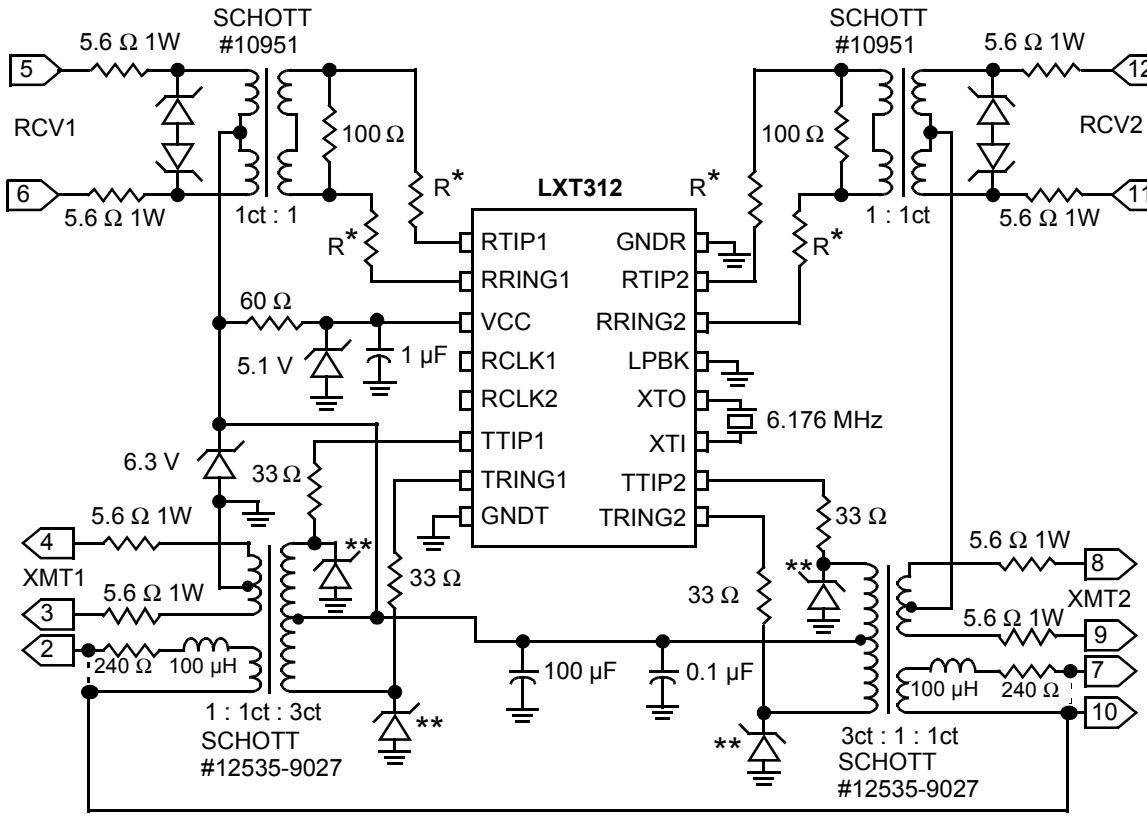
Figure 2 shows a typical T1 dual repeater/transceiver application using an LXT312 repeater/transceiver with standard PCB edge connectors. It includes a jumper-selectable shorting option (dashed lines at connector pins 2 and 7) for the fault location circuitry. Table 2 lists the specifications required for the crystal used with the LXT312 or LXT315 repeater/transceiver.

Table 2: Crystal Specifications

Parameter	Specification
Frequency	6.176 MHz
Frequency tolerance[1]	± 50 ppm
Effective series resistance	40 Ω Maximum
Crystal cut	AT
Resonance	Parallel
Maximum drive level	2.0 mW
Mode of operation	Fundamental

1. @ 25 °C, C Load = 10 pF; and from -40 °C to +85 °C (Ref 25 °C reading)

Figure 2: Typical T1 Dual Repeater/Transceiver Application



NOTES:

* RTIP/RRING Resistors are used to provide surge protection. Values can be 0 – 100 Ω.

** TTIP/TRING Zeners are used to reduce surge susceptibility. Values can be 12 – 14 V.

TEST SPECIFICATIONS

NOTE

Minimum and maximum values in Table 3 through Table 6 and Figure 3 through Figure 11 represent the performance specifications of the LXT312/315 repeaters/transceivers and are guaranteed by test except, as noted, by design

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Units
Supply voltage (min to max)	V_{CC}	-0.3 V to +6 V
Driver Voltage	V_{OH}	18 V
Receiver Current	I_{CC}	100 mA
Operating temperature (min to max)	T_{OP}	-40 °C to +85 °C
Storage temperature (min to max)	T_{ST}	-65 °C to +150 °C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4: Recommended Operating Conditions (Voltages are with respect to ground.)

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	-40	—	85	° C

Table 5: Electrical Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units
Interference Margin		SNR	-11	–	–	dB
Receiver Dynamic Range		–	-36	–	0	dB
Digital Outputs - Low	(I_{OL} = 1.6 mA	V_{OL}	–	–	0.4	V
	(I_{OL} = 10 µA)	V_{OL}	–	0.2	–	V
Digital Outputs - High	(I_{OH} = 0.4 mA	V_{OH}	2.4	–	–	V
	(I_{OH} < 10 µA)	V_{OH}	–	4.5	–	V
Digital Inputs - High		V_{IH}	2.0	–	–	V
Digital Inputs - Low		V_{IL}	–	–	0.8	V
Supply Current (from VCC supply)[2]	All zeros	I_{CC}	–	15	22	mA
	All ones	I_{CC}	–	–	23	mA
Driver Leakage Current (V_{DVR} = 18 V)		I_{LL}	–	–	100	µA
Driver Pulse Amplitude (Driver output I_O = 20 mA)		A_P	0.65	–	0.95	V

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Measured with $C_{LOAD} \leq 10$ pF, $R_{LOAD} > 100$ kΩ.

Figure 3: Digital Timing Characteristics

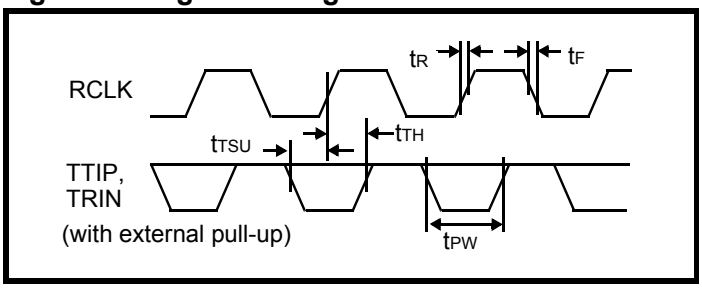


Table 6: Digital Timing Characteristics (Over Recommended Range) see Figure 3

Parameter	Symbol	Min	Typ[1]	Max	Units
Driver Pulse Width	t_{PW}	299	324	349	ns
Driver Pulse Imbalance	–	–	–	15	ns
Rise and Fall Time (any digital output[2])	t_R / t_F	–	–	18	ns
Setup Time - TTIP/TRING to RCLK	t_{TSU}	90	–	–	ns
Hold Time - TTIP/TRING from RCLK	t_{TH}	90	–	–	ns

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Measured with $C_{LOAD} \leq 10$ pF, $R_{LOAD} > 100$ kΩ.

Test Setups

Introduction

Both the LXT312 and LXT315 are fully tested (100% AC and DC parameters) using inputs generated by Level One's proprietary transmission line and network simulator. Device testing includes receiver jitter tolerance, jitter transfer and interference margin, and receiver immunity to gaussian and 60 Hz noise. Specifications and bench test setups are shown in Figures 4 through 11.

Receiver Jitter Tolerance Testing

Receiver jitter tolerance meets the template shown in Figure 4, when operated at line losses from 0 to 36 dB. Figure 6 shows the setup used for jitter tolerance testing.

Receiver Jitter Transfer Testing

Receiver jitter transfer meets the template shown in Figure 5, when operated with line losses from 0 to 36 dB and input jitter amplitude of 0.15 UI peak-to-peak. Jitter gain at a given frequency is defined as the difference between intrinsic jitter and additive jitter at the measurement frequency, divided by the amplitude of the input jitter. Figure 7 shows the setup used for jitter transfer testing.

Figure 4: Receiver Jitter Tolerance Template

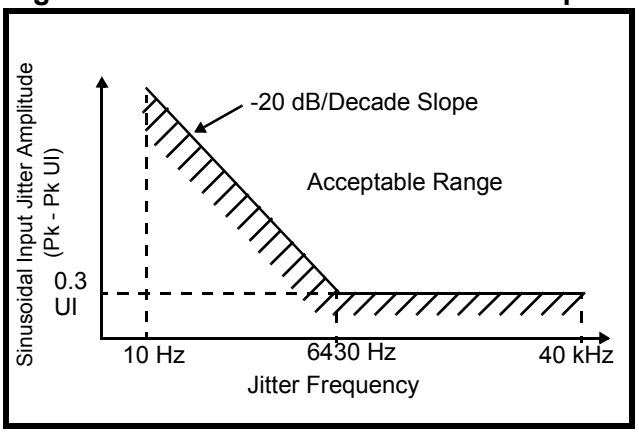


Figure 5: Receiver Jitter Transfer Template

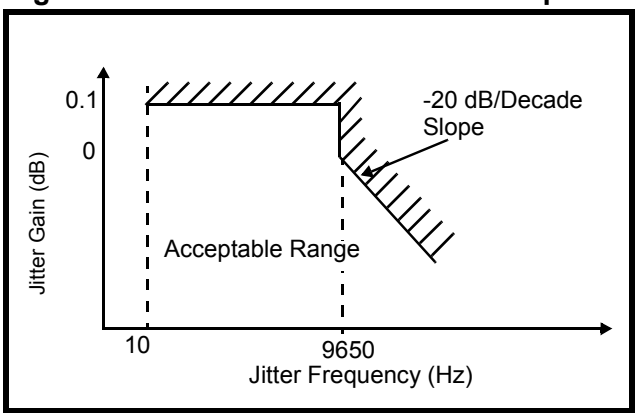


Figure 6: Receiver Jitter Tolerance Test Setup

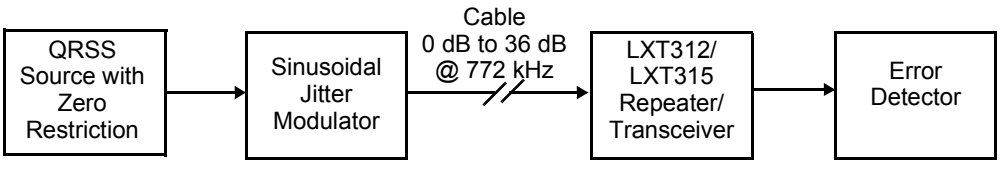
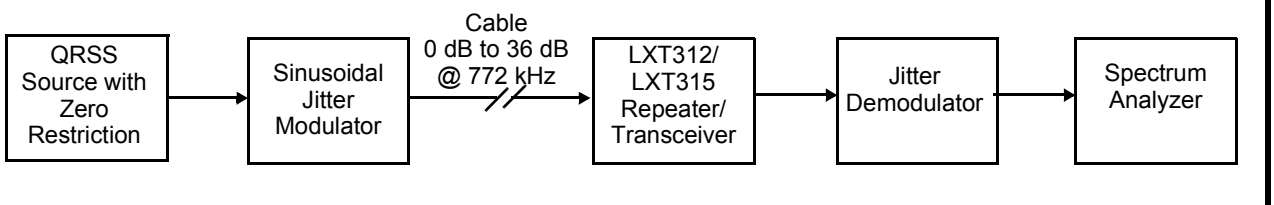


Figure 7: Receiver Jitter Transfer Test Setup



Interference Margin Testing

The LXT312 and LXT315 receiver noise interference margin is specified at a minimum of -11 dB for line losses from 0 dB to 36 dB. The test setup used to measure noise margin is shown in Figure 8.

Gaussian Noise Immunity Testing

Receiver immunity to gaussian noise is specified at a maximum BER of 10^{-7} for a quasi-random T1 signal at 1.544 MHz (±130 ppm). The receiver must be immune to noise power expressed as Np = -(L + 4.7) dBm, where L corresponds to the line loss and is valid for 0 to 36 dB.

Figure 9 shows the setup used to test gaussian noise immunity. The noise source is gaussian to at least 6 sigma and filtered to simulate expected noise in a binder group (per AT&T TA #24/CB113).

60 Hz Pulse Modulation Immunity Testing

Receiver immunity to 60 Hz pulse amplitude modulation is specified using the gaussian noise source described in the previous paragraph on gaussian noise immunity. Pulse amplitude modulation is specified between 10% and 30% of the nominal amplitude (see AT&T TA #24/CB113 for details on the modulation envelope). Figure 10 shows the setup used for testing receiver immunity to 60 Hz pulse amplitude modulation. The following data reflect noise power for 10^{-7} BER at each modulation level, where L corresponds to the line loss and is valid for 0 to 36 dB:

Modulation Level	Noise Power
10%	Np = -(L + 5.7) dBm
20%	Np = -(L + 6.7) dBm
30%	Np = -(L + 8.7) dBm

Receiver Timing Recovery Testing

Receiver timing recovery phase shift modulation for repetitive 8-bit patterns is specified at less than 0.07 UI. This is tested using any two out of 35 possible 8-bit patterns and measuring the change in output pulse timing from one pattern to the other (see AT&T TA #24/CB113 for details on the patterns). Switching rate from one pattern to the other is specified at between 300 Hz and 500 Hz. The setup used to test receiver timing recovery phase shift modulation is shown in Figure 11.

Figure 8: Receiver Noise Interference Margin Test Setup

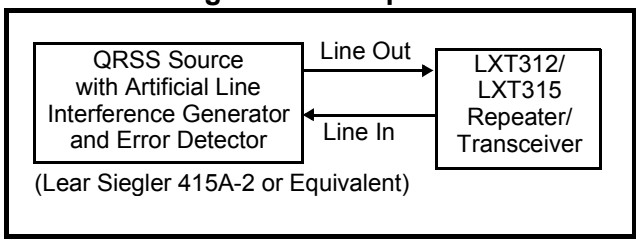


Figure 9: Receiver Gaussian Noise Immunity Test Setup

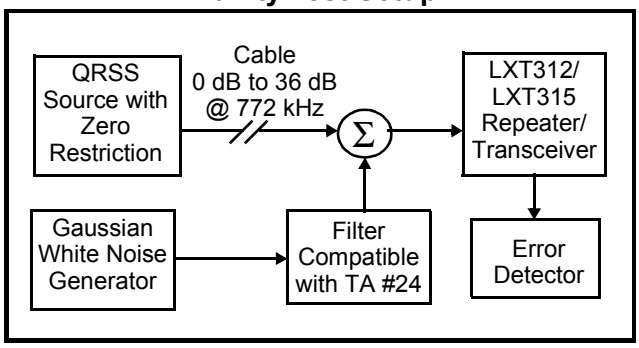


Figure 10: Receiver 60 Hz Pulse Amplitude Modulation Immunity Test Setup

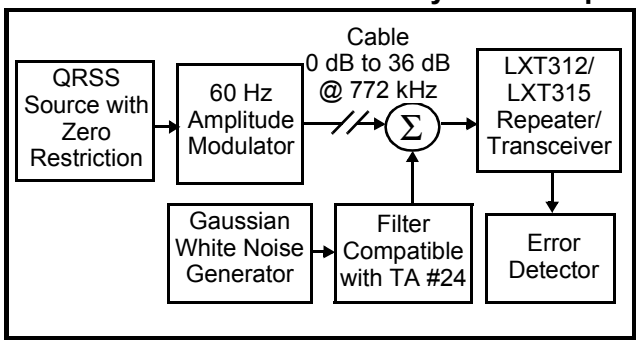
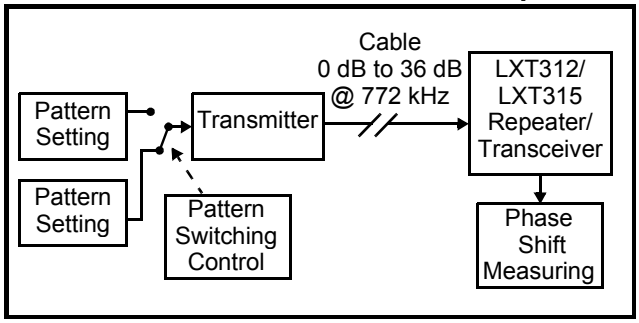


Figure 11: Receiver Timing Recovery Phase Shift Modulation Test Setup



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