LXT903

10Base-T Hub Transceiver

General Description

The LXT903 hub transceiver is designed for use in multi-port repeaters. It interfaces the hub (a multi-port transceiver) to the unshielded twisted-pair media. The LXT903 performs transmit, receive and receive squelch functions. Additional implementations include 10Base-T link integrity testing, automatic correction of receive polarity reversal, and a watchdog timer to jab continuous transmission.

The LXT903 software control mode provides a microprocessor interface with extensive command and status options. The hardware mode provides stand-alone operation.

The LXT903 is an advanced CMOS device and requires only a single 5-volt power supply.

Applications

- Multi-port Repeaters

Features

- Meets or exceeds IEEE 802.3 standards for 10Base-T interface
- Provides predistorted signal to the transmit filter
- Internal programmable squelch circuits
- Detection and correction of reversed polarity
- Microprocessor interface and control
- Differential or single-ended transmit input
- LED driver for jabber, link and reversed polarity
- Single 5 V supply, low-power CMOS technology
- Available in 24-pin DIP and 28-pin PLCC packages

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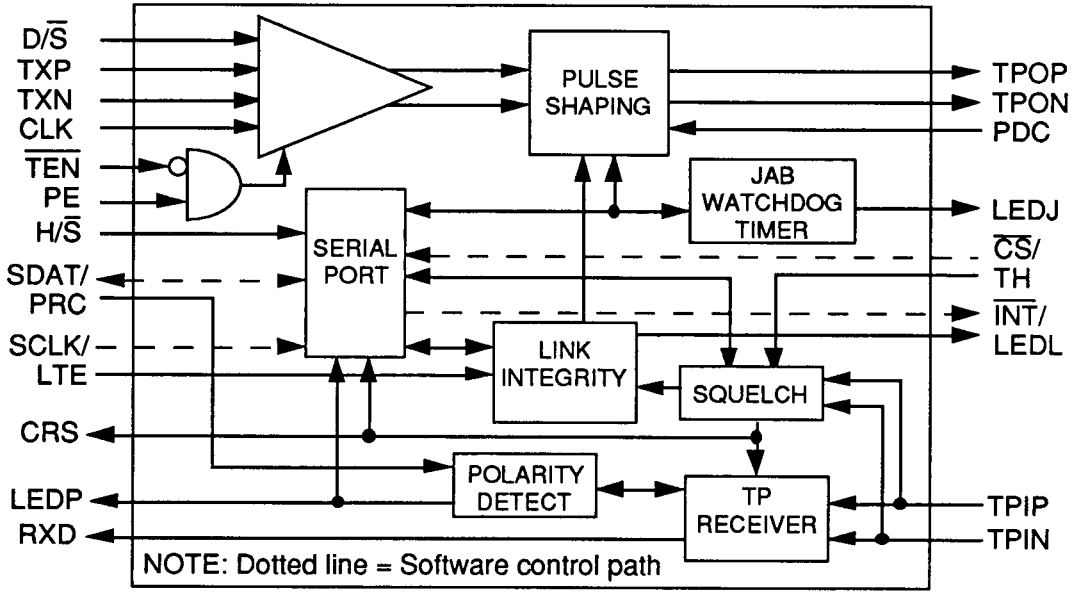
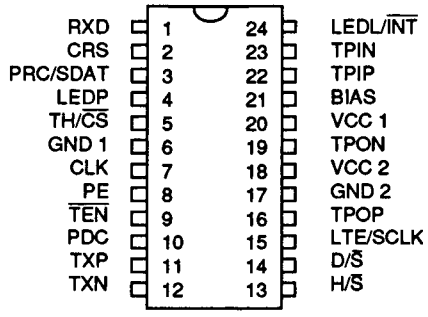
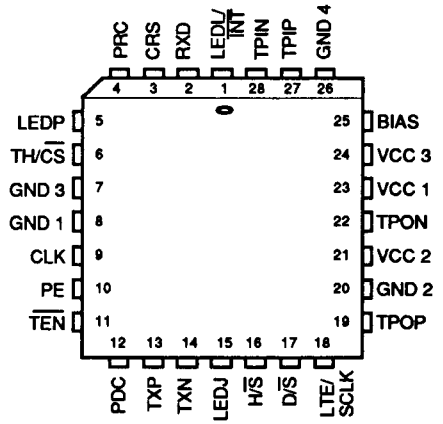
Figure 1: Block Diagram







Pin Descriptions

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
1	2	RXD	O	Receive Data	Data received from the twisted-pair is output to the hub controller DI circuit on this pin as a CMOS level Manchester encoded data stream. High impedance when in software shut down mode.
2	3	CRS	O	Carrier Sense	Goes high to indicate valid receive data. High impedance when in software shut down mode.
3	4	PRC	I	Polarity Reverse Correction *(Hardware Control)*	In the hardware control mode, tying this pin high enables the LXT903 to automatically correct for reversed polarity at the TPI circuit.
		SDAT	I/O	Serial Data *(Software Control)*	In software control mode, this pin is the serial data I/O port.
4	5	LEDP	O	Polarity Reverse	Open drain output. Active low indicates polarity reversed.
5	6	TH	I	Threshold Control *(Hardware Control)*	In hardware mode, forcing this pin low reduces the TP receive squelch by 4.5 dB.
		$\overline{CS}$	I	Chip Select *(Software Control)*	Active low input accesses the serial port in the software mode. $\overline{CS}$ must transition high to low, and remain low for each port operation.
6	8	GND1	–	Ground # 1	Ground.
7	9	CLK	I	Clock	20 MHz CMOS level clock input.
8	10	PE	I	Port Enable	Active CMOS high enables the transmitter. In differential input mode, PE must be high when $\overline{TEN}$ is low to enable transmitter.
9	11	$\overline{TEN}$	I	Transmit Enable	Active CMOS low enables the transmitter when PE is high. Required for differential input mode only.
10	12	PDC	I	Pre-Distortion Control	A CMOS level, synchronous input signal at logic 1 will predistort the output voltage (differential input mode only).
11 12	13 14	TXP TXN	I I	Data Out Positive Data Out Negative	Differential input pair connected to the hub controller DO circuit. When D/$\overline{S}$ pin is tied low, TXP becomes single-ended CMOS level input, synchronous to the 20 MHz CLK.

Pin Descriptions continued

Pin # DIP	Pin # PLCC	Sym	I/O	Name	Description
N/A	15	LEDJ	O	Jabber LED Driver	Open drain driver for the Jabber indicator LED. Goes active when watchdog timer begins jab and stays active until end of the unjab wait period (491 - 525 ms).
13	16	H/$\overline{S}$	I	Hardware/Software Control Select	When set to a logic 0, selects software control mode. When set to a logic 1, selects hardware control mode.
14	17	D/$\overline{S}$	I	Differential/Single-Ended Select	When set to a logic 0, selects single-ended TXP input. When set to a logic 1, selects differential TXP/TXN input.
15	18	LTE	I	Link Test Enable *(Hardware Control)*	In hardware control mode, an active high on this pin enables the link test function.
		SCLK	I	Serial Clock *(Software Control)*	The serial clock required for software control operation is input on this pin. SCLK must be ≤ 2 MHz.
16	19	TPOP	O	Twisted Pair Transmit Outputs	Transmit drivers to the twisted-pair output filter. The output is pre-distorted to meet the 10Base-T template.
19	22	TPON	O		
17	20	GND 2	–	Ground 2	Ground.
N/A	7	GND 3	–	Ground 3	Ground.
N/A	26	GND 4	–	Ground 4	Ground.
18	21	VCC 2	–	Power Supply # 2	+5 V power supply input.
20	23	VCC 1	–	Power Supply # 1	+5 V power supply input.
N/A	24	VCC 3	–	Power Supply # 3	+5 V power supply input.
21	25	BIAS	O	Resistor Bias Control	Bias control for the operating circuit. Bias is set from an external 12.4 kΩ resistor to ground.
22	27	TPIP	I	Twisted-Pair Receive Inputs	Differential receive inputs from the twisted-pair input filter.
23	28	TPIN	I		
24	1	LEDL[1]	O	Link Driver *(Hardware Control)*	LED driver indicates link activity.
		$\overline{INT}$	O	Interrupt *(Software Control)*	The microprocessor interrupt required for software control is output on this pin. The interrupt is an open drain, active low which indicates Jab, Link Failure or Non-correctable Polarity.

[1]LED drivers pull low when active.

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Supply Voltage V_{CC} -0.3 V to 6 V
- Operating temperature T_{OP} 0 °C (min) to +70 °C (max)
- Storage temperature T_{ST} -65 °C (min) to +150 °C (max)

Recommended Operating Conditions (Voltages are with respect to ground unless otherwise specified.)

Parameter	Symbol	Min	Typ[1]	Max	Units
Supply voltage[2]	V_{CC}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	0	-	70	°C

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] Maximum voltage differential between VCC1 and VCC2 (and VCC3 for PLCC parts) must not exceed 0.3V.

I/O Electrical Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage	V_{IL}	–	–	0.8	V	
Input high voltage	V_{IH}	2.0	–	–	V	
Output low voltage (Open drain LED Driver[2])	V_{OL}	–	–	0.7	V	I_{OUT} = 10 mA
Supply current	I_{CC}	-	40	-	mA	Line Idle
		-	75	-	mA	Line Active
Input leakage current[3]	I_{LL}	-	±1	±10	µA	Input between VCC and GND
High Z state leakage current	I_{TS}	-	±1	±10	µA	Output between VCC and GND

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] LED Drivers can sink up to 10 mA of drive current.
[3] Not including TPIN, TPIP, TXN, TXP, PDC, PE, CLK or $\overline{TEN}$.

CMOS I/O Characteristics[1] (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[2]	Max	Units
Input low voltage	V_{CIL}	–	2.0	–	V
Input high voltage	V_{CIH}	–	3.0	–	V
Output low voltage	V_{COL}	–	0	–	V
Output high voltage	V_{COH}	–	5.0	–	V
Input leakage current	I_{CIL}	–	± 1.0	–	µA

[1] Pins TXP, TXN, $\overline{TEN}$, PE, PDC, CLK and RXD.
[2] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Transmit Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	
Peak differential output voltage	V_{OD}	± 4.5	–	± 5.2	V	Load = 200 Ω at TXP/TXN
Differential voltage imbalance	V_{OB}	–	–	± 40	mV	Load = 200 Ω at TXP/TXN
Transmit timing jitter addition	–	–	–	± 8	ns	After Tx filter, 0 line length
Transmit timing jitter addition	–	–	–	± 3.5	ns	After Tx filter and line model specified by IEEE 802.3 for 10Base-T

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

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Receive Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Receive input impedance	Z_{IN}	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	V_{DS}	–	420	–	mV	
Reduced squelch threshold	V_{DSR}	–	250	–	mV	
Receive timing jitter	–	–	–	1.5	ns	

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Switching Characteristics[1] (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Min	Typ	Max	Units
Jabber Timing				
Maximum transmit time	88.5	–	144	ms
Unjab time	442	–	578	ms
Link Integrity Timing				
Time link loss	65	–	66	ms
Time between Link Integrity Pulses	9	–	11	ms
Valid interval for received Link Integrity Pulses	4.1	–	65	ms

Switching Characteristics (Ta = 0 to 70 °C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ	Max	Units
Serial Interface Timing					
SCLK low time	t_{S1}	100	–	–	ns
SCLK high time	t_{S2}	100	–	–	ns
$\overline{CS}$ to SCLK setup time	t_{S3}	50	–	–	ns
SCLK to $\overline{CS}$ hold time	t_{S4}	0	–	–	ns
$\overline{CS}$ inactive time	t_{S5}	50	–	–	ns
SDAT to SCLK setup time	t_{S6}	50	–	–	ns
SCLK to SDAT hold time	t_{S7}	0	–	–	ns
SCLK to SDAT valid	t_{S8}	–	–	100	ns
SCLK falling edge or $\overline{CS}$ rising edge to SDAT high Z	t_{S9}	–	–	100	ns
SCLK rise/fall time	–	–	–	20	ns
Transmit Timing (Single Ended Mode)					
TXP setup time to CLK high	t_{ST1}	20	–	–	ns
TXP hold time from CLK high	t_{ST2}	0	–	–	ns
Transmit Timing (Differential Mode)					
TXP rising edge to PDC rising edge	t_{DT1}	–	50	–	ns
TXP low to PDC low	t_{DT2}	–	0	–	ns
TXP high to TXN low	t_{DT3}	0	–	± 5	ns
TXP low to TXN high	t_{DT4}	0	–	± 5	ns
Receive Timing					
Valid receive data to CRS high	t_{R1}	–	–	500	ns
Receive steady state propagation delay	t_{R2}	–	–	100	ns
Receive turn-off to CRS low	t_{R3}	250	–	400	ns
Receiver jitter	t_{R4}	–	–	± 1.5	ns
CRS high to RXD low	t_{R5}	0	–	100	ns
General					
Receive start-up delay	–	0	–	500	ns
Transmit start-up delay	–	0	–	200	ns
TXP/TXN rise/fall time	t_{TRF}	–	5	–	ns

Figure 2: LXT903 Serial Interface Timing

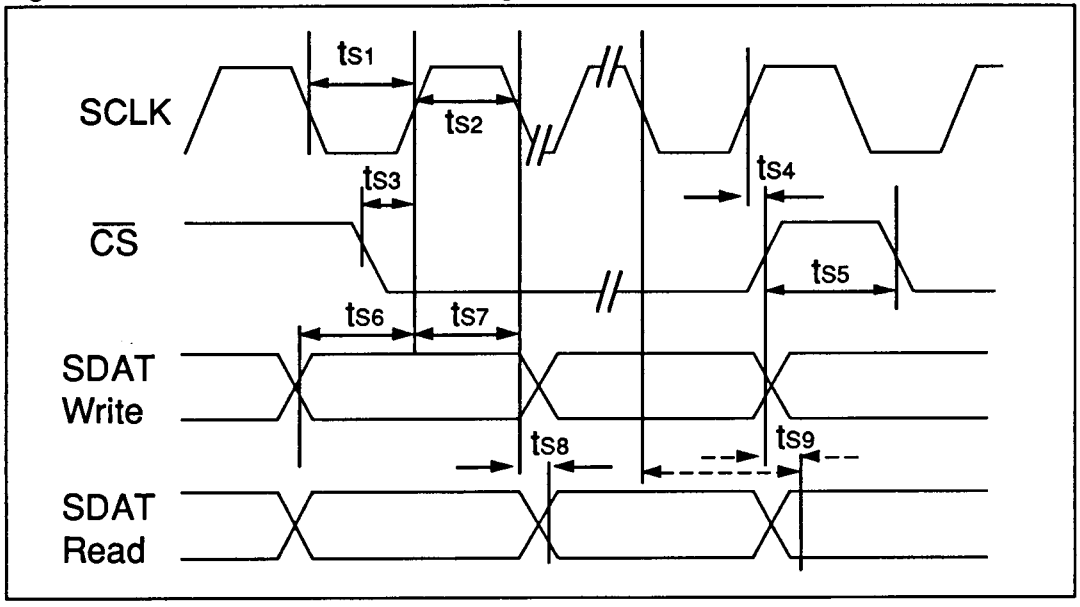


Figure 3: LXT903 Transmit Timing - Single Ended Input Mode

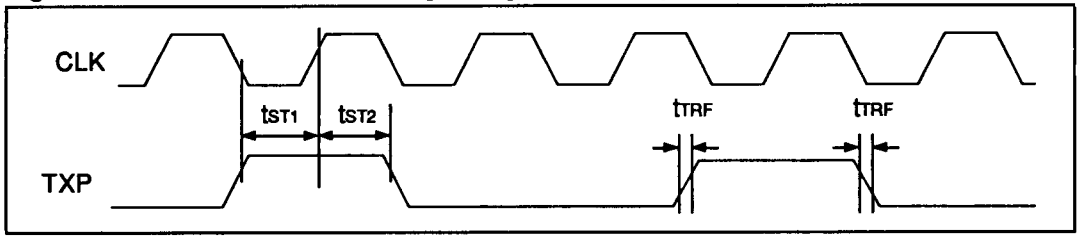


Figure 4: LXT903 Transmit Timing - Differential Input Mode

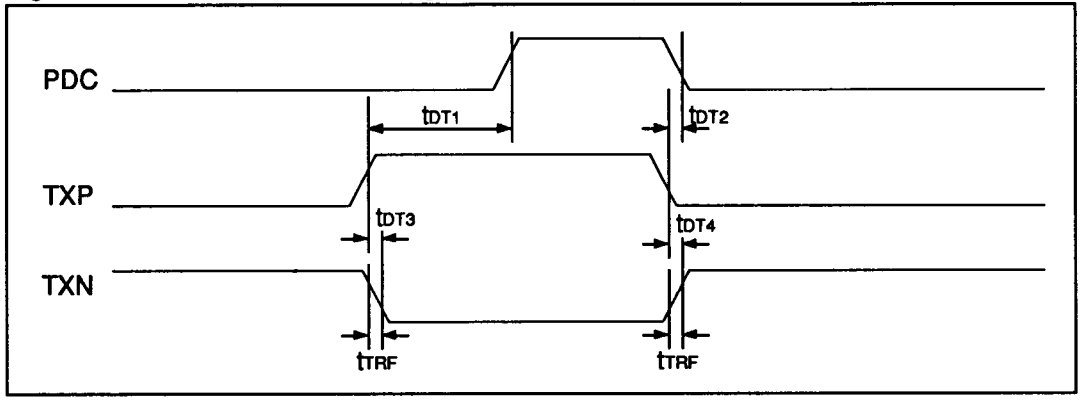
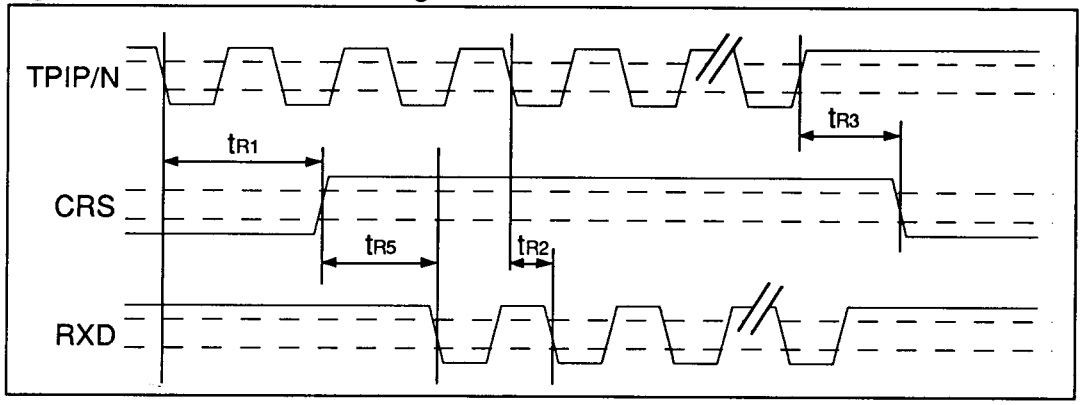


Figure 5: LXT903 Receive Timing



Functional Description

The LXT903 hub transceiver interfaces a hub controller to unshielded twisted-pair cables, transferring data in both directions. The hub side of the interface comprises three circuits: Transmit (the DO output from the hub controller), Receive (the DI input to the hub controller), and Status/ Command. The twisted-pair network side of the interface comprises two circuits: Twisted Pair Input (TPI) and Twisted Pair Output (TPO). In addition to these basic circuits, the LXT903 contains logic controls and LED drivers for status indications.

Functions are defined from the hub side of the interface. The LXT903 Transmit function refers to data transmitted by the hub over the DO circuit to the twisted-pair network. The LXT903 Receive function refers to data received by the hub over the DI circuit from the twisted-pair network. In addition to basic transmit and receive functions, the LXT903 performs some of the MAU functions defined by the IEEE 802.3 10Base-T specification such as link integrity testing and jabber control. The LXT903 also offers extensive software control and status reporting capabilities available through the serial interface.

Transmit Function

The LXT903 transfers manchester encoded, CMOS level data from the hub controller to the twisted-pair network (the TPO circuit). The output signal on TPON and TPOP is predistorted to meet the 10 Base-T jitter template. The output waveform (after the transmit filter) is shown in Figure 6. During idle periods, the LXT903 transmits link integrity test pulses on the TPO circuit. Transmitter inputs can be differential or single-ended, as selected by the D/$\overline{S}$ pin. The differential input is TXP/TXN. Single-ended input is supplied by TXP.

Single Ended Input Mode

The single ended transmit interface consists of TXP, Port Enable (PE) and the 20 MHz clock input (CLK). In the single-ended mode, TXP is sampled before transmission at the 20 MHz clock rate and must meet the specified setup and hold times relative to the CLK input. Predistortion control is generated internally. PE must be high for transmission to occur. Transmission begins at the first low-going data on TXP. End of Frame is detected when TXP is held high for more than 150 ns (plus setup and hold times).

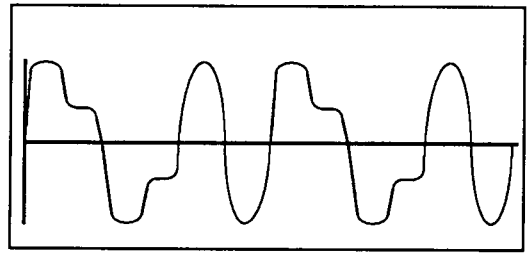
Differential Input Mode

In the differential input mode, the transmit interface consists of TXP and TXN, PE, PDC, and the Transmit Enable input ($\overline{TEN}$). Transmission starts when PE is high and $\overline{TEN}$ is low, and ends when either PE or $\overline{TEN}$ goes inactive. Predistortion control is provided by the PDC input.

Receive Function

The LXT903 receive function accepts serial data from the twisted-pair network (the TPI circuit), converts it to a CMOS level signal, and passes it to the hub controller. An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the receive function. If the differential signal at the TPI circuit

Figure 6: LXT903 TPO Output Waveform

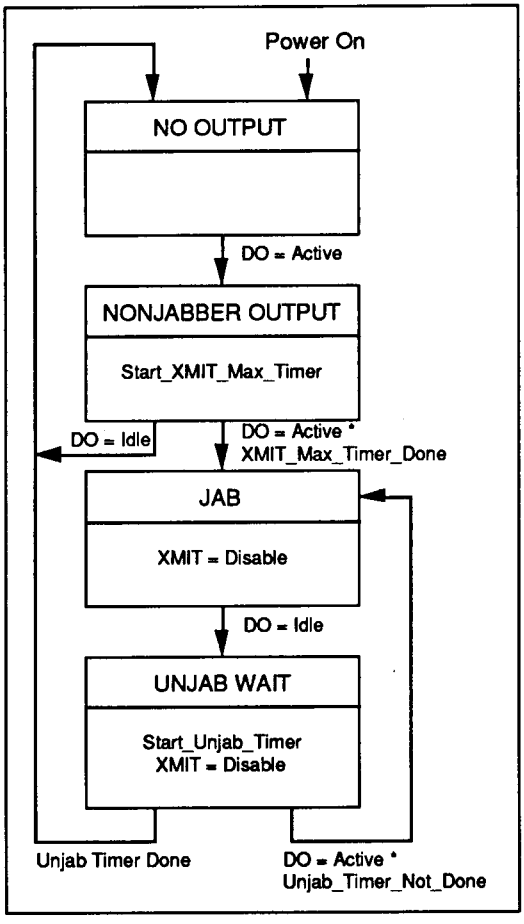


input falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT903 receive function will enter the idle state. A reduced threshold is available which lowers the squelch level by 4.5 dB. Reducing the squelch level extends the network range when used with a low-noise media such as shielded twisted-pair. In the software control mode, the reduced threshold is selected through the serial interface. In the hardware mode, the reduced threshold is selected by tying the TH pin low.

Polarity Reverse Function

The LXT903 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is declared when eight opposite link pulses are received without receipt of a link pulse with the expected polarity. Reversed polarity is also declared if four frames are received with a reversed start-of-idle. Whenever reversed polarity is declared, these two counters are reset to zero. If the LXT903 enters the link fail state and no receive data or link pulses are received within 96 to 128 ms, the polarity is reset to the default (non-flipped) condition. (If Link Integrity is disabled, polarity detection is based only on received data.)

Figure 7: Jabber Control Function



Jabber Control Function

Figure 7 is a state diagram of the LXT903 Jabber control function. In the software mode, jabber control may be disabled through the serial port. In the hardware mode, jabber control is enabled at all times. The LXT903 on-chip watchdog timer prevents the device from locking into a continous transmit mode. When a transmission exceeds the time limit, the Watchdog timer disables the transmit function. Once the LXT903 is in the jabber state, the transmit circuit must remain idle for a period of 491 to 525 ms before it will exit the jabber state.

Link Integrity Test

Figure 8 is a state diagram of the LXT903 Link Integrity Test Function. The Link Integrity Test is used to determine the status of the receive side twisted-pair cable. Link testing is enabled when the LTE pin is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulse is detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit function. The LXT903 ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT903 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses. Link activity is indicated by a low on the LEDL pin.

Hardware Control Mode

In hardware control mode the serial port is not used, and the transceiver is accessed and controlled through individual pins. Hardware control mode is selected when the H/$\overline{S}$ pin is set to a logic 1.

Software Control Mode

To allow a microprocessor to access and control the LXT903 through the serial interface, the H/$\overline{S}$ pin is set to logic 0. The serial interface consists of three signals: the Chip Select input ($\overline{CS}$), the bidirectional Serial Data port (SDAT), and a Serial Clock (SCLK). The LXT903 incorporates a standard microcontroller interface which operates with any standard 8051 using TXD/RXD (port 3) for SCLK and SDAT, and any port for $\overline{CS}$. The SCLK frequency should be 5 MHz or less. In software control mode, the LEDL pin is reconfigured as an interrupt out ($\overline{INT}$). $\overline{INT}$ is an open drain, active low which is set by any of three conditions: Jab, Link Fail, or Non-Correctable Polarity. The $\overline{INT}$ signal stays active until CS goes active (low). The $\overline{INT}$ bit remains set until the first port read cycle. Once set and then cleared, $\overline{INT}$ will not set again until all failure interrupts return to a pass state. The $\overline{INT}$ signal can be masked by bit C4 of the Command word. The serial data (SDAT) is contained in a

16-bit word consisting of an 8-bit Address/Command byte and an 8-bit Command/Status byte. Figure 9 shows the serial interface data structure and timing.

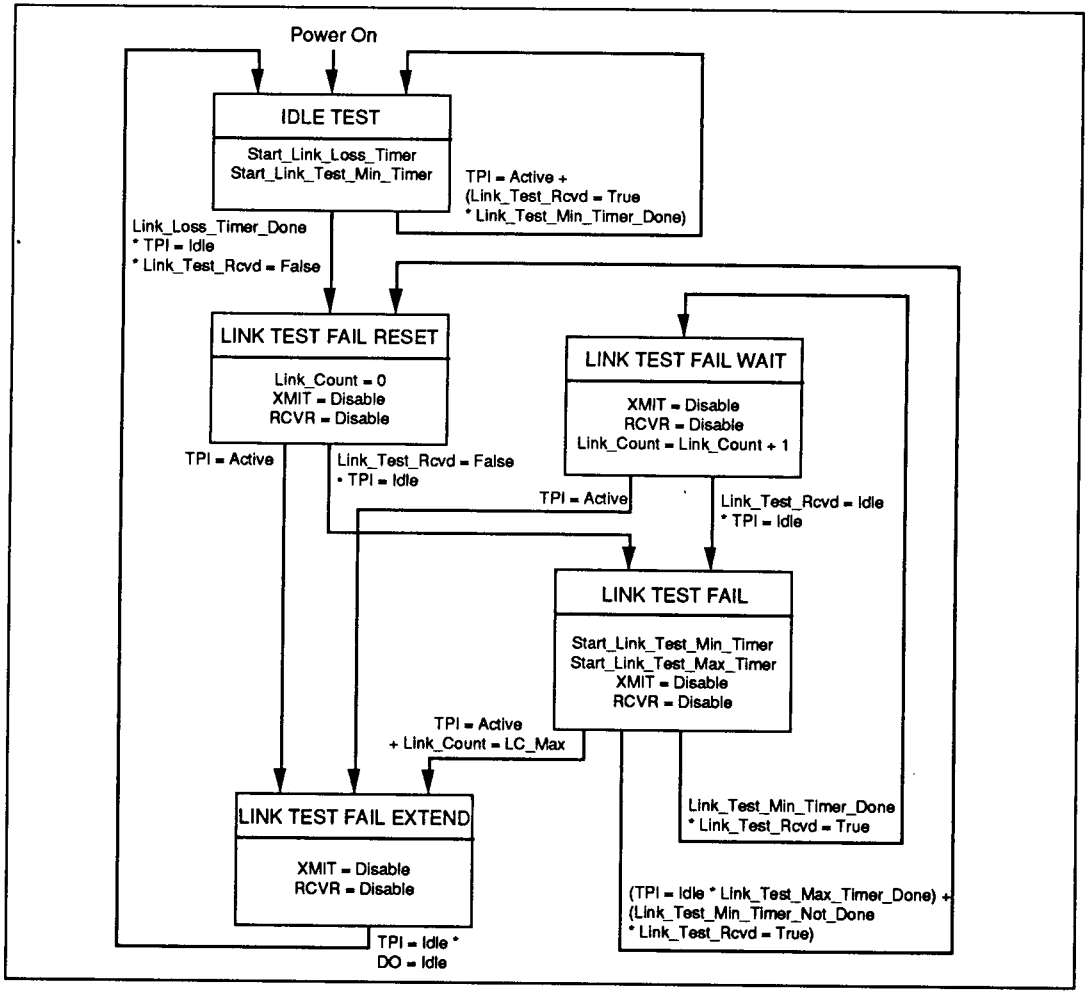
The Address/Command bits are assigned as follows:

AC0	Test Mode. Must be 0 (1 reserved for Factory)
AC1	Address Bit 0. Must be 0 (reserved)
AC2	Address Bit 1. Must be 0 (reserved)
AC3	Address Bit 2. Must be 1 (reserved)
AC4	Read/Write. 1 = Read, 0 = Write
AC5	Must be 0 (reserved)
AC6	Must be 0 (reserved)
AC7	Must be 0 (reserved)

The Command (Write) bits are assigned as follows:

C0	Shut Down (TXP/TXN and TEN are ignored, RXD and CRS go to high impedance. Standard transmit functions are disabled, but Link Pulse reception/transmission continue.)
C1	Link Test Enable/Disable
C2	Jabber Enable/Disable
C3	Polarity Correction Enable
C4	Mask Interrupt (Prevents the open drain $\overline{INT}$ pin from going active.)
C5	Reduced Threshold (Receive threshold reduced by 4.5 dB.)
C6	Must be 0 (reserved)
C7	Must be 0 (reserved)

Figure 8: Link Integrity Test Function

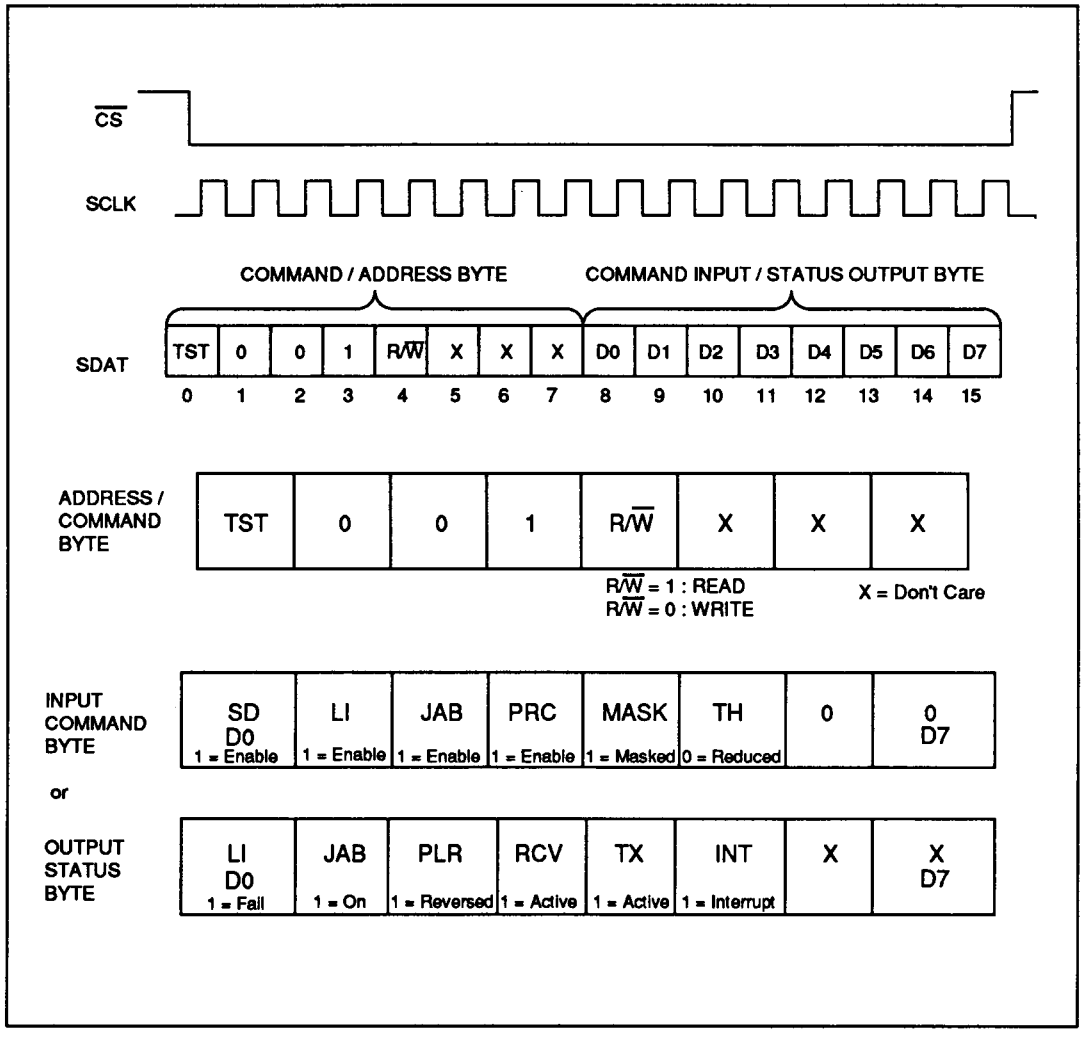


The Status (Read) bits are assigned as follows:

S0 Link Test Fail/Pass
S1 Jabber On/Off
S2 Polarity Reversed/Normal
S3 Receiver Active (Cleared on Read)
S4 Transmitter Active (Cleared on Read)
S5 Interrupt (Cleared on Read)
S6 Don't Care
S7 Don't Care

The LXT903 serial port is accessed by causing the Chip Select ($\overline{CS}$) input to transition from high to low. Bit 4 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation.

Figure 9: LXT903 Serial Interface Data Structure



Applications

Figure 10 shows the LXT903 in a typical hardware control application. The LXT903 hub transceivers interface the Hub Controller to the RJ45 connectors of the twisted pair network. The D/$\overline{S}$ pin is grounded, effecting the single ended mode, so TXN, PDC and $\overline{TEN}$ are not connected. An external source provides the required 20 MHz clock signal. Transmit and receive filters are required in the TPO and TPI circuits. Details of the transmit and receive filters are shown in Figures 11 and 12, respectively. (Differential filters are also recommended.) Integrated filterers such as the Valor PT3877, Fil-Mag 78Z1120B or Pulse Engineering PE65421 may be used. Figure 13 shows a typical software control application, operating in the differential input mode (D/$\overline{S}$ is tied high) with TXN, $\overline{TEN}$, and PDC connected.

Figure 10: Typical LXT903 Hardware Control Application

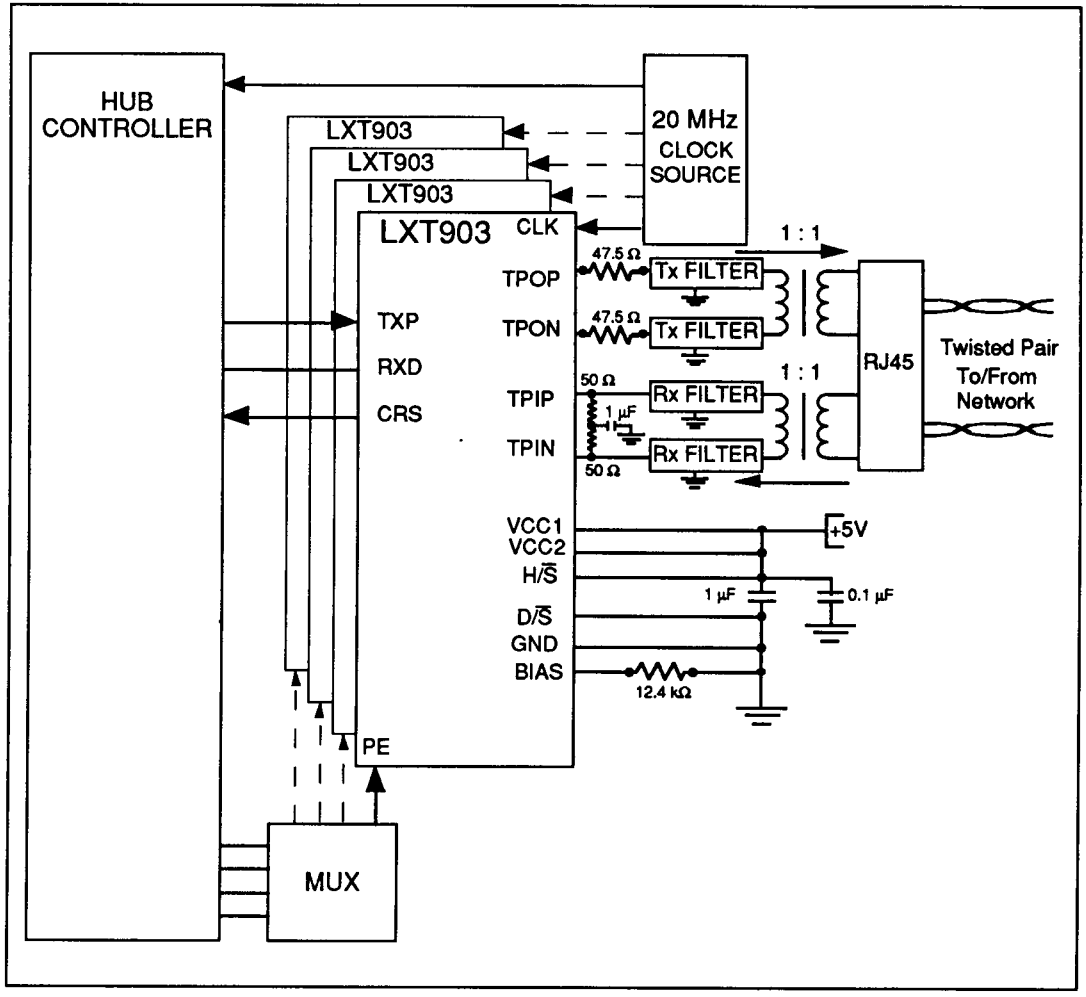


Figure 11: Transmit Filter Diagram

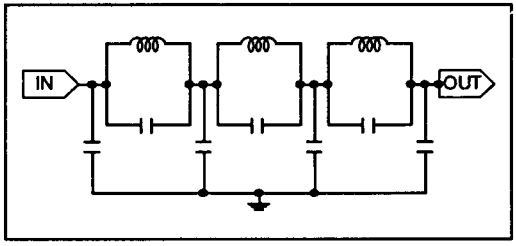


Figure 12: Receive Filter Diagram

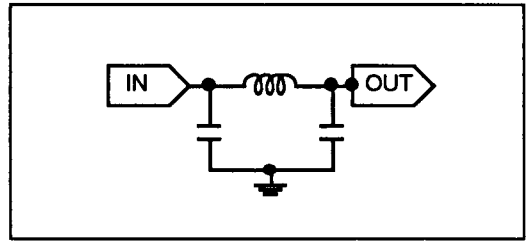


Figure 13: Typical LXT903 Software Control Application