APRIL 2000
Revision 1.2

LXT9763

Fast Ethernet 10/100 Hex Transceiver with Full MII

General Description

The LXT9763 is a six-port PHY Fast Ethernet Transceiver that supports IEEE 802.3 physical layer applications at both 10 and 100 Mbps. The mixed-signal adaptive equalization and clock recovery with proprietary Optimal Signal Processing (OSP™) architecture improves SNR 3 dB over ideal analog filters. All six network ports provide a combination twisted-pair (TP) or pseudo-ECL (PECL) interface for a 10/100BASE-TX or 100BASE-FX connection. The LXT9763 supports both half- and full-duplex operation at 10 and 100 Mbps.

A fully independent Media Independent Interface (MII) for each port provides maximum control for switch and multi-port adapter applications.

In addition to an expanded set of MDIO registers, the LXT9763 provides three discrete LED driver outputs for each port. The LXT9763 requires only a single 3.3V power supply.

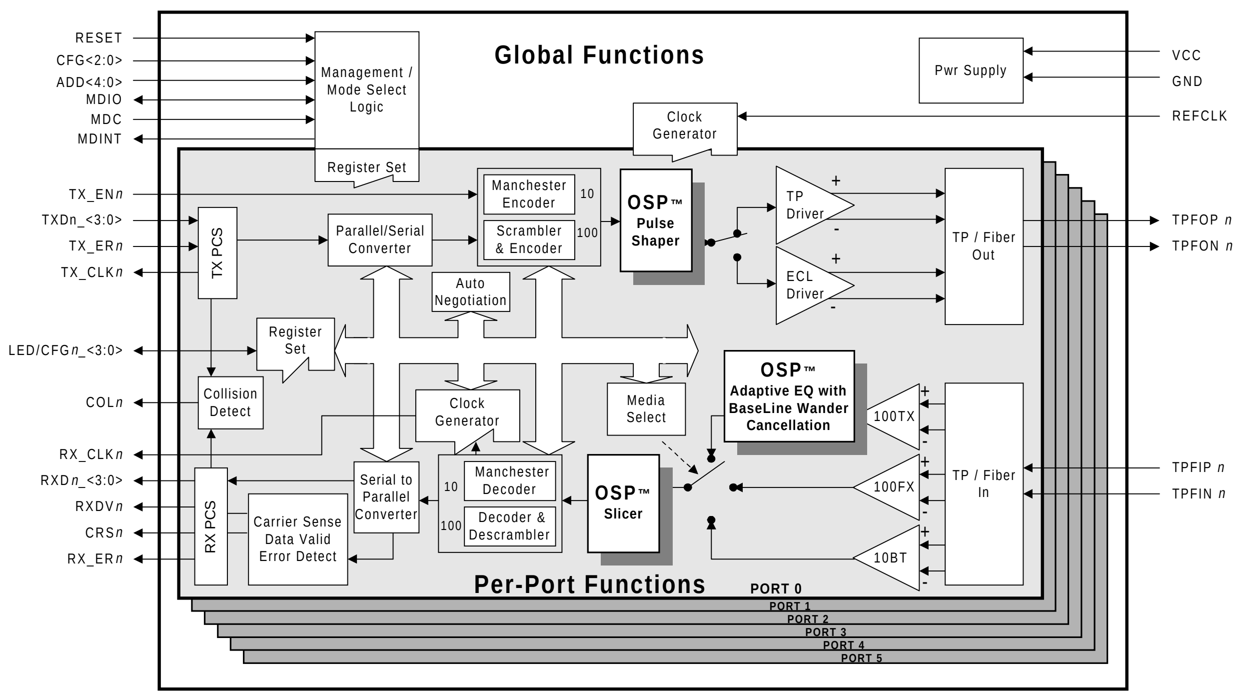
Applications

- 100BASE-T, 10/100-TX, or 100BASE-FX Switches and multi-port NICs.

Features

- Six independent IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports with integrated filters.
- Proprietary Optimal Signal Processing™ (OSP™) architecture improves SNR by 3 dB over ideal analog filters.
- Baseline wander correction for improved 100BASE-TX performance.
- 100BASE-FX fiber-optic capability on all ports.
- Supports both auto-negotiation and legacy systems without auto-negotiation capability.
- JTAG boundary scan.
- Six MII ports for independent PHY port operation.
- Configurable via MDIO port or external control pins.
- Maskable interrupts.
- Very low power 3.3V operation (380 mW per channel, typical).
- 208-pin PQFP (0-70 °C ambient temperature range).

LXT9763 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT9763 Pin Assignments

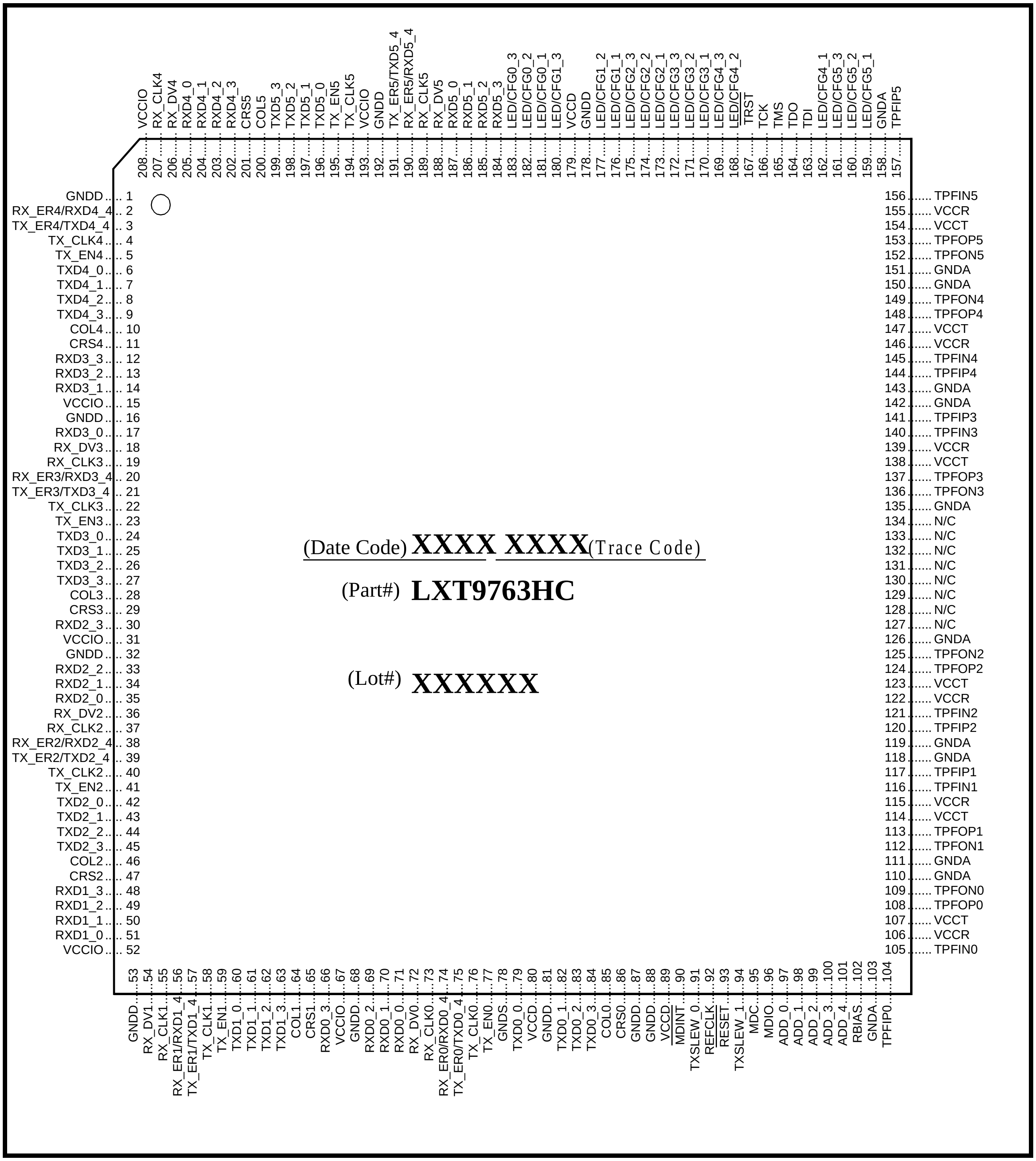


Table 1: LXT9763 MII Signal Descriptions

Pin#	Symbol	Type[1]	Signal Description[2]
			Data Interface Pins
79 82 83 84	TXD0_0 TXD0_1 TXD0_2 TXD0_3	I	**Transmit Data - Port 0**. 4-bit parallel data to be transmitted from port 0 is clocked in synchronously to TX_CLK. In symbol mode (16.11 = 1), the port transmit error signal is re-mapped to provide a fifth data bit.
60 61 62 63	TXD1_0 TXD1_1 TXD1_2 TXD1_3	I	**Transmit Data - Port 1**. 4-bit parallel data to be transmitted from port 1 is clocked in synchronously to TX_CLK. In symbol mode (16.11 = 1), the port transmit error signal is re-mapped to provide a fifth data bit.
42 43 44 45	TXD2_0 TXD2_1 TXD2_2 TXD2_3	I	**Transmit Data - Port 2**. 4-bit parallel data to be transmitted from port 2 is clocked in synchronously to TX_CLK. In symbol mode (16.11 = 1), the port transmit error signal is re-mapped to provide a fifth data bit.
24 25 26 27	TXD3_0 TXD3_1 TXD3_2 TXD3_3	I	**Transmit Data - Port 3**. 4-bit parallel data to be transmitted from port 3 is clocked in synchronously to TX_CLK. In symbol mode (16.11 = 1), the port transmit error signal is re-mapped to provide a fifth data bit.
6 7 8 9	TXD4_0 TXD4_1 TXD4_2 TXD4_3	I	**Transmit Data - Port 4**. 4-bit parallel data to be transmitted from port 4 is clocked in synchronously to TX_CLK. In symbol mode (16.11 = 1), the port transmit error signal is re-mapped to provide a fifth data bit.
196 197 198 199	TXD5_0 TXD5_1 TXD5_2 TXD5_3	I	**Transmit Data - Port 5**. 4-bit parallel data to be transmitted from port 5 is clocked in synchronously to TX_CLK. In symbol mode (16.11 = 1), the port transmit error signal is re-mapped to provide a fifth data bit.
77 59 41 23 5 195	TX_EN0 TX_EN1 TX_EN2 TX_EN3 TX_EN4 TX_EN5	I	**Transmit Enable - Ports 0 - 5**. Active High input enables respective port transmitter. This signal must be synchronous to the TX_CLK.
75 57 39 21 3 191	TX_ER0/TXD0_4 TX_ER1/TXD1_4 TX_ER2/TXD2_4 TX_ER3/TXD3_4 TX_ER4/TXD4_4 TX_ER5/TXD5_4	I	**Transmit Coding Error - Ports 0 - 5**. Valid during 100 Mbps operation only. This signal must be driven synchronously to TX_CLK. When High, forces the respective port to transmit Halt (H) code group. **Transmit Data - Ports 0 - 5**. During symbol mode operation (16.11 = 1), these signals are re-mapped to provide the fifth data bit (TXD*n*_4) for their respective ports (*n*).

1. Type Column Coding: I = Input, O = Output, OD = Open Drain
2. The LXT9763 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 1: LXT9763 MII Signal Descriptions – continued

Pin#	Symbol	Type[1]	Signal Description[2]
76 58 40 22 4 194	TX_CLK0 TX_CLK1 TX_CLK2 TX_CLK3 TX_CLK4 TX_CLK5	O	**Transmit Clock - Ports 0 - 5**. 25 MHz for 100 Mbps operation, 2.5 MHz for 10 Mbps operation. The transmit data and control signals must always be synchronized to TX_CLK by the MAC. The LXT9763 samples these signals on the rising edge of TX_CLK.
71 70 69 66	RXD0_0 RXD0_1 RXD0_2 RXD0_3	O	**Receive Data - Port 0**. Data received at network port 0 is output in 4-bit parallel nibbles, driven synchronously to RX_CLK. In symbol mode (16.11 = 1), the receive error signals are re-mapped to provide a fifth data bit.
51 50 49 48	RXD1_0 RXD1_1 RXD1_2 RXD1_3	O	**Receive Data - Port 1**. Data received at network port 1 is output in 4-bit parallel nibbles, driven synchronously to RX_CLK. In symbol mode (16.11 = 1), the receive error signals are re-mapped to provide a fifth data bit.
35 34 33 30	RXD2_0 RXD2_1 RXD2_2 RXD2_3	O	**Receive Data - Port 2**. Data received at network port 2 is output in 4-bit parallel nibbles, driven synchronously to RX_CLK. In symbol mode (16.11 = 1), the receive error signals are re-mapped to provide a fifth data bit.
17 14 13 12	RXD3_0 RXD3_1 RXD3_2 RXD3_3	O	**Receive Data - Port 3**. Data received at network port 3 is output in 4-bit parallel nibbles, driven synchronously to RX_CLK. In symbol mode (16.11 = 1), the receive error signals are re-mapped to provide a fifth data bit.
205 204 203 202	RXD4_0 RXD4_1 RXD4_2 RXD4_3	O	**Receive Data - Port 4**. Data received at network port 4 is output in 4-bit parallel nibbles, driven synchronously to RX_CLK. In symbol mode (16.11 = 1), the receive error signals are re-mapped to provide a fifth data bit.
187 186 185 184	RXD5_0 RXD5_1 RXD5_2 RXD5_3	O	**Receive Data - Port 5**. Data received at network port 5 is output in 4-bit parallel nibbles, driven synchronously to RX_CLK. In symbol mode (16.11 = 1), the receive error signals are re-mapped to provide a fifth data bit.
86 65 47 29 11 201	CRS0 CRS1 CRS2 CRS3 CRS4 CRS5	O	**Carrier Sense - Ports 0 - 5**. On detection of valid carrier (either transmit or receive in half-duplex; receive only in full-duplex), these signals are asserted asynchronously with respect to RX_CLK. CRS is deasserted on loss of carrier, synchronous to RX_CLK.
85 64 46 28 10 200	COL0 COL1 COL2 COL3 COL4 COL5	O	**Collision - Ports 0 - 5**. Active High indication of simultaneous receive and transmit activity. These signals are asserted asynchronously with respect to RX_CLK. These signals are inactive during full-duplex operation.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain
2. The LXT9763 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 1: LXT9763 MII Signal Descriptions – continued

Pin#	Symbol	Type[1]	Signal Description[2]
72 54 36 18 206 188	RX_DV0 RX_DV1 RX_DV2 RX_DV3 RX_DV4 RX_DV5	O	**Receive Data Valid - Ports 0 - 5**. These signals are synchronous to the respective RX_CLK*n*. Active High indication that received code group maps to valid data. During 10M operation, RX_DVn is asserted with the first nibble of the Start-of-Frame Delimiter (SFD) “5D” and remains asserted until the end of the packet.
74 56 38 20 2 190	RX_ER0/RXD0_4 RX_ER1/RXD1_4 RX_ER2/RXD2_4 RX_ER3/RXD3_4 RX_ER4/RXD4_4 RX_ER5/RXD5_4	O	**Receive Error - Ports 0 - 5**. These signals are synchronous to the respective RX_CLK. Active High indicates that received code group is invalid, or that PLL is not locked. During 10M operation, active High indicates that the received data is invalid (SFD = A2 rather than 5D.) **Receive Data - Ports 0 - 5**. During symbol mode operation (16.11 = 1), these signals are re-mapped to provide the fifth data bit (RXD*n*_4) for their respective ports.
73 55 37 19 207 189	RX_CLK0 RX_CLK1 RX_CLK2 RX_CLK3 RX_CLK4 RX_CLK5	O	**Receive Clock - Ports 0 - 5**. This continuous recovered clock provides the reference for RXD, RX_DV and RX_ER signals. 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
MII Control Interface Pins			
95	MDC	I	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 8 MHz.
96	MDIO	I/O	**Management Data Input/Output**. Bidirectional serial data channel for PHY/STA communication.
90	$\overline{\text{MDINT}}$	OD	**Management Data Interrupt**. When bit 18.1 = 1, an active Low output on this pin indicates status change. Interrupt is cleared by reading Register 19.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain
2. The LXT9763 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 2: LXT9763 Network Interface Signal Descriptions

Pin#	Symbol	Type[1]	Signal Description
108, 109 113, 112 124, 125 137, 136 148, 149 153, 152	TPFOP0, TPFON0 TPFOP1, TPFON1 TPFOP2, TPFON2 TPFOP3, TPFON3 TPFOP4, TPFON4 TPFOP5, TPFON5	O	**Twisted-Pair/Fiber Outputs, Positive & Negative - Ports 0-5.** During 100BASE-TX or 10BASE-T operation, TPFO pins drive 802.3 compliant pulses onto the line. During 100BASE-FX operation, TPFO pins produce differential PECL outputs for fiber transceivers.
104, 105 117, 116 120, 121 141, 140 144, 145 157, 156	TPFIP0, TPFIN0 TPFIP1, TPFIN1 TPFIP2, TPFIN2 TPFIP3, TPFIN3 TPFIP4, TPFIN4 TPFIP5, TPFIN5	I	**Twisted-Pair/Fiber Inputs, Positive & Negative - Ports 0-5.** During 100BASE-TX or 10BASE-T operation, TPFI pins receive differential 100BASE-TX or 10BASE-T signals from the line. During 100BASE-FX operation, TPFI pins receive differential PECL inputs from fiber transceivers.

1. Type Column Coding: I = Input, O = Output.

Table 3: LXT9763 Miscellaneous Signal Descriptions

<table>
<tr><th>Pin#</th><th>Symbol</th><th>Type[1]</th><th colspan="3">Signal Description[2]</th></tr>
<tr><td rowspan="6">91
94</td><td rowspan="6">TxSLEW_0
TxSLEW_1</td><td rowspan="6">I</td><td colspan="3">Tx Output Slew Controls 0 and 1. These pins select the TX output slew rate (rise and fall time) as follows:</td></tr>
<tr><td>TxSLEW_1</td><td>TxSLEW_0</td><td>Slew Rate (Rise and Fall Time)</td></tr>
<tr><td>0</td><td>0</td><td>2.5 ns</td></tr>
<tr><td>0</td><td>1</td><td>3.1 ns</td></tr>
<tr><td>1</td><td>0</td><td>3.7 ns</td></tr>
<tr><td>1</td><td>1</td><td>4.3 ns</td></tr>
<tr><td>93</td><td>$\overline{\text{RESET}}$</td><td>I</td><td colspan="3">Reset. This active Low input is OR’ed with the control register Reset bit (0.15). When held Low, output pins go to inactive state.</td></tr>
<tr><td>101
100
99
98
97</td><td>ADD_4
ADD_3
ADD_2
ADD_1
ADD_0</td><td>I
I
I
I
I</td><td colspan="3">Address <4:0>. Sets base address. Each port adds its port number to this address to determine its PHY address.
Port 0 Address = Base + 0.
Port 1 Address = Base + 1.
Port 2 Address = Base + 2.
Port 3 Address = Base + 3.
Port 4 Address = Base + 4.
Port 5 Address = Base + 5.</td></tr>
</table>

1. Type Column Coding: I = Input, O = Output, A = Analog.
2. The LXT9763 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 3: LXT9763 Miscellaneous Signal Descriptions – continued

Pin#	Symbol	Type[1]	Signal Description[2]
102	RBIAS	I	**Bias**. This pin provides bias current for the internal circuitry. Must be tied to ground through a 22.1 kΩ, 1% resistor.
92	REFCLK	I	**Reference Clock**. A 25 MHz clock is required at this pin.
127-134	N/C	-	**No Connection**. These pins should be left floating.

1. Type Column Coding: I = Input, O = Output, A = Analog.
2. The LXT9763 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 4: LXT9763 Power Supply Signal Descriptions

Pin#	Symbol	Type	Signal Description
107, 114, 123, 138, 147, 154	VCCT	-	**Transmitter Supply.** +3.3V supply for analog circuits.
106, 115, 122, 139, 146, 155	VCCR	-	**Receiver Supply.** +3.3V supply for analog circuits.
80, 89, 179	VCCD	-	**Digital Power Supply - Core.** +3.3V supply for core digital circuits.
15, 31, 52, 67, 193, 208	VCCIO	-	**Digital Power Supply - I/O Ring.** 3.3V supply for digital I/O circuits. Regardless of the IO supply, digital I/O pins remain tolerant of 5V signal levels.
1, 16, 32, 53, 68, 81, 87, 88, 178, 192	GNDD	-	**Digital Ground**. Ground return for both core and I/O digital supplies (VCCD and VCCIO).
103, 110, 111, 118, 119, 126, 135, 142, 143, 150, 151, 158	GNDA	-	**Analog Ground**. Ground return for analog supply.
78	GNDS	-	**Substrate Ground**. Ground for chip substrate.

Table 5: LXT9763 JTAG Test Signal Descriptions

Pin#	Symbol	Type[1]	Signal Description
163	TDI	I / IP	**Test Data Input**. Test data sampled with respect to the rising edge of TCK.
164	TDO	O	**Test Data Output**. Test data driven with respect to the falling edge of TCK.
165	TMS	I / IP	**Test Mode Select**.
166	TCK	I / ID	**Test Clock**. Clock for JTAG test (REFCLK).
167	$\overline{\text{TRST}}$	I / IP	**Test Reset**. Reset input for JTAG test.

1. Type Column Coding: I = Input, O = Output, A = Analog, IP = weak internal pull-up, ID = weak internal pull-down.

Table 6: LXT9763 LED Signal Descriptions

Pin#	Symbol	Type[1]	Signal Description
181 182 183	LED/CFG0_1 LED/CFG0_2 LED/CFG0_3	I/OD/OS	**Port 0 LED Drivers 1 -3.** These pins drive LED indicators for Port 0. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 65 for details). **Port 0 Configuration Inputs 1-3.** These pins also provide initial configuration settings (refer to Table 7 on page 16 for details).
176 177 180	LED/CFG1_1 LED/CFG1_2 LED/CFG1_3	I/OD/OS	**Port 1 LED Drivers 1 -3.** These pins drive LED indicators for Port 1. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 65 for details). **Port 1 Configuration Inputs 1-3.** These pins also provide initial configuration settings (refer to Table 7 on page 16 for details).
173 174 175	LED/CFG2_1 LED/CFG2_2 LED/CFG2_3	I/OD/OS	**Port 2 LED Drivers 1 -3.** These pins drive LED indicators for Port 2 Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 65 for details). **Port 2 Configuration Inputs 1-3.** These pins also provide initial configuration settings (refer to Table 7 on page 16 for details).
170 171 172	LED/CFG3_1 LED/CFG3_2 LED/CFG3_3	I/OD/OS	**Port 3 LED Drivers 1 -3.** These pins drive LED indicators for Port 3. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 65 for details). **Port 3 Configuration Inputs 1-3.** These pins also provide initial configuration settings (refer to Table 7 on page 16 for details).
162 168 169	LED/CFG4_1 LED/CFG4_2 LED/CFG4_3	I/OD/OS	**Port 4 LED Drivers 1 -3.** These pins drive LED indicators for Port 4. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 65 for details). **Port 4 Configuration Inputs 1-3.** These pins also provide initial configuration settings (refer to Table 7 on page 16 for details).
159 160 161	LED/CFG5_1 LED/CFG5_2 LED/CFG5_3	I/OD/OS	**Port 5 LED Drivers 1 -3.** These pins drive LED indicators for Port 5. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 51 on page 65 for details). **Port 5 Configuration Inputs 1-3.** These pins also provide initial configuration settings (refer to Table 7 on page 16 for details).

1. Type Column Coding: I = Input, O = Output, OD = Open Drain, OS = Open Source.

FUNCTIONAL DESCRIPTION

Introduction

The LXT9763 six-port Fast Ethernet 10/100 Transceiver supports 10 Mbps and 100 Mbps networks. It complies with all applicable requirements of IEEE 802.3. Each port directly drives either a 100BASE-TX line (up to 100 meters) or a 10BASE-T line (up to 185 meters). The LXT9763 also supports 100BASE-FX operation via a Pseudo-ECL (PECL) interface.

OSP™ Architecture

Level One's LXT9763 incorporates high-efficiency Optimal Signal Processing™ design techniques, combining the best properties of digital and analog signal processing to produce a truly optimal device.

The receiver utilizes decision feedback equalization to increase noise and cross-talk immunity by as much as 3 dB over an ideal all-analog equalizer. Using OSP mixed-signal processing techniques in the receive equalizer avoids the quantization noise and calculation truncation errors found in traditional DSP-based receivers (typically complex DSP engines with A/D converters). This results in improved receiver noise and cross-talk performance.

The OSP signal processing scheme also requires substantially less computational logic than traditional DSP-based designs. This lowers power consumption and also reduces the logic switching noise generated by high-speed DSP engines. This logic switching noise can be a considerable source of EMI generated on the device's power supplies.

The OSP-based LXT9763 provides improved data recovery, EMI performance, and power consumption.

Comprehensive Functionality

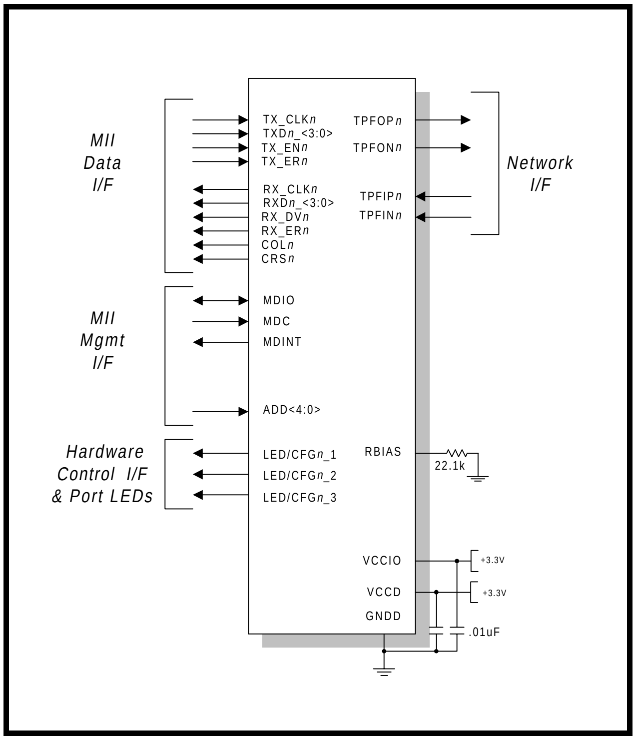
The LXT9763 provides six standard Media Independent Interfaces (MIIs) for 10/100 MACs, each serving an individual network port. The LXT9763 performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X specification. This device also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

On power-up, the LXT9763 reads its configuration pins to check for forced operation settings. If not configured for forced operation, each port uses auto-negotiation/parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT9763 auto-negotiates with it using Fast Link Pulse (FLP) bursts. If the PHY partner does not support auto-negotiation, the LXT9763 automatically detects the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and set its operating conditions accordingly.

The LXT9763 provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

Interface Descriptions

Figure 2: LXT9763 Interfaces



10/100 Network Interface

The LXT9763 supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair, or 100 Mbps Ethernet over fiber media (100BASE-FX). Each of the six network interface ports consists of four external pins (two differential signal pairs). The pins are shared between twisted-pair (TP) and fiber. Refer to Table 2 on page 8 for specific pin assignments.

The LXT9763 output drivers generate either 100BASE-TX, 10BASE-T, or 100BASE-FX output. When not transmitting data, the LXT9763 generates 802.3-compliant link pulses or idle code. Input signals are decoded either as a 100BASE-TX, 100-BASE-FX, or 10BASE-T input, depending on the mode selected. Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface.

Twisted-Pair Interface

When operating at 100 Mbps, the LXT9763 continuously transmits and receives MLT3 symbols. When not transmitting data, the LXT9763 generates “IDLE” symbols.

During 10 Mbps operation, Manchester-encoded data is exchanged. When no data is being exchanged, the line is left in an idle state.

The LXT9763 supports either 100BASE-TX or 10BASE-T connections over 100Ω, Category 5, Unshielded Twisted Pair (UTP) cable. Only a transformer, RJ-45 connector, series capacitors and load resistor, and bypass capacitors are required to complete this interface. On the receive side, the internal impedance is high enough that it has no practical effect on the external termination circuit. On the transmit side, Level One's patented waveshaping technology shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings (refer to Table 3 on page 8) allow the designer to match the output waveform to the magnetic characteristics.

Fiber Interface

The LXT9763 provides a PECL interface that complies with the ANSI X3.166 specification. This interface is suitable for driving a fiber-optic coupler. Fiber ports cannot be enabled via auto-negotiation; they must be enabled via the MDIO interface.

Configuration Management Interface

The LXT9763 provides both an MDIO interface and a hardware control interface (via the LED/CFG pins) for device configuration and management.

MDIO Management Interface

The LXT9763 supports the IEEE 802.3 MII Management Interface also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT9763. The MDIO interface consists of a physical connection, a specific protocol that runs across the connection, and an internal set of addressable registers.

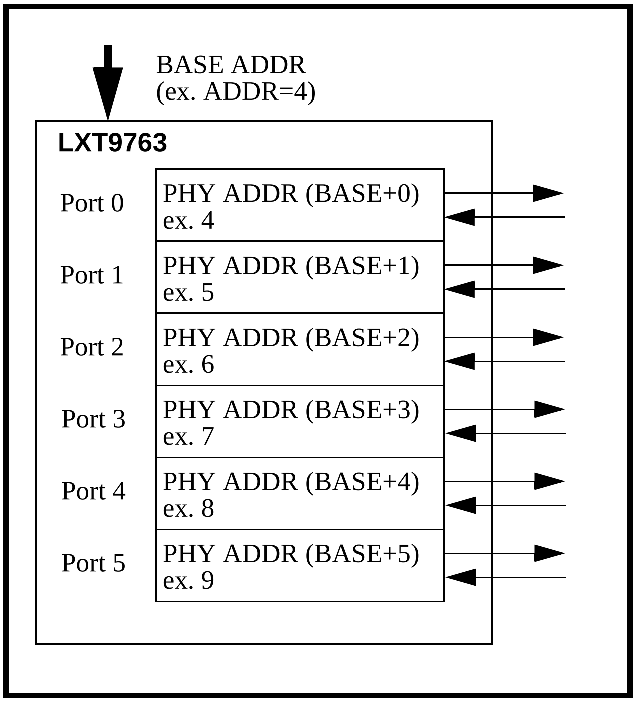
Some registers are required and their functions are defined by the IEEE 802.3 specification. The LXT9763 also supports additional registers for expanded functionality. The LXT9763 supports 12 internal registers per port (48 total), each of which is 16 bits wide. Specific register bits are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).

The physical interface consists of a data line (MDIO) and clock line (MDC). The timing for the MDIO Interface is shown in Table 33 on page 49. MDIO read and write cycles are shown in Figures 4 (read) and 5 (write).

MII Addressing

The protocol allows one controller to communicate with multiple LXT9763 chips. Pins ADD_<4:0> determine the base address. Each port adds its port number to the base address to obtain its port address as shown in Figure 3.

Figure 3: Port Address Scheme



MII Interrupts

The LXT9763 provides a single interrupt pin available to all ports. Interrupt logic is shown in Figure 6. The LXT9763 also provides two dedicated interrupt registers for each port. Register 18 provides interrupt enable and mask functions and Register 19 provides interrupt status. Setting bit 18.1 = 1, enables a port to request interrupt via the MDINT pin. An active Low on this pin indicates a status change on the LXT9763. However, because it is a shared interrupt, it does not indicate which port is requesting service. Interrupts may be caused by one of four conditions:

- Auto-negotiation complete
- Speed status change
- Duplex status change
- Link status change

Figure 4: Management Interface Read Frame Structure

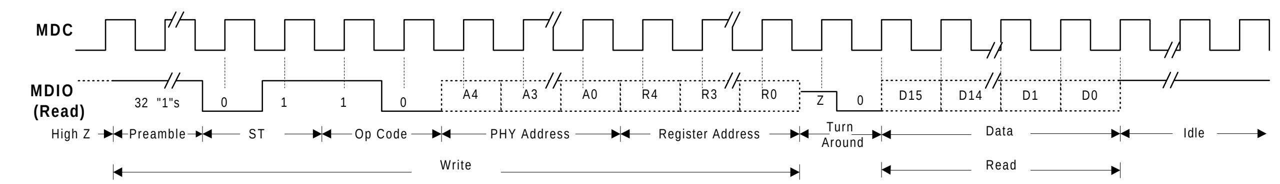


Figure 5: Management Interface Write Frame Structure

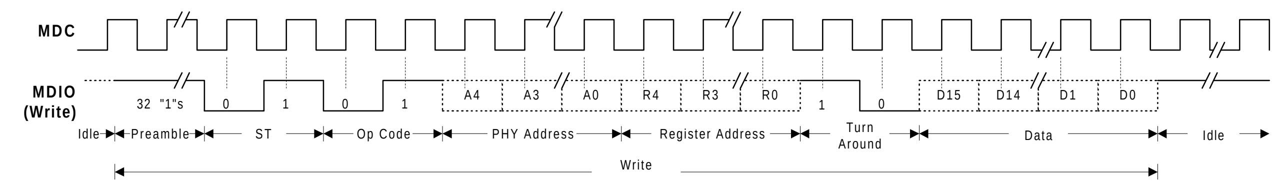
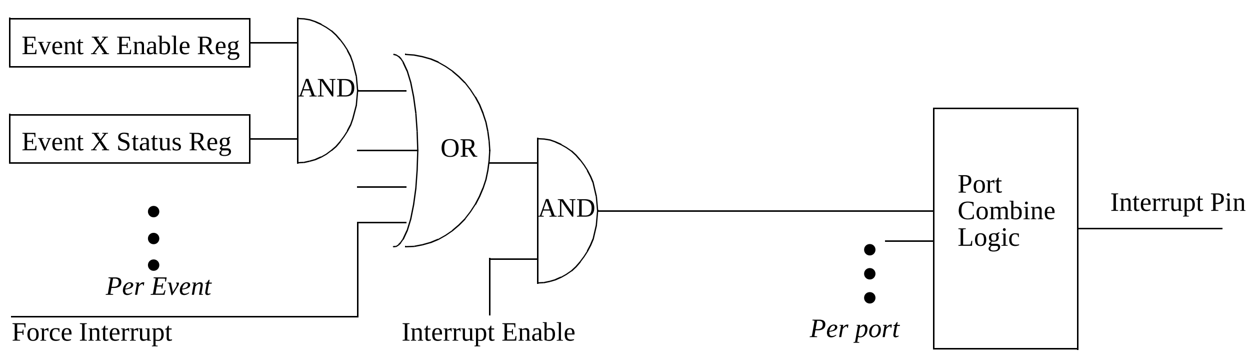


Figure 6: Interrupt Logic



1. Interrupt (Event) Status Register is cleared on read.
2. X = Any Interrupt capability

Hardware Control Interface

The LXT9763 provides a Hardware Control Interface for applications where the MDIO is not desired. The Hardware Control Interface consists of three Configuration (CFG) pins for each port. The CFG pins double as LED drivers. Refer to "Hardware Configuration Settings" on page 16 for additional details.

MII Data Interface

The LXT9763 supports six standard MIIs (one per port). The MII consists of a data interface and a management interface. The MII Data Interface passes data between the LXT9763 and one or more Media Access Controllers (MACs). Separate parallel buses are provided for transmit and receive. This interface operates at either 2.5 MHz or 25 MHz. The speed is set automatically, once the operating conditions of the network link have been determined.

Operating Requirements

Power Requirements

The LXT9763 requires four power supply inputs, VCCD, VCCR, VCCT, and VCCIO. The digital and analog circuits require 3.3 V supplies (VCCD, VCCR and VCCT). These inputs may be supplied from a single source although decoupling is required to each respective ground.

An additional supply may be used for the MII (VCCIO). VCCIO should be supplied from the same power source used to supply the controller on the other side of the MII interface. Refer to Table 17 on page 36 for MII I/O characteristics.

As a matter of good practice, these supplies should be as clean as possible. Typical filtering and decoupling are shown in Figure 16 on page 32.

Clock Requirements

Reference Clock

The LXT9763 requires a constant 25 MHz reference clock (REFCLK) that must be enabled at all times. Refer to Test Specifications, Table 18 on page 36, for REFCLK requirements.

MII Clocks

The LXT9763 requires an MDC reference clock for the MDIO serial channel. Typically operated at 2.5 MHz, the LXT9763 accepts MDC clocks as high as 8 MHz. Refer to Test Specifications, Table 18 on page 36, for MDC clock requirements.

The LXT9763 supplies both MII data clocks (RX_CLK and TX_CLK) for each port. The MII data clocks run at 25 MHz for 100BASE-X operation and at 2.5 MHz for 10BASE-T operation.

Initialization

When the LXT9763 is first powered on, reset, or encounters a link failure state, it checks the MDIO register configuration bits to determine the line speed and operating conditions to use for the network link. The configuration bits may be set by the Hardware Control or MDIO interface as shown in Figure 7.

The LXT9763 can be initialized to allow auto-negotiation/ parallel-detection to establish a link, or it may be forced to any of the following configurations:

- 100FX (Fiber).
- 100TX, Full-Duplex
- 100TX, Half-Duplex
- 10BASE-T, Full-Duplex
- 10BASE-T, Half-Duplex

When the network link is forced to a specific configuration, the LXT9763 immediately begins operating the network interface as commanded. When auto-negotiation is enabled, the LXT9763 begins the auto-negotiation / parallel-detection operation.

Power-Down Mode

The LXT9763 provides a per-port Power-Down Mode. Individual port power-down control is provided by bit 0.11 in the respective port Control Registers (refer to Table 38 on page 54). During individual port power-down, the following conditions are true:

- The individual port is shut down.
- The MDIO registers remain accessible.
- The MDIO registers are unaffected.

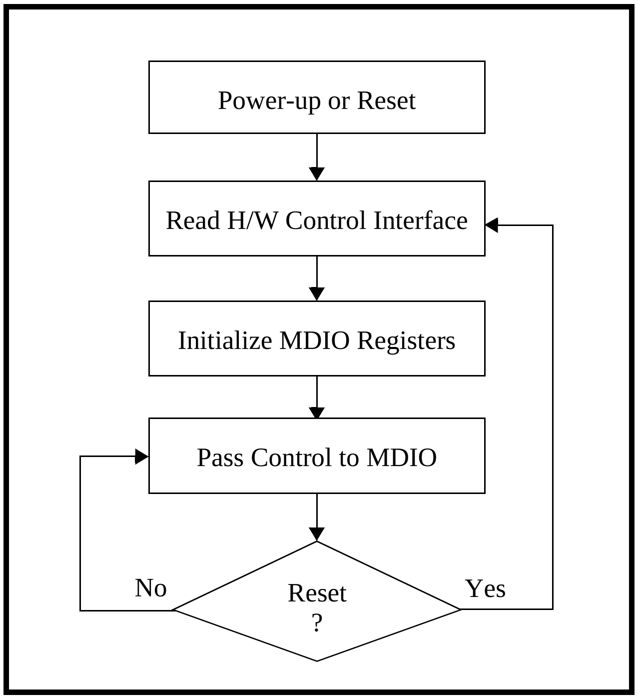
Reset

The LXT9763 provides both hardware and software resets. Configuration control of Auto-Negotiation, speed and duplex mode selection is handled differently for each. During a hardware reset, settings for bits 0.13, 0.12 and 0.8 are read in from the pins (refer to Table 7 on page 16 for pin settings and Table 38 on page 54 for register bit definitions).

During a software reset (0.15 = 1), these bit settings are not re-read from the pins. They revert back to the values that were read in during the last hardware reset. Therefore, any changes to pin values made since the last hardware reset will not be detected during a software reset.

During a hardware reset, register information is unavailable for 1 ms after de-assertion of the reset. During a software reset (0.15 = 1) the registers are available for reading. The reset bit should be polled to see when the part has completed reset (0.15 = 0).

Figure 7: Initialization Sequence



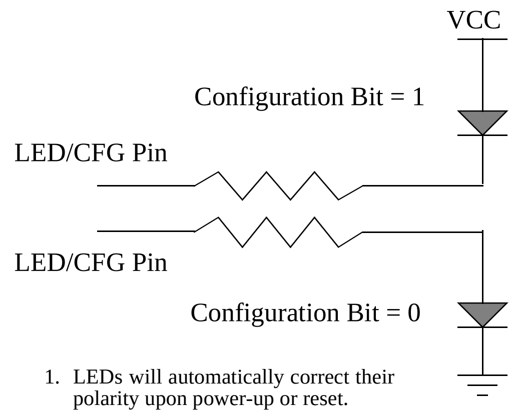
Hardware Configuration Settings

The LXT9763 provides a hardware option to set the initial device configuration. The hardware option uses the three LED/CFG pins for each port. This provides three control bits per port, as listed in Table 7. The LED drivers can operate as either open drain or open source circuits as shown in Figure 8. The LED pins are sensitive to polarity and will automatically pull up or pull down to configure for either open drain or open source circuits (10 mA max current rating) as required by the hardware configuration. In applications where all ports are configured the same, several pins may be tied together with a single resistor.

NOTE

Fiber operation cannot be selected via hardware. Fiber operation must be enabled via the MDIO port.

Figure 8: Hardware Configuration Settings



1. LEDs will automatically correct their polarity upon power-up or reset.

.

Table 7: Hardware Configuration Settings

Desired Configuration			Pin Settings			Resulting Register Bit Values						
			LED/CFG*n*_[1]			Control Register			AN Advertisement Register			
AutoNeg Mode	Speed Mode	Duplex Mode	1	2	3	AutoNeg 0.12	Speed 0.13	FD 0.8	100FD 4.8	100TX 4.7	10 FD 4.6	10T 4.5
Disabled	10	Half	0	0	0	0	0	0	X X X X[2] Auto-Negotiation Advertisement			
		Full	0	0	1			1				
	100	Half	0	1	0		1	0				
		Full	0	1	1			1				
Enabled[3]	100	Half	1	0	0	1	1	0	0	1	0	0
		Full	1	0	1			1	1			
	10/100	Half	1	1	0			0	0		0	1
		Full	1	1	1			1	1		1	

1. These pins set the default values for registers 0 and 4 accordingly.
2. X = Don't Care.
3. Do not select Fiber mode with Auto-Negotiation enabled.

Establishing Link

See Figure 9 for an overview of link establishment.

Auto-Negotiation

The LXT9763 attempts to auto-negotiate with its counterpart across the link by sending Fast Link Pulse (FLP) bursts. Each burst consists of 33 link pulses spaced 62.5 µs apart. Odd link pulses (clock pulses) are always present. Even link pulses (data pulses) may be present or absent to indicate a “1” or a “0”. Each FLP burst exchanges 16 bits of data, which are referred to as a “page”. All devices that support auto-negotiation must implement the “Base Page” defined by IEEE 802.3 (registers 4 and 5). LXT9763 also supports the optional ‘Next Page’ function (registers 7 and 8).

Base Page Exchange

By exchanging Base Pages, the LXT9763 and its link partner communicate their capabilities to each other. Both sides must receive at least three identical base pages for negotiation to proceed. Each side finds the highest common capabilities that both sides support. Both sides then exchange more pages, and finally agree on the operating state of the line.

Next Page Exchange

Additional information, above that required by base page exchange is also sent via “Next Pages’. The LXT9763 fully supports the 802.3 method of negotiation via Next Page exchange.

Controlling Auto-Negotiation

When auto-negotiation is controlled by software, the following steps are recommended:

- After power-up, power-down, or reset, the power-down recovery time, (see Table 34 on page 50), must be exhausted before proceeding.
- Set the auto-negotiation advertisement bits.
- Enable auto-negotiation (set MDIO bit 0.12 = 1).

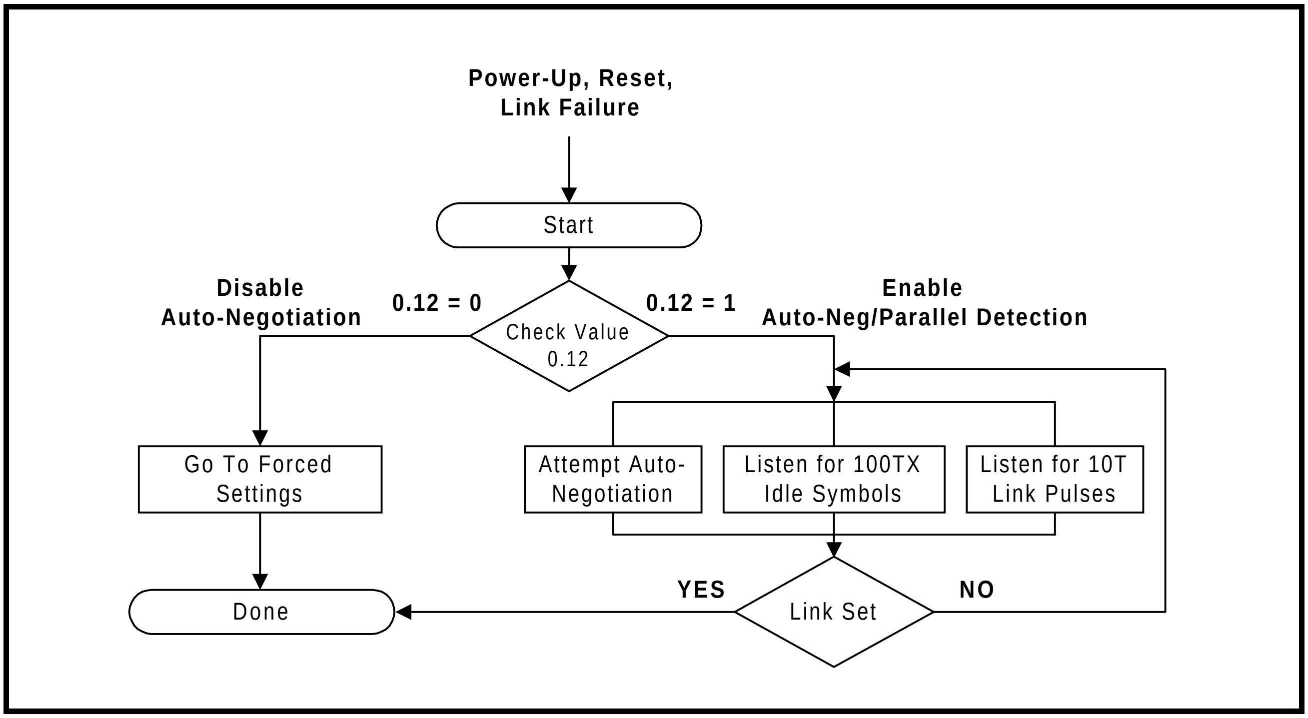
NOTE

Do not enable Auto-Negotiation if fiber mode is selected.

Parallel Detection

In parallel with auto-negotiation, the LXT9763 also monitors for 10 Mbps Normal Link Pulses (NLP) or 100 Mbps Idle symbols. If either is detected, the device automatically reverts to the corresponding operating mode. Parallel detection allows the LXT9763 to communicate with devices that do not support auto-negotiation.

Figure 9: Overview of Link Establishment

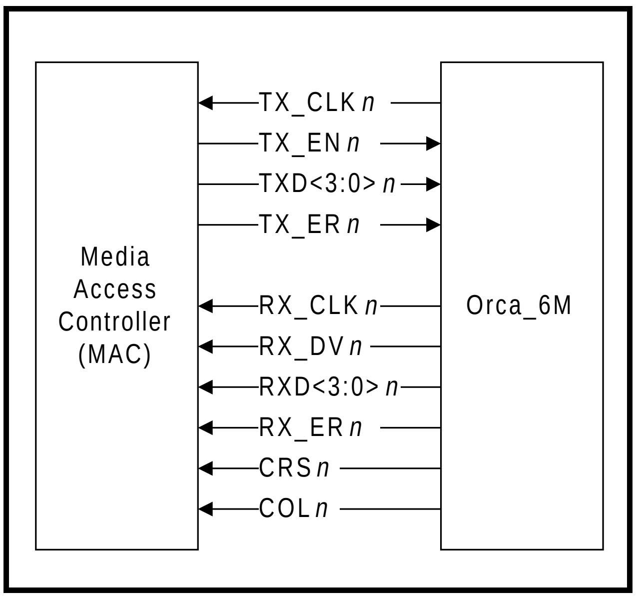


MII Operation

Figure 10 is a simple block diagram of the MII data interface. Separate channels are provided for transmitting data from the MAC to the LXT9763 (TXD), and for passing data received from the line to the MAC (RXD). Each channel has its own clock, data bus, and control signals. Nine signals are used to pass received data to the MAC: RXD<3:0>, RX_CLK, RX_DV, RX_ER, COL and CRS. Seven signals are used to transmit data from the MAC: TXD<3:0>, TX_CLK, TX_EN, and TX_ER. The LXT9763 supplies both transmit and receive clock signals as well as separate outputs for carrier sense and collision.

Data is normally exchanged across the MII in 4-bit-wide nibbles. However, two alternative data exchange methods are provided. A 5-bit symbol mode is available via bit 16.11 for 100M operation. Refer to Table 47 on page 61 for additional information on these bit settings.

Figure 10: MII Data Interface



Transmit Clock

The LXT9763 is the master clock source for data transmission. It automatically sets the speed of TX_CLK to match port conditions. If the port is operating at 100 Mbps, TX_CLK will be set to 25 MHz. If the port is operating at 10 Mbps, TX_CLK will be set to 2.5 MHz. The transmit data and control signals must always be synchronized to TX_CLK by the MAC. The LXT9763 samples these signals on the rising edge of TX_CLK.

Transmit Enable

The MAC must assert TX_EN synchronously with the first nibble of preamble, and de-assert TX_EN after the last bit of the packet.

Receive Data Valid

The LXT9763 asserts RX_DV when it receives a valid packet. Timing changes depend on line operating speed:

- For 100TX links, RX_DV is asserted from the first nibble of preamble to the last nibble of the data packet.
- For 10BT links, the entire preamble is truncated. RX_DV is asserted with the first nibble of the Start-of-Frame Delimiter (SFD) “5D” and remains asserted until the end of the packet.

Error Signals

Whenever the LXT9763 receives an errored symbol from the network, it asserts RX_ER and drives “1110” on the RXD pins. RX_ER is synchronous with RX_CLK.

When the MAC asserts TX_ER, the LXT9763 will drive “H” symbols out on the line. TX_ER must be synchronous with TX_CLK.

Carrier Sense

Carrier sense (CRS) is an asynchronous output. It is always generated when a packet is received from the network and in some modes when a packet is transmitted.

On transmit, CRS is asserted on a 10 Mbps or 100 Mbps half-duplex link. Carrier sense is not generated on transmit when the link is operating in full-duplex mode.

Collision

The LXT9763 asserts its collision signal, asynchronously to any clock, whenever the line state is half-duplex and the transmitter and receiver are active at the same time. Table 8 summarizes the conditions for assertion of carrier sense, collision, and data loopback signals.

Loopback

The LXT9763 provides two loopback functions, operational and test (see Table 8).

Operational Loopback

Operational loopback is provided for 10 Mbps half-duplex links when bit 16.8 = 0. Data transmitted by the MAC (TXData) will be looped back on the receive side of the MII (RXData). Operational loopback is not provided for 100 Mbps links, full-duplex links, or when 16.8 = 1.

Test Loopback

A test loopback function is provided for diagnostic testing of the LXT9763. During test loopback, twisted-pair and fiber interfaces are disabled. Data transmitted by the MAC is internally looped back by the LXT9763 and returned to the MAC.

Test loopback is available for 100TX, 100FX, and 10T operation. Test loopback is enabled by setting bit 0.14 = 1, bit 0.8 = 1 (full-duplex), and bit 0.12 = 0 (disable auto-negotiation). Loopback paths are shown in Figure 11.

Figure 11: Loopback Paths

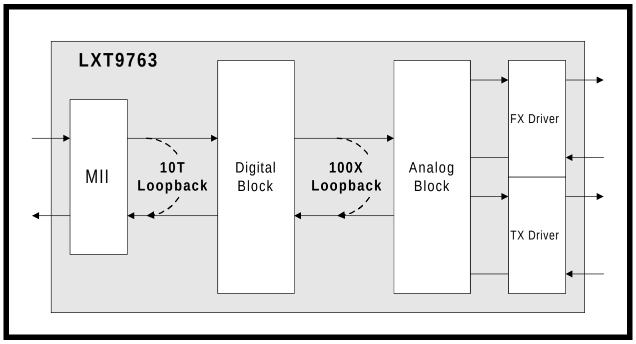


Table 8: Carrier Sense, Loopback, and Collision Conditions

Speed	Duplex Condition	Carrier Sense	Test[1] Loopback	Operational Loopback	Collision
100 Mbps	Full-Duplex	Receive Only	Yes	No	None
	Half-Duplex	Transmit or Receive	No	No	Transmit and Receive
10 Mbps	Full-Duplex	Receive Only	Yes	No	None
	Half-Duplex, 16.8 = 0	Transmit or Receive	No	Yes	Transmit and Receive
	Half-Duplex, 16.8 = 1	Transmit or Receive	None	No	Transmit and Receive

1. Test Loopback is enabled when 0.14 = 1

100 Mbps Operation

100BASE-X Network Operations

During 100BASE-X operation, the LXT9763 transmits and receives 5-bit symbols across the network link. Figure 12 shows the structure of a standard frame packet. When the MAC is not actively transmitting data, the LXT9763 sends out Idle symbols on the line.

As shown in Figure 12, the MAC starts each transmission with a preamble pattern. As soon as the LXT9763 detects the start of preamble, it transmits a J/K Start-of-Stream Delimiter (SSD) symbol to the network. It then encodes and transmits the rest of the packet, including the balance of the preamble, the Start-of-Frame Delimiter (SFD), packet data, and CRC. Once the packet ends, the LXT9763 transmits the T/R End-of-Stream Delimiter (ESD) symbol and then returns to transmitting Idle symbols.

In 100TX mode, the LXT9763 scrambles the data and transmits it to the network using MLT-3 line code. The MLT-3 signals received from the network are descrambled and decoded and sent across the MII to the MAC. Figure 13 shows the internal signal flow between the MII and the network interface.

In 100FX mode, the LXT9763 transmits and receives NRZI signals across the PECL interface. An external 100FX transceiver module is required to complete the fiber connection.

Figure 12: 100BASE-X Frame Format

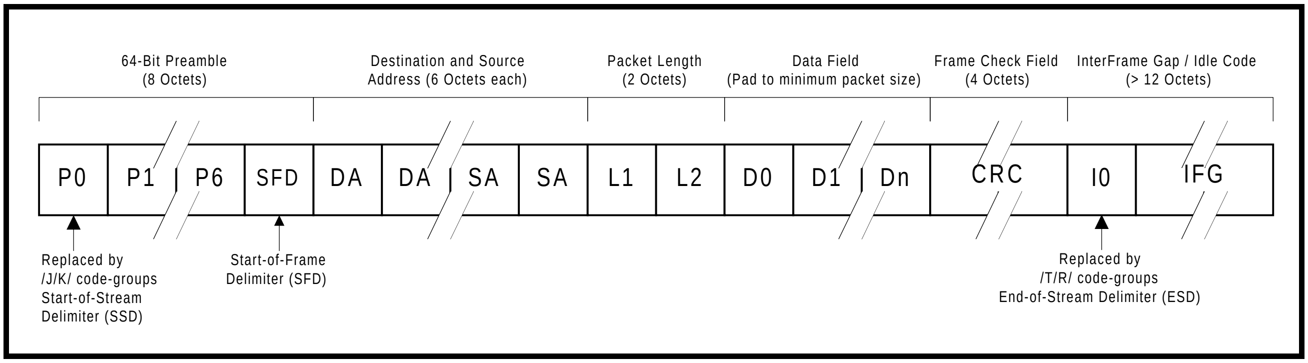
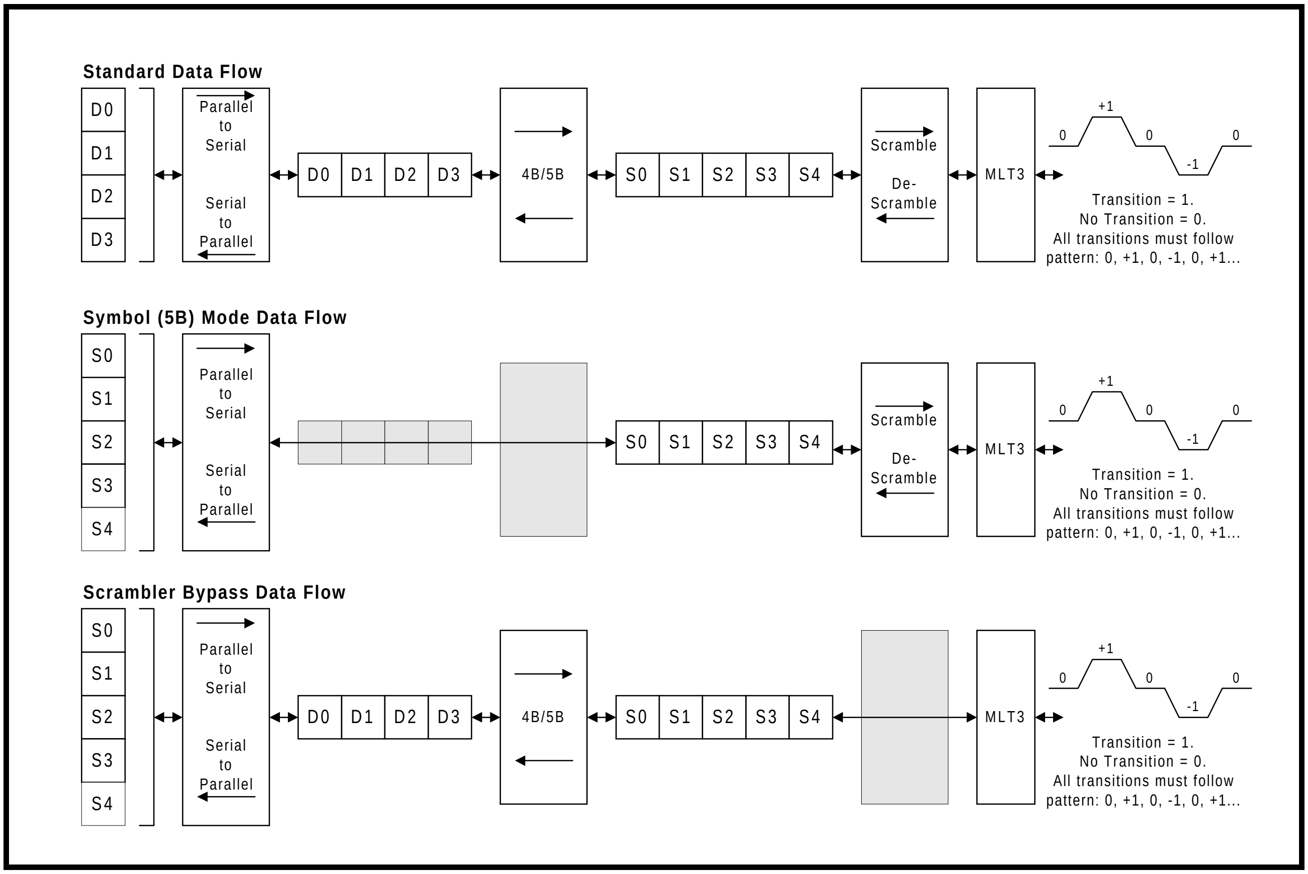


Figure 13: 100BASE-TX Data Path



100BASE-X Protocol Sublayer Operations

With respect to the 7-layer communications model, the LXT9763 is a Physical Layer 1 (PHY) device. The LXT9763 implements the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) sublayers of the reference model defined by the IEEE 802.3u specification. The following paragraphs discuss LXT9763 operation from the reference model point of view.

PCS Sublayer

The Physical Coding Sublayer (PCS) provides the MII interface, as well as the 4B/5B encoding/ decoding function. (For symbol mode operation, the 4B/5B function can be bypassed by setting 16.11 = 1.)

For 100TX and 100FX operation, the PCS layer provides IDLE symbols to the PMD-layer line driver as long as TX_EN is de-asserted.

Preamble Handling

When the MAC asserts TX_EN, the PCS substitutes a /J/K symbol pair, also known as the Start of Stream Delimiter (SSD), for the first two nibbles received across the MII. The PCS layer continues to encode the remaining MII data, following Table 9 on page 23, until TX_EN is de-asserted. It then returns to supplying IDLE symbols to the line driver.

In the receive direction, the PCS layer performs the opposite function, substituting two preamble nibbles for the SSD.

Dribble Bits

The LXT9763 handles dribbles bits in all modes. If between 1-4 dribble bits are received, the nibble is passed across the MII, padded with 1s if necessary. If between 5-7 dribble bits are received, the second nibble is not sent onto the MII bus.

Figure 14: Protocol Sublayers

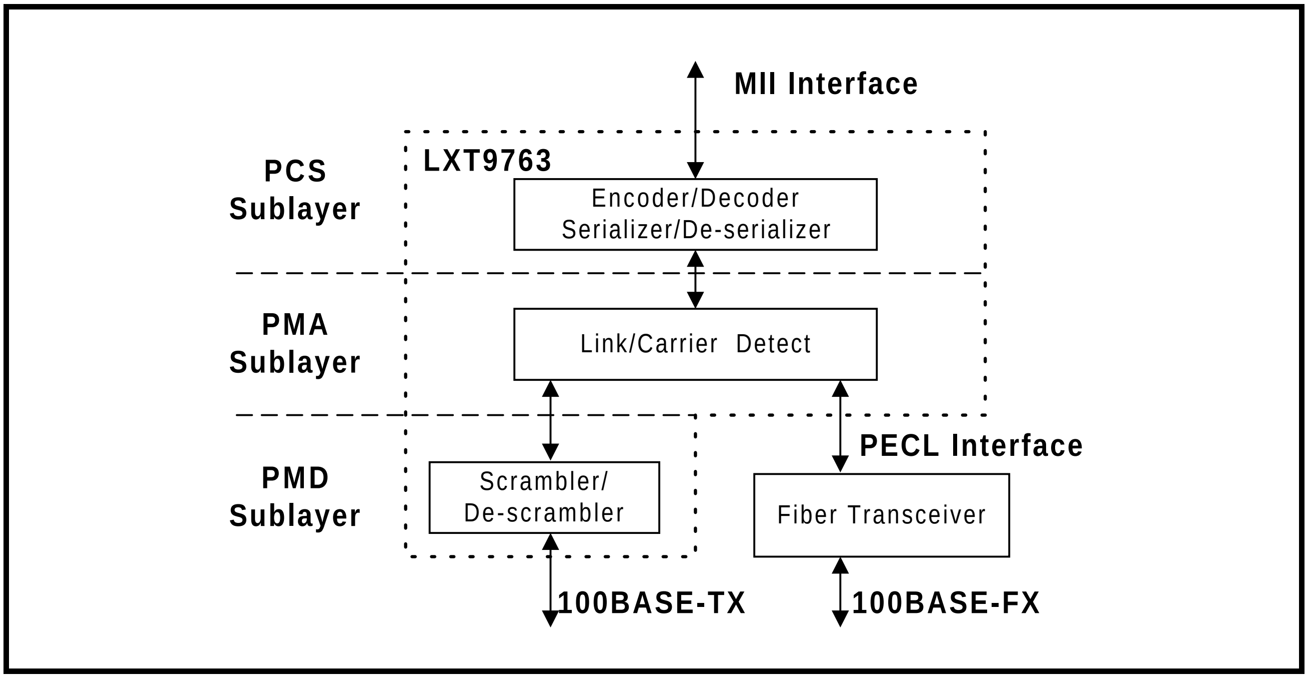


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Table 9: 4B/5B Coding

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
DATA	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5
	0 1 1 0	6	0 1 1 1 0	Data 6
	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E
	1 1 1 1	F	1 1 1 0 1	Data F
IDLE	undefined	I [1]	1 1 1 11	Idle. Used as inter-stream fill code
CONTROL	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2
	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2
	undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (ESD), part 1 of 2
	undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (ESD), part 2 of 2
INVALID	undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signaling errors
	undefined	Invalid	0 0 0 0 0	Invalid
	undefined	Invalid	0 0 0 0 1	Invalid
	undefined	Invalid	0 0 0 1 0	Invalid
	undefined	Invalid	0 0 0 1 1	Invalid
	undefined	Invalid	0 0 1 0 1	Invalid
	undefined	Invalid	0 0 1 1 0	Invalid
	undefined	Invalid	0 1 0 0 0	Invalid
	undefined	Invalid	0 1 1 0 0	Invalid
	undefined	Invalid	1 0 0 0 0	Invalid
	undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

PMA Sublayer

Link

In 100TX and FX modes, the LXT9763 establishes a link whenever the scrambler becomes locked and remains locked for approximately 50 ms. Whenever the scrambler loses lock (<12 consecutive idle symbols during a 2 ms window), the link will be taken down. This provides a very robust link, essentially filtering out any small noise hits that may otherwise disrupt the link.

The LXT9763 reports link failure via the MII status bits (1.2, 17.10, and 19.4) and interrupt functions. If auto-negotiate is enabled, link failure causes the LXT9763 to re-negotiate.

Link Failure Override

The LXT9763 normally transmits 100 Mbps data packets or Idle symbols only if the link is up, and transmits only FLP bursts if the link is not up. Setting bit 16.14 = 1 overrides this function, allowing the LXT9763 to transmit data packets even when the link is down. This feature is provided as a diagnostic tool. Note that auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT9763 automatically begins transmitting FLP bursts if the link goes down.

Carrier Sense

For 100TX and 100FX links, a Start-of-Stream Delimiter (SSD) or /J/K symbol pair causes assertion of carrier sense (CRS). An End-of-Stream Delimiter (ESD), or /T/R symbol pair causes de-assertion of CRS. The PMA layer also de-asserts CRS if IDLE symbols are received without /T/R; however, in this case RX_ER is asserted for one clock cycle when CRS is de-asserted.

Usage of CRS for Interframe Gap (IFG) timing is *not* recommended for the following reasons:

- De-assertion time for CRS is slightly longer than assertion time. This causes IFG intervals to appear somewhat shorter to the MAC than it actually is on the wire.
- CRS de-assertion is not aligned with TX_EN de-assertion on transmit loopbacks in half-duplex mode.

Receive Data Valid

The LXT9763 asserts RX_DV to indicate that the received data maps to valid symbols. However, RXD outputs zeros until the received data is decoded and available for transfer to the controller.

Twisted-Pair PMD Sublayer

The twisted-pair Physical Medium Dependent (PMD) layer provides the signal scrambling and descrambling, line coding and decoding (MLT-3 for 100TX, Manchester for 10T), as well as receiving, polarity correction, and baseline wander correction functions.

Scrambler/Descrambler (100TX Only)

The scrambler spreads the signal power spectrum and further reduces EMI using an 11-bit, non-data-dependent polynomial. The receiver automatically decodes the polynomial whenever it receives IDLE symbols.

The scrambler/descrambler can be bypassed by setting bit 16.12 = 1. The scrambler is automatically bypassed when the fiber port is enabled. Scramber bypass is provided for diagnostic and test support.

Baseline Wander Correction (100TX Only)

The LXT9763 provides a baseline wander correction function, making the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is by definition “unbalanced”. This means that the DC average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). This wander can cause receiver errors, particularly in less robust designs, at long line lengths (100 meters). The exact characteristics of the wander are completely data dependent.

The LXT9763 baseline wander correction characteristics allow the device to recover error-free data while receiving worst-case “killer” packets over all cable lengths.

Polarity Correction

The LXT9763 automatically detects and corrects for the condition where the receive signal (TPIP/N) is inverted. Reversed polarity is detected if eight inverted link pulses, or four inverted end-of-frame (EOF) markers, are received consecutively. If link pulses or data are not received by the maximum receive time-out period, the polarity state is reset to a non-inverted state.

Fiber PMD Sublayer

The LXT9763 provides a PECL interface for connection to an external fiber-optic transceiver. (The external transceiver provides the PMD function for fiber media.) The LXT9763 uses an NRZI format for the fiber interface.

The fiber interface operates at 100 Mbps and does not support 10FL applications.

Far End Fault Indications

The LXT9763 does not provide Signal Detect pins and therefore does not independently detect signal faults. However, the device can detect a far end fault code embedded in the received data stream and uses bit 1.4 to report far end fault indications received from its link partner. Bit 1.4 is set once and clears when read.

A far end fault condition causes the LXT9763 to drop the link unless Forced Link Pass is selected (16.14 = 1). Link down condition is then reported via interrupts and status bits.

10 Mbps Operation

The LXT9763 can operate as a standard 10BASE-T transceiver, supporting all the standard 10 Mbps functions. During 10BASE-T (10T) operation, the LXT9763 transmits and receives Manchester-encoded data across the network link. When the MAC is not actively transmitting data, the LXT9763 drives link pulses onto the line.

In 10T mode, the polynomial scrambler/descrambler is inactive. Manchester-encoded signals received from the network are decoded by the LXT9763 and sent across the MII to the MAC. The 10M reversed polarity correction function is the same as the 100M function described on page 24.

The LXT9763 does not support fiber connections at 10 Mbps.

10T Preamble Handling

The LXT9763 offers two options for preamble handling, selected by bit 16.5. In 10T Mode when 16.5 = 0, the LXT9763 strips the entire preamble off of received packets. CRS is asserted coincident with SFD. RX_DV is held Low for the duration of the preamble. When RX_DV is asserted, the very first two nibbles driven by the LXT9763 are the SFD “5D” hex followed by the body of the packet.

In 10T mode with 16.5 = 1, the LXT9763 passes the preamble through the MII and asserts RX_DV and CRS simultaneously. In 10T loopback, the LXT9763 loops back whatever the MAC transmits to it, including the preamble.

10T Carrier Sense

For 10T links, CRS assertion is based on reception of valid preamble, and de-assertion on reception of an end-of-frame (EOF) marker. Bit 16.7 allows CRS de-assertion to be synchronized with RX_DV de-assertion. Refer to Table 47 on page 61.

10T Dribble Bits

The LXT9763 device handles dribbles bits in all modes. If between 1-4 dribble bits are received, the nibble is sent across the MII, padded with 1s if necessary. If between 5-7 dribble bits are received, the second nibble is not sent onto the MII bus.

10T Link Test

In 10T mode, the LXT9763 always transmit link pulses. If the Link Test function is enabled, it monitors the connection for link pulses. Once link pulses are detected, data transmission will be enabled and will remain enabled as long as either the link pulses or data transmission continue. If the link pulses stop, the data transmission will be disabled.

If the Link Test function is disabled (Force Link Pass), the LXT9763 will transmit to the connection regardless of detected link pulses. The Link Test function can be disabled by setting bit 16.14 = 1.

Link Test Failure

Link Test failure occurs if Link Test is enabled and link pulses or packets stop being received. If this condition occurs, the LXT9763 returns to the auto-negotiation phase if auto-negotiation is enabled.

10T Jabber

If a transmission exceeds the jabber timer, the LXT9763 will disable the transmit and loopback functions. See Figure 28 on page 47 for jabber timing parameters.

The LXT9763 automatically exits jabber mode after the unjab time has expired. This function can be disabled by setting bit 16.10 = 1.

Monitoring Operations

Monitoring Auto-Negotiation

Auto-negotiation can be monitored as follows:

- Bit 17.7 is set to 1 once the auto-negotiation process is completed.
- Bits 1.2 and 17.10 are set to 1 once the link is established.
- Additional bits in Register 1 (refer to Table 39 on page 55) and Register 17 (refer to Table 48 on page 62) can be used to determine the link operating conditions and status.

Monitoring Next Page Exchange

The LXT9763 offers an Alternate Next Page mode to simplify the next page exchange process. Normally, bit 6.1 (Page Received) remains set until read. When Alternate Next Page mode is enabled (16.1 = 1), bit 6.1 is automatically cleared whenever a new negotiation process takes place. This prevents the user from reading an old value in 6.1 and assuming that Registers 5 and 8 (Partner Ability) contain valid information. Additionally, the LXT9763 uses bit 6.5 to indicate when the current received page is the base page. This information is useful for recognizing when next pages must be resent due to a new negotiation process starting. Bits 6.1 and 6.5 are cleared when read.

Per-Port LED Driver Functions

The LXT9763 incorporates three direct drive LEDs per port. On power up all the LEDs will light for approximately 1 second after reset de-asserts. Each LED can be programmed to one of several different display modes using the LED Configuration Register. Each per-port LED can be programmed (refer to Table 51 on page 65) to indicate one the following conditions:

- Operating Speed
- Transmit Activity
- Receive Activity
- Collision Condition
- Link Status
- Duplex Mode

The LEDs can also be programmed to display various combined status conditions. For example, setting bits 20.15:12 = 1101 produces the following combination of Link and Activity indications:

- If Link is down LED is off.
- If Link is up LED is on.
- If Link is up AND activity is detected, the LED will blink at the stretch interval selected by bits 20.3:2 and will continue to blink as long as activity is present.

The LED driver pins are also used to provide initial configuration settings. The LED pins are sensitive to polarity and will automatically pull up or pull down to configure for either open drain or open source circuits (10mA max current rating) as required by the hardware configuration. Refer to the discussion of "Hardware Configuration Settings" on page 16 for details.

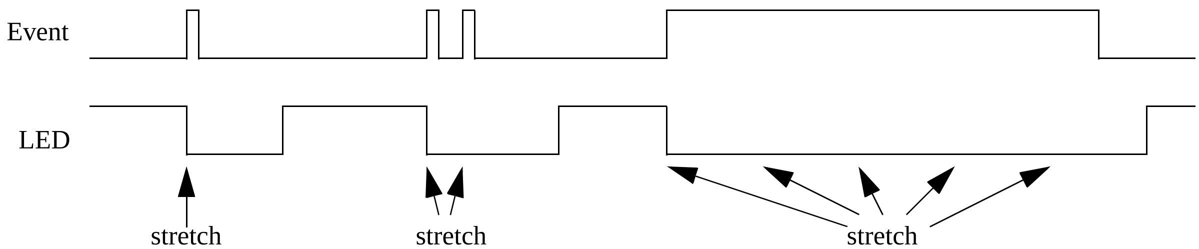
LED Pulse Stretching

The LED Configuration Register also provides optional LED pulse stretching to 30, 60, or 100 ms. If during this pulse stretch period, the event occurs again, the pulse stretch time will be further extended.

When an event such as receiving a packet occurs it will be edge detected and it will start the stretch timer. The LED driver will remain asserted until the stretch timer expires. If another event occurs before the stretch timer expires then the stretch timer will be reset and the stretch time will be extended.

When a long event (such as duplex status) occurs it will be edge detected and it will start the stretch timer. When the stretch timer expires the edge detector will be reset so that a long event will cause another pulse to be generated from the edge detector which will reset the stretch timer and cause the LED driver to remain asserted. Figure 15 shows how the stretch operation functions.

Figure 15: LED Pulse Stretching



Note: The direct drive LED outputs in this diagram are shown as active Low.

Boundary Scan (JTAG1149.1) Functions

LXT9763 includes a IEEE 1149.1 boundary scan test port for board level testing. All digital input, output, and input/output pins are accessible.

Boundary Scan Interface

This interface consists of five pins (TMS,TDI,TDO,TCK and $\overline{\text{TRST}}$). It includes a state machine, data register array, and instruction register. The TMS and TDI pins are internally pulled up. TCK is internally pulled down. TDO does not have an internal pull-up or pull-down.

State Machine

The TAP controller is a 16 Bit state machine driven by the TCK and TMS pins. Upon reset the TEST_LOGIC_RESET state is entered. The state machine is also reset when TMS is High for five TCK periods.

Instruction Register

After the state machine resets, the IDCODE instruction is always invoked. The decode logic ensures the correct data flow to the Data registers according to the current instruction. Valid instructions are listed in Table 11.

Boundary Scan Register

Each BSR cell has two stages. A flip-flop and a latch are used for the serial shift stage and the parallel output stage. There are four modes of operation as listed in Table 10.

Table 10: BSR Mode of Operation

Mode	Description
1	Capture
2	Shift
3	Update
4	System Function

Table 11: Supported JTAG Instructions

Name	Code	Description	Mode	Data Register
EXTEST	0000000000000000	External Test	BSR	EXTEST
IDCODE	1111111111111110	ID Code Inspection	ID REG	IDCODE
SAMPLE	1111111111111110	Sample Boundary	BSR	SAMPLE
High Z	1111111111001111	Force Float	Bypass	High Z
Clamp	1111111111101111	Clamp	BSR	Clamp
BYPASS	1111111111111111	Bypass Scan	Bypass	BYPASS

Table 12: Device ID Register

31:28	27:12	11:8	7:1	0
Version	**Part ID (hex)**	**Jedec Continuation Characters**	**JEDEC ID[1]**	**Reserved**
0000	2623	0000	111 1110	1

1. The JEDEC ID is an 8-bit identifier. The MSB is for parity and is ignored.
Level One's JEDEC ID is FE (1111 1110) which becomes 111 1110.

APPLICATION INFORMATION

Design Recommendations

The LXT9763 is designed to comply with IEEE requirements and to provide outstanding receive Bit Error Rate (BER) and long-line-length performance. To achieve maximum performance from the LXT9763, attention to detail and good design practices are required. Refer to the LXT9763 Design and Layout Guide for detailed design and layout information.

General Design Guidelines

Adherence to generally accepted design practices is essential to minimize noise levels on power and ground planes. Up to 50 mV of noise is considered acceptable. 50 to 80 mV of noise is considered marginal. High-frequency switching noise can be reduced, and its effects can be eliminated, by following these simple guidelines throughout the design:

- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer.
- Use ample bulk and decoupling capacitors throughout the design (a value of .01 µF is recommended for decoupling caps).
- Provide ample power and ground planes.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Filter and shield DC-DC converters, oscillators, etc.
- Do not route any digital signals between the LXT9763 and the RJ-45 connectors at the edge of the board.
- Do not extend any circuit power and ground plane past the center of the magnetics or to the edge of the board. Use this area for chassis ground, or leave it void.

Power Supply Filtering

Power supply ripple and digital switching noise on the VCC plane can cause EMI problems and degrade line performance. The best approach is to minimize ground noise as much as possible using good general techniques and by filtering the VCC plane. It is generally difficult to predict in advance the performance of any design, although certain factors greatly increase the risk of having problems:

- Poorly-regulated or over-burdened power supplies
- Wide data busses (32-bits+) running at a high clock rate
- DC-to-DC converters

Level One recommends filtering the power supply to the analog VCC pins of the LXT9763. This has two benefits. First, it keeps digital switching noise out of the analog circuitry inside the LXT9763, which helps line performance. Second, if the VCC planes are laid out correctly, it keeps digital switching noise away from external connectors, reducing EMI problems.

The recommended implementation is to break the VCC plane into two sections. The digital section supplies power to the VCCD and VCCIO pins of the LXT9763. The analog section supplies power to the VCCA pins. The break between the two planes should run underneath the device. In designs with more than one LXT9763, a single continuous analog VCC plane can be used to supply them all.

The digital and analog VCC planes should be joined at one or more points by ferrite beads. The beads should produce at least a 100Ω impedance at 100 MHz. Beads should be placed so that current flow is evenly distributed. The maximum current rating of the beads should be at least 150% of the current that is actually expected to flow through them. A bulk cap (2.2 -10 µF) should be place on each side of each bead.

In addition, a high-frequency bypass cap (.01 µF) should be placed near each analog VCC pin.

Power and Ground Plane Layout Considerations

Great care needs to be taken when laying out the power and ground planes.

- Follow the guidelines in the *LXT9761/62/63/81/82 Design & Layout Guide* for locating the split between the digital and analog VCC planes.
- Keep the digital VCC plane away from the TPFOP/N and TPFIP/N signals, away from the magnetics, and away from the RJ45 connectors.
- Place the layers so that the TPFOP/N and TPFIP/N signals can be routed near or next to the ground plane. For EMI reasons, it is more important to shield TPFOP/N than TPFIP/N.

Chassis Ground

For ESD reasons, it is a good design practice to create a separate chassis ground that encircles the board and is isolated via moats and keep-out areas from all circuit-ground planes and active signals. Chassis ground should extend from the RJ45 connectors to the magnetics, and can be used to terminate unused signal pairs (‘Bob Smith’ termination). In single-point grounding applications, provide a single connection between chassis and circuit grounds with a 2 kV isolation capacitor. In multi-point grounding schemes (chassis and circuit grounds joined at multiple points), provide 2 kV isolation to the Bob Smith termination.

MII Terminations

The LXT9763 MII has high output impedance (250 - 350Ω) and normally only requires termination on the output signals in designs with long traces (>3 inches). Use series termination resistors on all RX_CLK and TX_CLK signals to minimize reflections. Place the resistor as close to the device as possible. Use a software trace termination package to select an optimal resistance value for the specific trace. If this is not possible, use a 50Ω resistor value.

The RBIAS Pin

The LXT9763 requires a 22.1 kΩ, 1% resistor directly connected between the RBIAS pin and ground. Place the RBIAS resistor as close to the RBIAS pin as possible. Run an etch directly from the pin to the resistor, and sink the other side of the resistor to a filtered ground. Surround the RBIAS trace with a filtered ground; do not run high-speed signals next to RBIAS.

The Twisted-Pair Interface

Follow standard guidelines for a twisted-pair interface:

- Place the magnetics as close as possible to the LXT9763.
- Keep transmit pair traces as short as possible; both traces should have the same length.
- Avoid vias and layer changes as much as possible.
- Keep the transmit and receive pairs apart to avoid cross-talk.
- Route the transmit pair adjacent to a ground plane. The optimum arrangement is to place the transmit traces two to three layers from the ground plane, with no intervening signals.
- Improve EMI performance by filtering the TPO center tap. A single ferrite bead may be used to supply center tap current to all ports. All six ports draw a combined total of 370 mA so the bead should be rated at 560 mA.

Magnetics Information

The LXT9763 requires a 1:1 ratio for the receive transformers and a 1:1 ratio for the transmit transformers. The transformer isolation voltage should be rated at 1.5 kV to protect the circuitry from static voltages across the connectors and cables. Refer to Table 13 for transformer requirements. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and validate the magnetics for the specific application.

The Fiber Interface

The fiber interface consists of a PECL transmit and receive pair to an external fiber-optic transceiver. The LXT9763 does not provide Signal Detect pins and therefore does not receive or transmit fault signals. The transmit and receive pair should be DC-coupled to the transceiver, and biased appropriately. Refer to the fiber transceiver manufacturer's recommendations for termination circuitry. Figure 18 on page 34 shows a typical example.

Table 13: Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1 : 1	–	–	
Tx turns ratio	–	1 : 1	–	–	
Insertion loss	0.0	0.6	1.1	dB	
Primary inductance	350	–	–	µH	
Transformer isolation	–	1.5	–	kV	
Differential to common mode rejection	40	–	–	dB	.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	-16	–	–	dB	30 MHz
	-10	–	–	dB	80 MHz
Rise Time	2.0	–	3.5	ns	10% to 90%

Typical Application Circuits

Figure 17 shows a typical layout of the LXT9763 twisted-pair interface in a dual-high (stacked) RJ-45 application.

Figure 16: Power and Ground Supply Connections

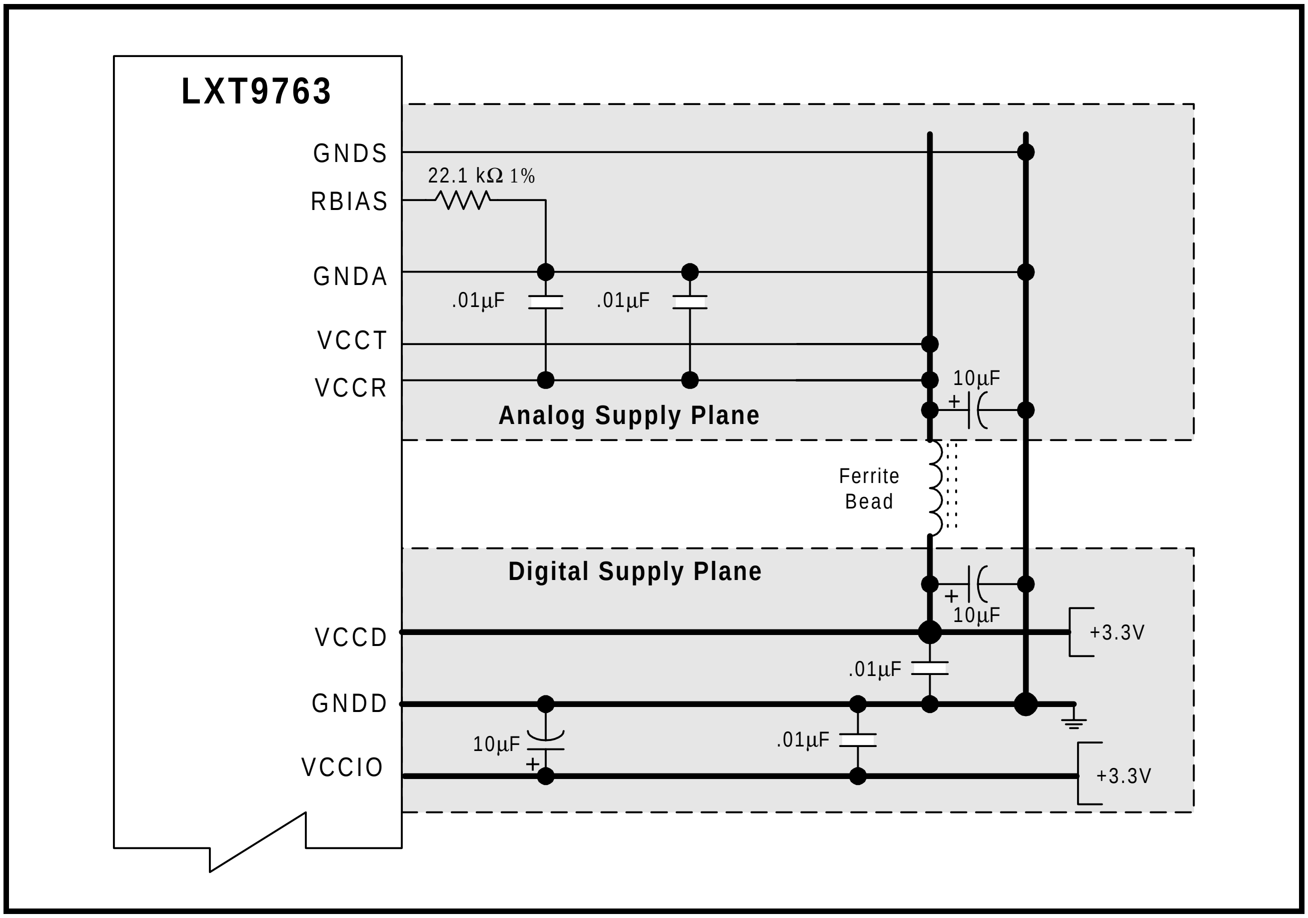
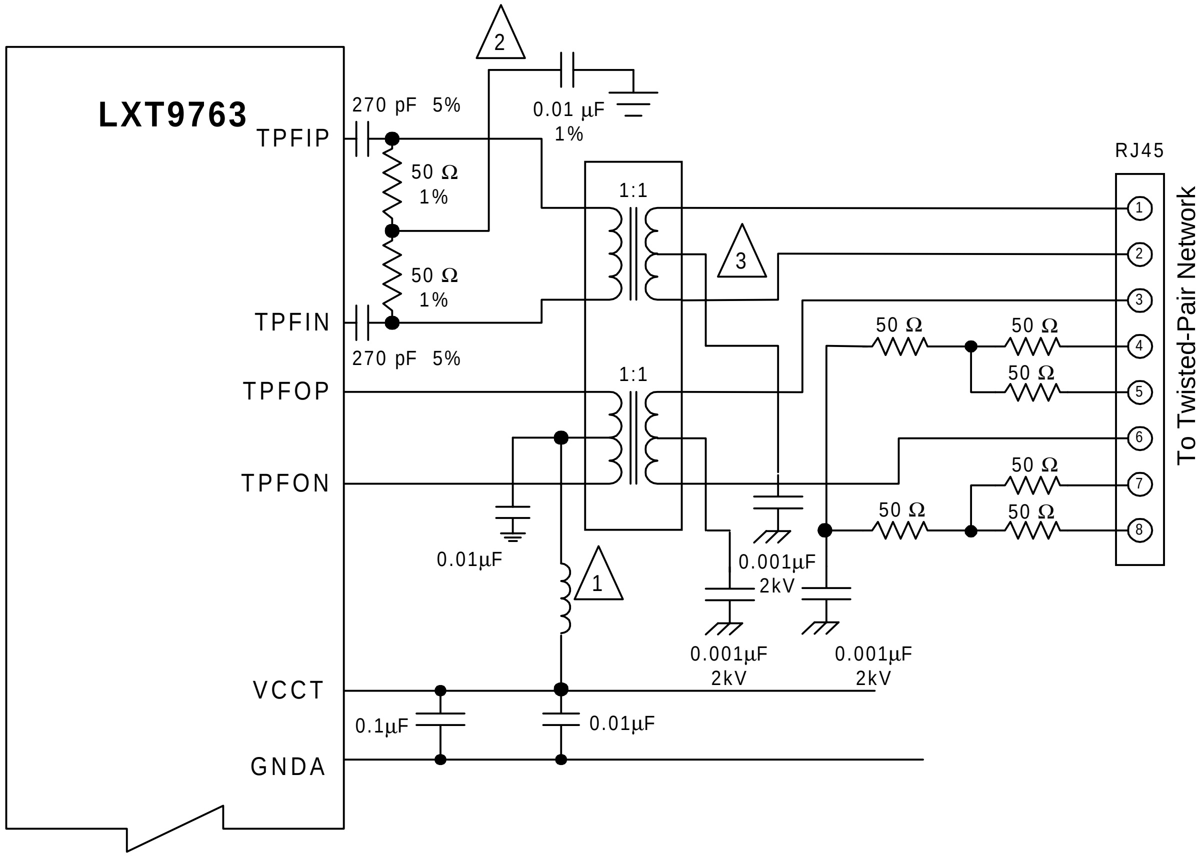
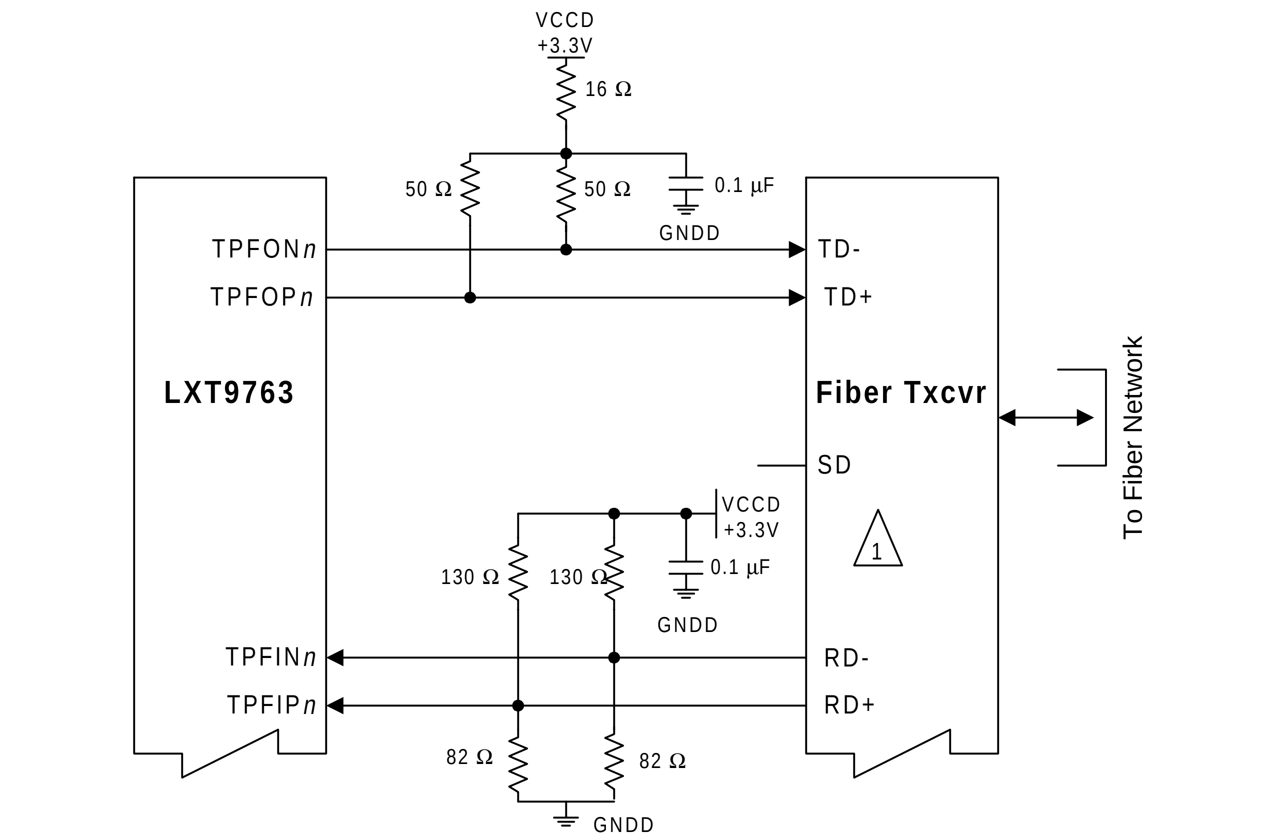


Figure 17: Typical Twisted-Pair Interface



1. Center tap current may be supplied from 3.3V VCCA as shown. However, additional power savings may be realized by supplying the center-tap from a 2.5V current source. In either case a single ferrite bead (rated at 560 mA) may be used to supply center tap current to all ports.
2. Receiver common mode bypass cap may improve BER performance in systems with noisy power supplies.
3. Magnetics without a receive pair center-tap do not require a 2 kV termination.

Figure 18: Typical Fiber Interface



1. Refer to fiber transceiver manufacturer's recommendations for termination circuitry. Example shown above is suitable for HFBR5900-series devices.

TEST SPECIFICATIONS

NOTE

Tables 14 through 34 and Figures 19 through 33 represent the performance specifications of the LXT9763. These specifications are guaranteed by test except where noted “by design.” Minimum and maximum values listed in Tables 16 through 34 apply over the recommended operating conditions specified in Table 15.

Table 14: Absolute Maximum Ratings

Parameter		Sym	Min	Max	Units
Supply voltage		VCC	-0.3	4.0	V
Operating temperature	Ambient	TOPA	0	+70	ºC
	Case	TOPC	–	+120	ºC
Storage temperature		TST	-65	+150	ºC

CAUTION

Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 15: Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units
Recommended operating temperature	Ambient	TOPA	0	–	70	ºC
	Case	TOPC	0	–	110	ºC
Recommended supply voltage[2]	Analog & Digital	VCCA, VCCD	3.15	3.3	3.45	V
	I/O	VCCIO	3.15	3.3	3.45	V
VCC current	100BASE-TX	ICC	–	115[3]–	130[3]	mA
	100BASE-FX	ICC	–	–	–	mA
	10BASE-T	ICC	–	115[3]–	130[3]	mA
	Auto-Negotiation	ICC	–	114.5[3]	130[3]	mA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.
3. Per port @ 3.3V.

Table 16: Digital I/O Characteristics [1]

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage[3]	V_{IL}	–	–	0.8	V	–
Input High voltage[3]	V_{IH}	2.0	–	–	V	–
Input current	I_I	-10	–	10	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

1. Applies to all pins except MII pins. Refer to Table 17 for MII I/O Characteristics.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. Does not apply to REFCLK. Refer to Table 18 for clock input levels.

Table 17: Digital I/O Characteristics - MII Pins

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input current	I_I	-10	–	10	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.2	–	–	V	I_{OH} = -4 mA, V_{CC} = 3.3V
	V_{OH}	2.0	–	–	V	I_{OH} = -4 mA, V_{CC} = 2.5V
Driver output resistance (Line driver output enabled)	R_O[2]	–	100	–	Ω	V_{CC} = 2.5V
	R_O[2]	–	100	–	Ω	V_{CC} = 3.3V

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

Table 18: Required Reference Clock (REFCLK) Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input frequency	F	–	25	–	MHz	–
Input clock frequency tolerance[1]	Δf	–	–	± 100	ppm	–
Input clock duty cycle[1]	T_{DC}	40	–	60	%	–

1. Parameter is guaranteed by design; not subject to production testing.

Table 19: 100BASE-TX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	V_P	0.95	–	1.05	V	Note 2
Signal amplitude symmetry	V_{SS}	98	–	102	%	Note 2
Signal rise/fall time	T_{RF}	3.0	–	5.0	ns	Note 2
Rise/fall time symmetry	T_{RFS}	–	–	0.5	ns	Note 2
Duty cycle distortion	–	–	–	± 0.5	ns	Offset from 16ns pulse width at 50% of pulse peak
Overshoot	V_O	–	–	5	%	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω(+/-1%) resistor.

Table 20: 100BASE-FX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage (single ended)	V_{OP}	0.6	–	1.5	V	–
Signal rise/fall time	T_{RF}	–	–	1.9	ns	10 <–> 90% 2.0 pF load
Jitter (measured differentially)	–	–	–	1.4	ns	–
Receiver						
Peak differential input voltage	V_{IP}	0.55	–	1.5	V	–
Common mode input range	V_{CMIR}	–	–	V_{CC} - 0.7	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 21: 10BASE-T Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage	V_{OP}	2.2	–	2.8	V	Note 2
Link transmit period	–	8	–	24	ms	–
Transmit timing jitter added by the MAU and PLS sections [3, 4]	–	0	–	11	ns	Note 5
Receiver						
Link min receive timer	TLRmin	2	4	7	ms	–
Link max receive timer	TLRmax	50	64	150	ms	–
Time link loss receive	TLL	50	64	150	ms	–
Differential squelch threshold	V_{DS}	–	–	–	mV Peak	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω(+/-1%) resistor.
3. Parameter is guaranteed by design; not subject to production testing.
4. IEEE 802.3 specifies maximum jitter addition at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.
5. After line model specified by IEEE 802.3 for 10BASE-T MAU.

Figure 19: 100BASE-TX Receive Timing (4B Mode)

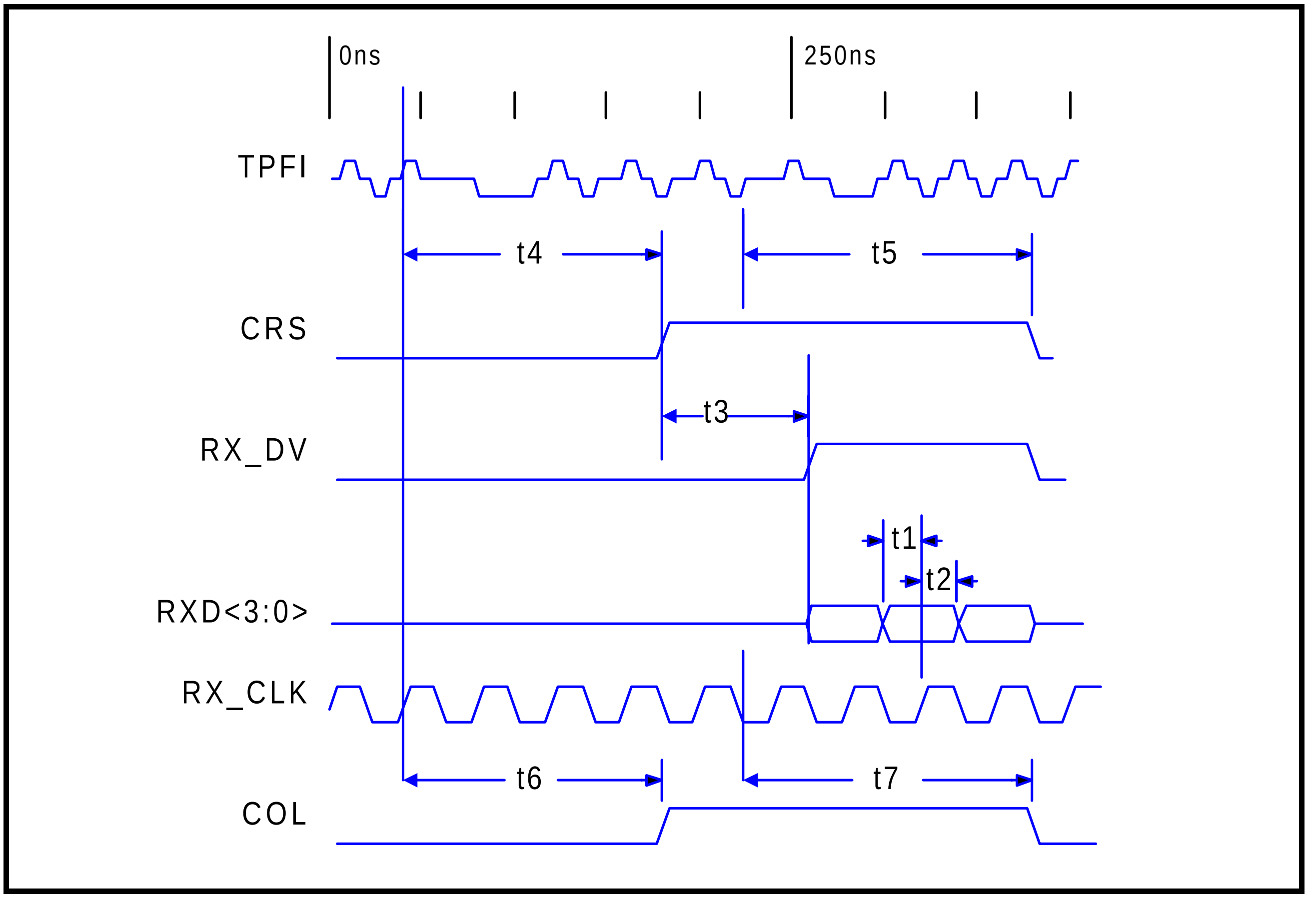


Table 22: 100BASE-TX Receive Timing Parameters (4B Mode)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD<3:0>, RX_DV, RX_ER setup to RX_CLK High	t1	10	–	–	ns	–
RXD<3:0>, RX_DV, RX_ER hold from RX_CLK High	t2	10	–	–	ns	–
CRS asserted to RXD<3:0>, RX_DV	t3	–	4	–	BT	–
Receive start of "J" to CRS asserted	t4	–	10	–	BT	–
Receive start of "T" to CRS de-asserted	t5	13	14	24	BT	–
Receive start of "J" to COL asserted	t6	–	14	20	BT	–
Receive start of "T" to COL de-asserted	t7	13	18	24	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 20: 100BASE-TX Transmit Timing (4B Mode)

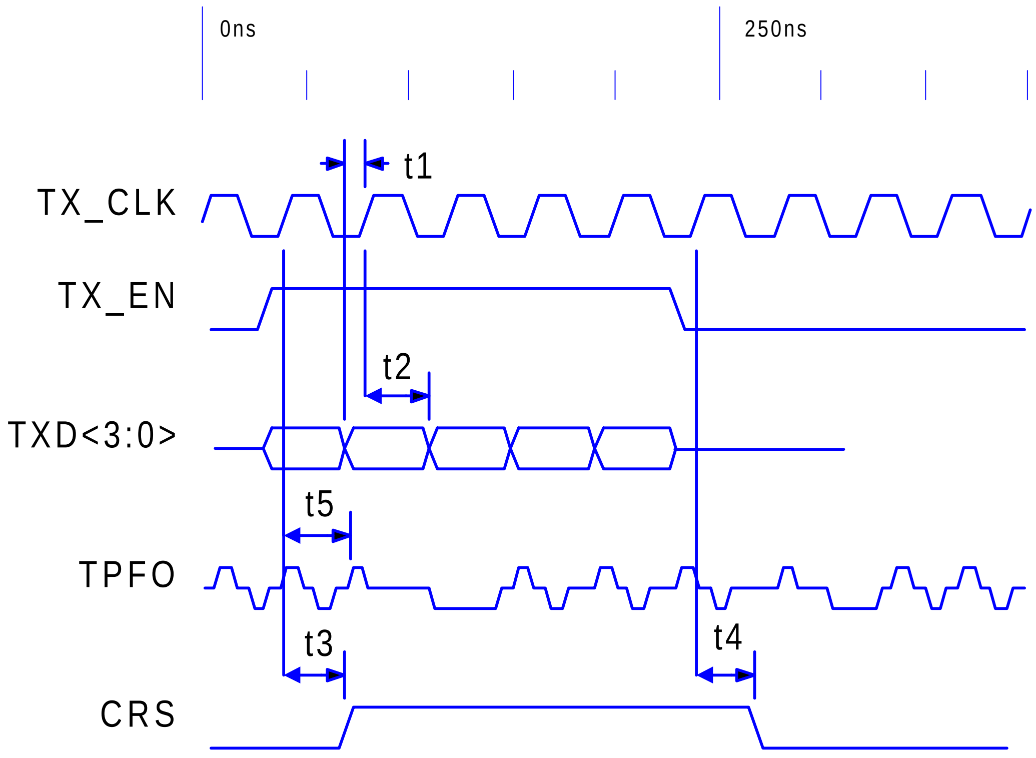


Table 23: 100BASE-TX Transmit Timing Parameters (4B Mode)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD<3:0>, TX_EN, TX_ER setup to TX_CLK High	t1	15	–	–	ns	–
TXD<3:0>, TX_EN, TX_ER hold from TX_CLK High	t2	0	–	–	ns	–
TX_EN sampled to CRS asserted	t3	–	44	–	ns	–
TX_EN sampled to CRS de-asserted	t4	–	52	–	ns	–
TX_EN sampled to TPFO out (Tx latency)	t5	–	13	–	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 21: 100BASE-TX Receive Timing (5B Mode)

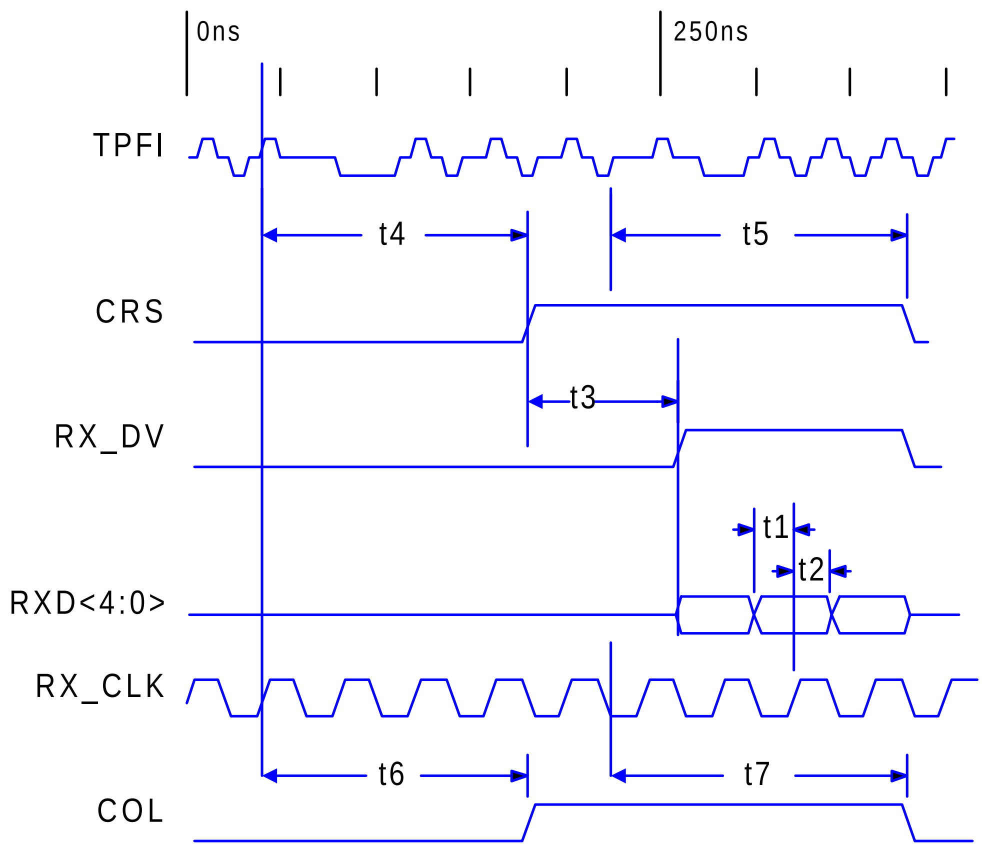


Table 24: 100BASE-TX Receive Timing Parameters (5B Mode)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD<4:0>, RX_DV, RX_ER setup to RX_CLK High	t1	10	–	–	ns	–
RXD<4:0>, RX_DV, RX_ER hold from RX_CLK High	t2	10	–	–	ns	–
CRS asserted to RXD<4:0>, RX_DV	t3	–	4	–	BT	–
Receive start of "J" to CRS asserted	t4	–	14	–	BT	–
Receive start of "T" to CRS de-asserted	t5	–	19	–	BT	–
Receive start of "J" to COL asserted	t6	–	14	–	BT	–
Receive start of "T" to COL de-asserted	t7	–	19	–	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 22: 100BASE-TX Transmit Timing (5B Mode)

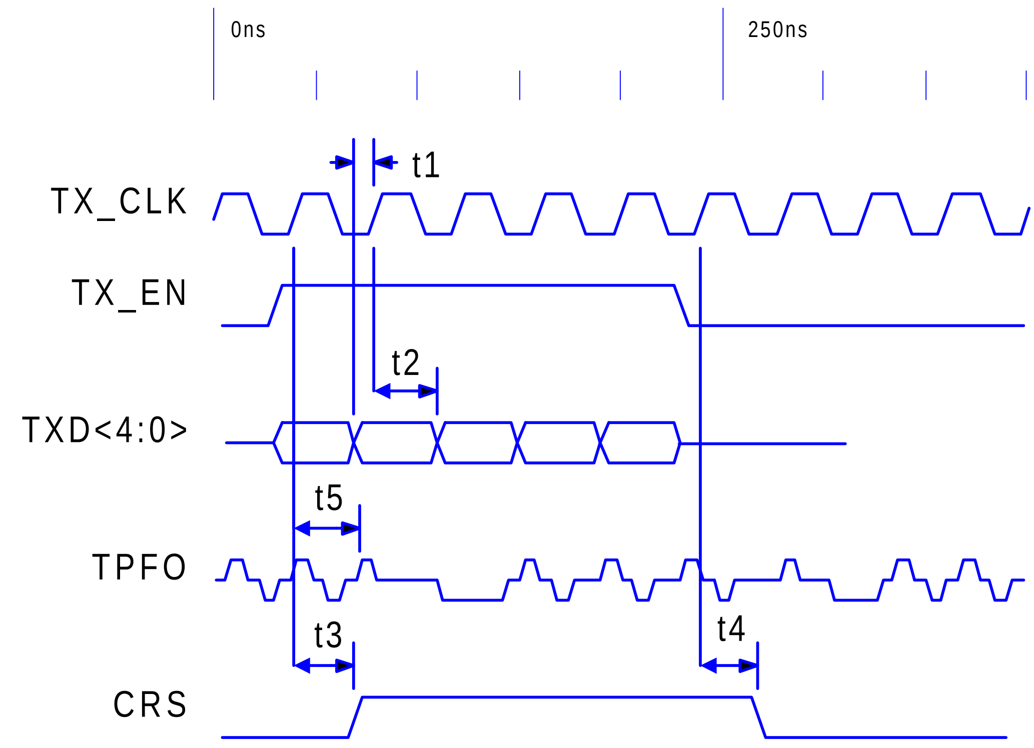


Table 25: 100BASE-TX Transmit Timing Parameters (5B Mode)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD<4:0>, TX_EN, TX_ER setup to TX_CLK High	t1	15	–	–	ns	–
TXD<4:0>, TX_EN, TX_ER hold from TX_CLK High	t2	0	–	–	ns	–
TX_EN sampled to CRS asserted	t3	–	44	–	ns	–
TX_EN sampled to CRS de-asserted	t4	–	52	–	ns	–
TX_EN sampled to TPOP out (Tx latency)	t5	–	6	–	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

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Figure 23: 100BASE-FX Receive Timing

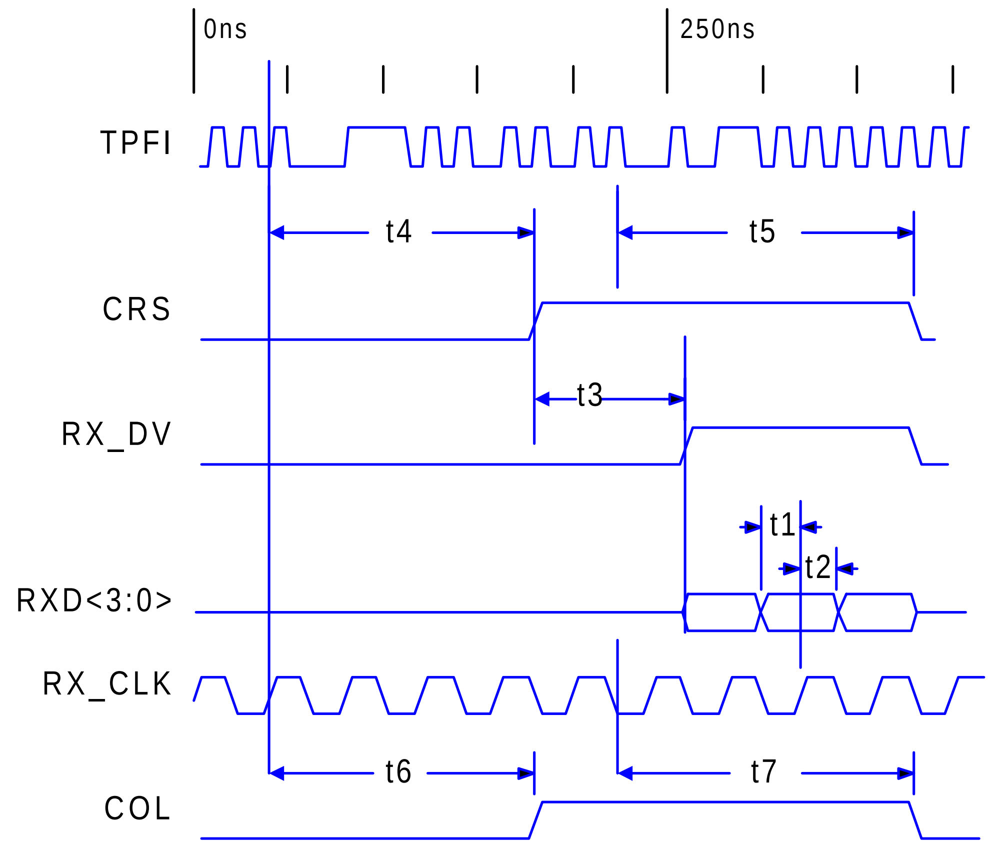


Table 26: 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD<3:0>, RX_DV, RX_ER setup to RX_CLK High	t1	10	–	–	ns	–
RXD<3:0>, RX_DV, RX_ER hold from RX_CLK High	t2	10	–	–	ns	–
CRS asserted to RXD<3:0>, RX_DV	t3	–	4	–	BT	–
Receive start of "J" to CRS asserted	t4	–	10	–	BT	–
Receive start of "T" to CRS de-asserted	t5	–	14	–	BT	–
Receive start of "J" to COL asserted	t6	–	10	–	BT	–
Receive start of "T" to COL de-asserted	t7	–	14	–	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 24: 100BASE-FX Transmit Timing

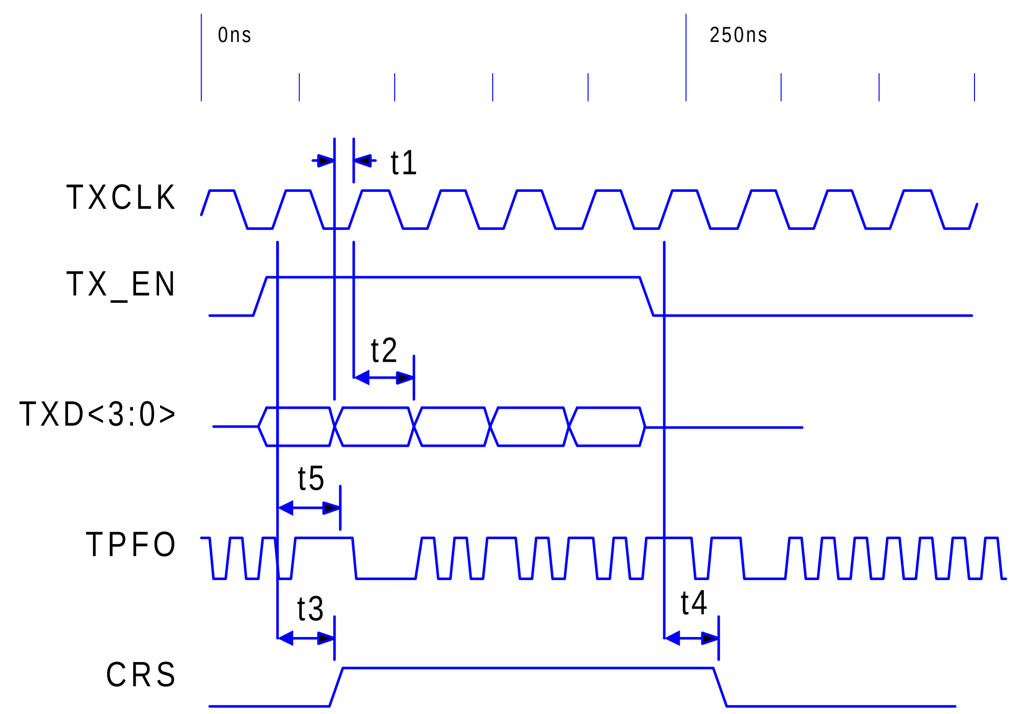


Table 27: 100BASE-FX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD<3:0>, TX_EN, TX_ER setup to TX_CLK High	t1	15	–	–	ns	–
TXD<3:0>, TX_EN, TX_ER hold from TX_CLK High	t2	0	–	–	ns	–
TX_EN sampled to CRS asserted	t3	–	3	–	BT	–
TX_EN sampled to CRS de-asserted	t4	–	4	–	BT	–
TX_EN sampled to TPFO out (Tx latency)	t5	–	13	–	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 25: 10BASE-T Receive Timing

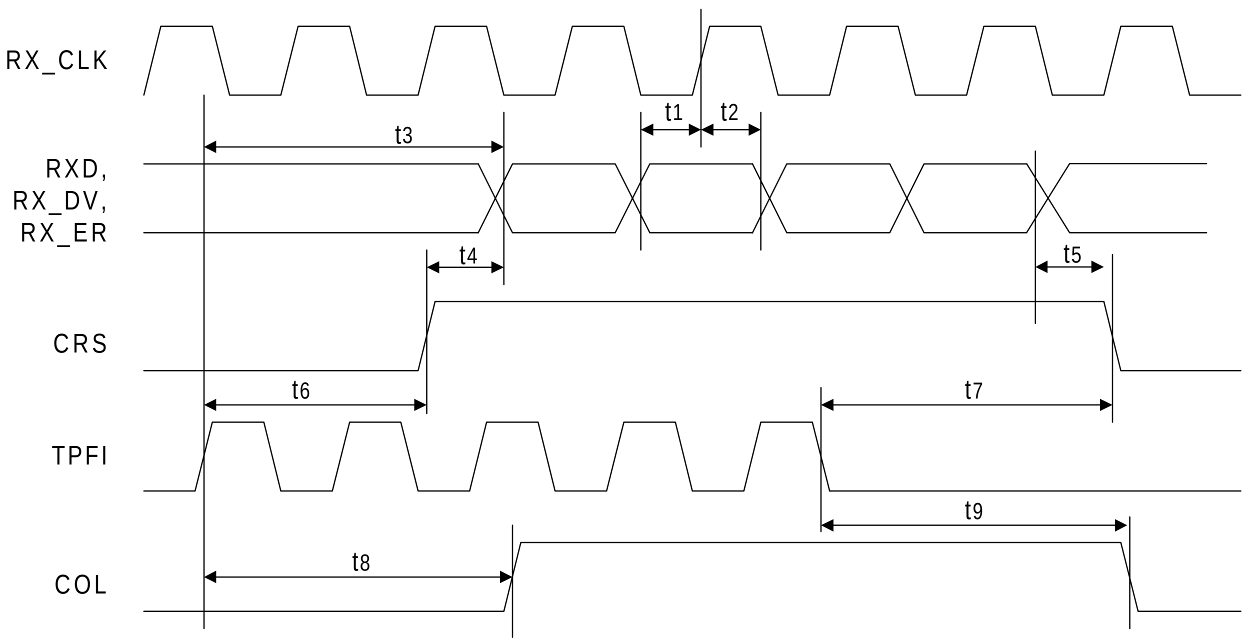


Table 28: 10BASE-T Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD, RX_DV, RX_ER setup to RX_CLK High	t1	10	–	–	ns	–
RXD, RX_DV, RX_ER hold from RX_CLK High	t2	10	–	–	ns	–
TPFI in to RXD out (Rx latency)	t3	–	6.6	–	BT	–
CRS asserted to RXD, RX_DV, RX_ER asserted	t4	–	18	–	BT	–
RXD, RX_DV, RX_ER de-asserted to CRS de-asserted	t5	–	1	–	BT	–
TPFI in to CRS asserted	t6	–	2.5	–	BT	–
TPFI quiet to CRS de-asserted	t7	–	12	–	BT	–
TPFI in to COL asserted	t8	–	3	–	BT	–
TPFI quiet to COL de-asserted	t9	–	12	–	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. CRS is asserted. RXD/RX_DV are driven at the start of SFD (64 BT).

Figure 26: 10BASE-T Transmit Timing

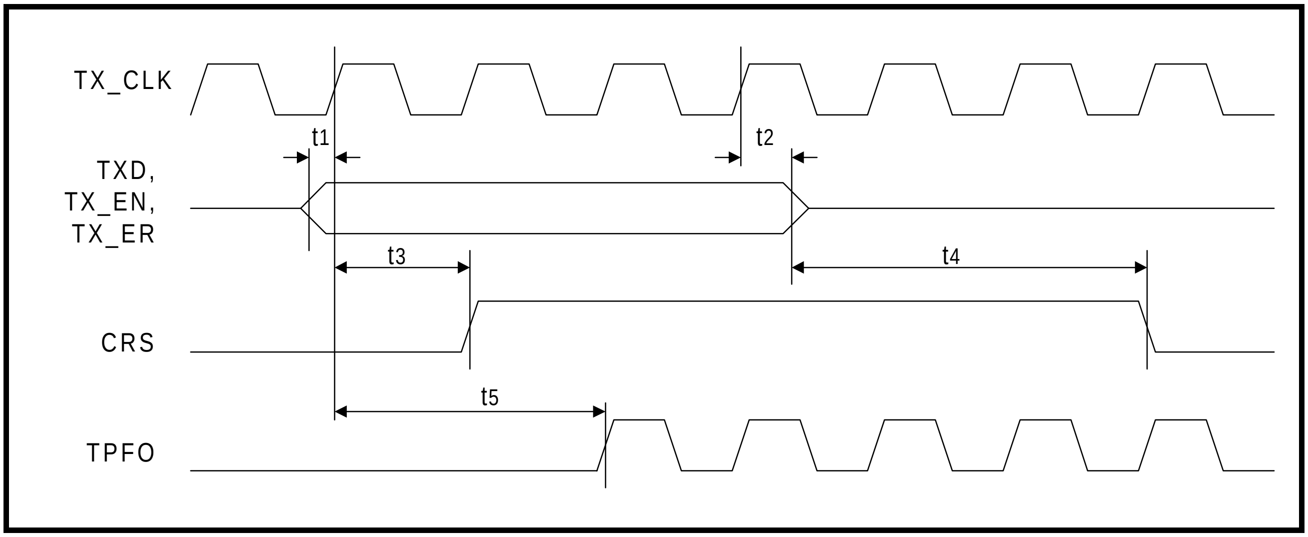


Table 29: 10BASE-T Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD, TX_EN, TX_ER setup to TX_CLK High	t1	10	–	–	ns	–
TXD, TX_EN, TX_ER hold from TX_CLK High	t2	0	–	–	ns	–
TX_EN sampled to CRS asserted	t3	–	2	–	BT	–
TX_EN sampled to CRS de-asserted	t4	–	1	–	BT	–
TX_EN sampled to TPFO out (Tx latency)	t5	–	280	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 27: 10BASE-T SQE (Heartbeat) Timing

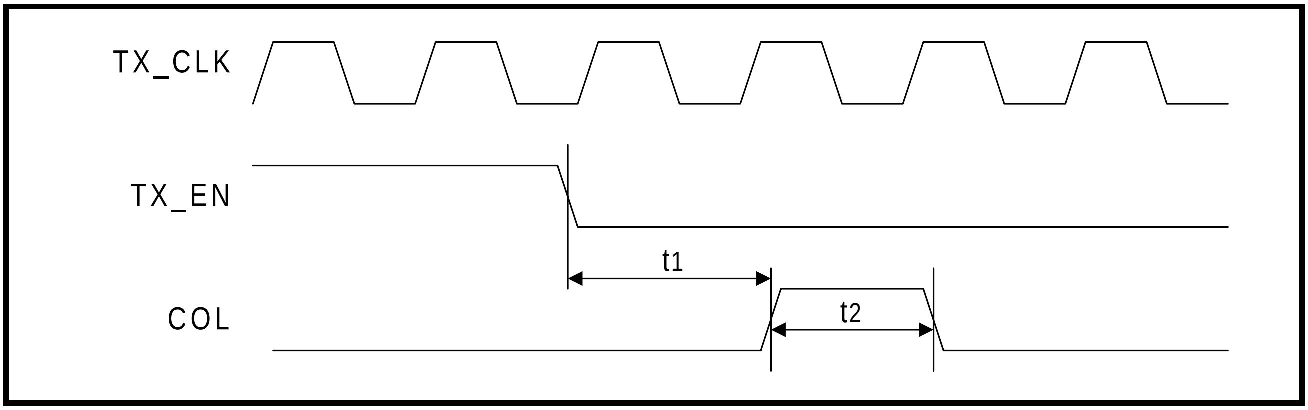


Table 30: 10BASE-T SQE (Heartbeat) Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
COL (SQE) delay after TX_EN off	t1	0.65	–	1.6	µs	–
COL (SQE) pulse duration	t2	0.5	–	1.5	µs	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 28: 10BASE-T Jab and Unjab Timing

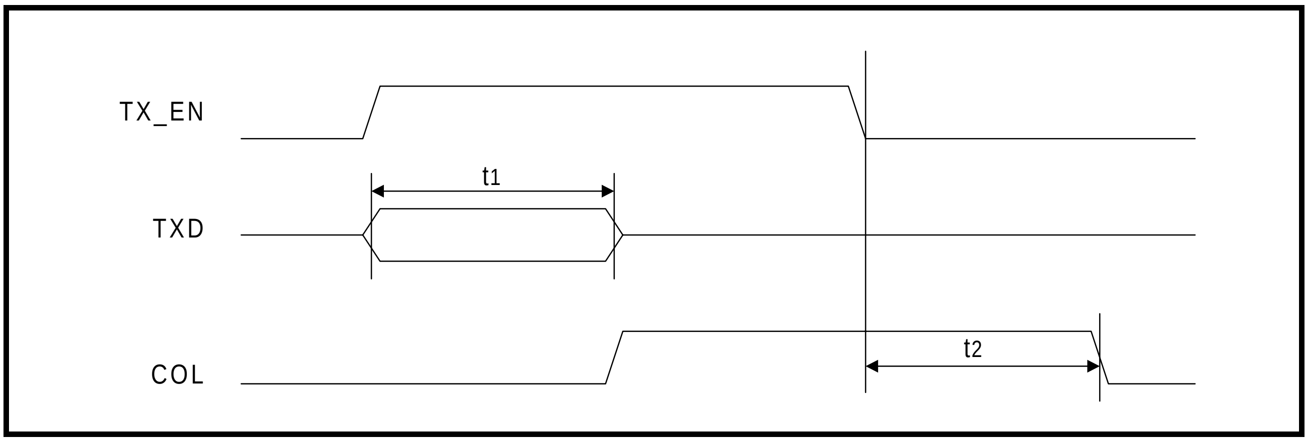


Table 31: 10BASE-T Jab and Unjab Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Maximum transmit time	t1	20	–	150	ms	–
Unjab time	t2	–	–	750	ms	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 29: Auto Negotiation and Fast Link Pulse Timing

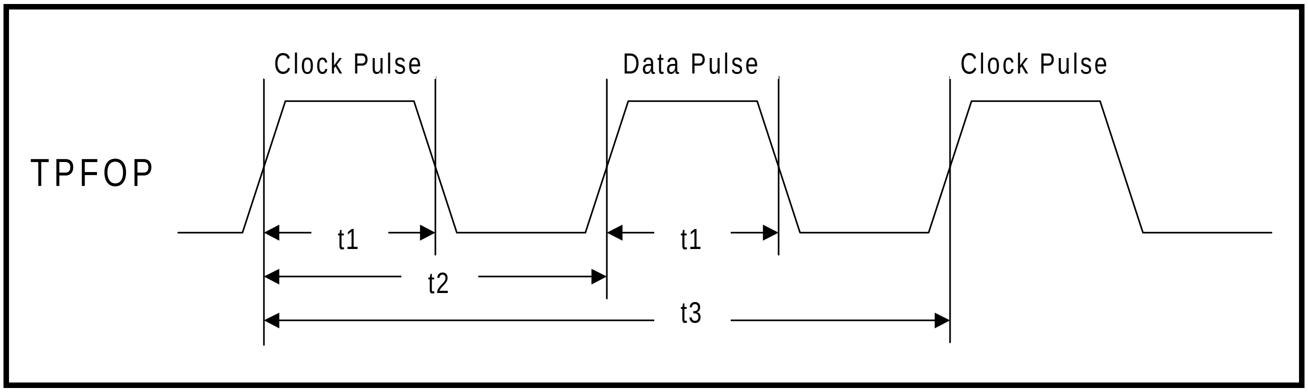


Figure 30: Fast Link Pulse Timing

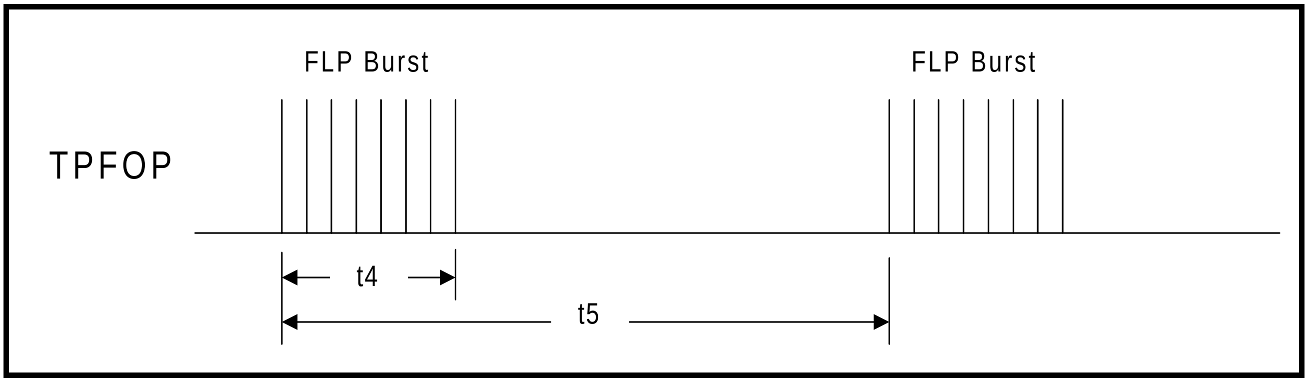


Table 32: Auto Negotiation and Fast Link Pulse Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Clock/Data pulse width	t1	–	100	–	ns	–
Clock pulse to Data pulse	t2	55.5	–	69.5	µs	–
Clock pulse to Clock pulse	t3	111	–	139	µs	–
FLP burst width	t4	–	2	–	ms	–
FLP burst to FLP burst	t5	8	–	24	ms	–
Clock/Data pulses per burst	–	17	–	33	ea	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 31: MDIO Write Timing (MDIO Sourced by MAC)

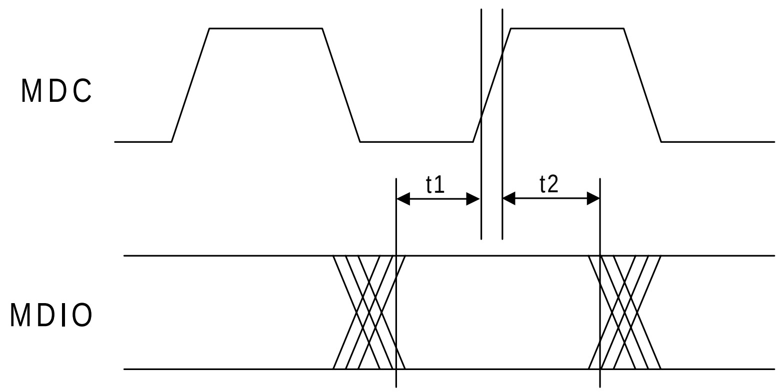


Figure 32: MDIO Read Timing (MDIO Sourced by PHY)

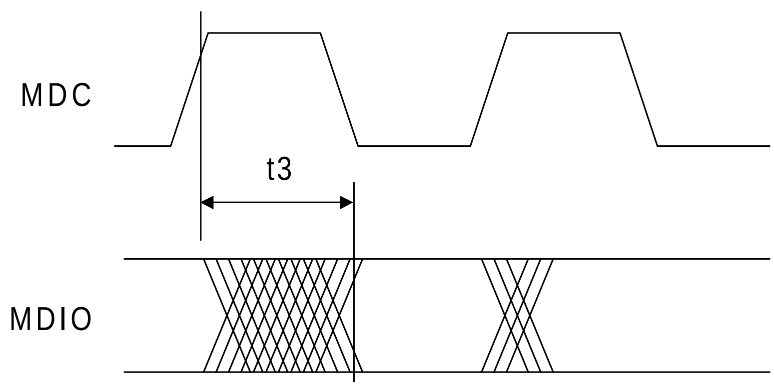


Table 33: MDIO Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
MDIO setup before MDC, sourced by STA	t1	10	–	–	ns	MDC = 2.5 MHz
		1	–	–	ns	MDC = 8 MHz
MDIO hold after MDC, sourced by STA	t2	10	–	–	ns	MDC = 2.5 MHz
		1	–	–	ns	MDC = 8 MHz
MDC to MDIO output delay, sourced by PHY	t3	10	–	300	ns	MDC = 2.5 MHz
		–	130	–	ns	MDC = 8 MHz

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 33: Power-Up Timing

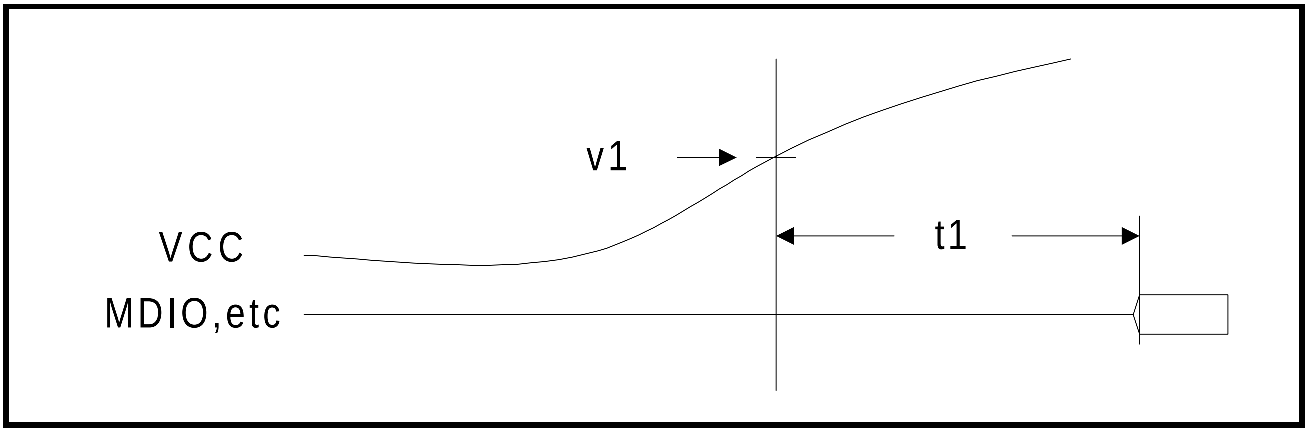


Table 34: Power-Up Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Voltage threshold	v1	–	2.9	–	V	–
Power Up delay	t1	–	–	500	ms	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 34: $\overline{\text{RESET}}$ And Power-Down Recovery Timing

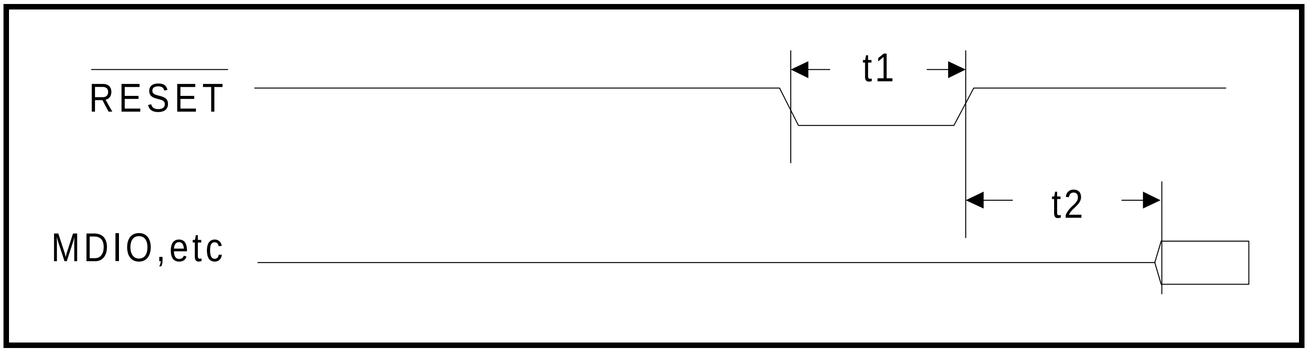


Table 35: $\overline{\text{RESET}}$ and Power-Down Recovery Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
$\overline{\text{RESET}}$ pulse width	t1	10	–	–	ns	–
$\overline{\text{RESET}}$ recovery delay	t2	–	1	–	ms	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

REGISTER DEFINITIONS

The LXT9763 register set includes multiple 16-bit registers. Refer to Table 36 for a complete register listing and to Table 37 for a complete bit map. Tables 38 through 53 provide additional details.

- Base registers (0 through 8) are defined in accordance with the "Reconciliation Sublayer and Media Independent Interface" and "Physical Layer Link Signaling for 10/100 Mbps Auto-Negotiation" sections of the IEEE 802.3 specification.
- Additional registers (16 through 30) are defined in accordance with the IEEE 802.3 specification for adding unique chip functions.

Table 36: Register Set

Address	Register Name	Bit Assignments
0	Control Register	Refer to Table 38 on page 54
1	Status Register	Refer to Table 39 on page 55
2	PHY Identification Register 1	Refer to Table 40 on page 56
3	PHY Identification Register 2	Refer to Table 41 on page 56
4	Auto-Negotiation Advertisement Register	Refer to Table 42 on page 57
5	Auto-Negotiation Link Partner Base Page Ability Register	Refer to Table 43 on page 58
6	Auto-Negotiation Expansion Register	Refer to Table 44 on page 59
7	Auto-Negotiation Next Page Transmit Register	Refer to Table 45 on page 59
8	Auto-Negotiation Link Partner Received Next Page Register	Refer to Table 46 on page 60
9	1000BASE-T/100BASE-T2 Control Register	Not Implemented
10	1000BASE-T/100BASE-T2 Status Register	Not Implemented
15	Extended Status Register	Not Implemented
16	Port Configuration Register	Refer to Table 47 on page 61
17	Quick Status Register	Refer to Table 48 on page 62
18	Interrupt Enable Register	Refer to Table 49 on page 63
19	Interrupt Status Register	Refer to Table 50 on page 64
20	LED Configuration Register	Refer to Table 51 on page 65
21-27	Reserved	
28	Transmit Control Register #1	Refer to Table 52 on page 67
29	Reserved	
30	Transmit Control Register #2	Refer to Table 53 on page 67
31	Reserved	

Table 37: Register Bit Map

Reg Title	Bit Fields																Addr
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Control Register																	
Control	Reset	Loopback	Speed Select	A/N Enable	Power Down	Isolate	Re-start A/N	Duplex Mode	COL Test	Speed Select	Reserved						**0**
Status Register																	
Status	100T4	100X Full Duplex	100X Half Duplex	10T Full Duplex	10T Half Duplex	100T2 Full Duplex	100T2 Half Duplex	Extended Status	Reserved	MF Preamble Suppress	A/N Complete	Remote Fault	A/N Ability	Link Status	Jabber Detect	Extended Capability	**1**
PHY ID Registers																	
PHY ID 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**2**
PHY ID2	PHY ID No						MFR Model No						MFR Rev No				**3**
Auto-Negotiation Advertisement Register																	
A/N Advertise	Next Page	Reserved	Remote Fault	Reserved	Asymm Pause	Pause	100T4	100TX Full Duplex	100TX	10T Full Duplex	10T	IEEE Selector Field					**4**
Auto-Negotiation Link Partner Base Page Ability Register																	
A/N Link Ability	Next Page	Ack	Remote Fault	Reserved	Asymm Pause	Pause	100T4	100TX Full Duplex	100TX	10T Full Duplex	10T	IEEE Selector Field					**5**
Auto-Negotiation Expansion Register																	
A/N Expansion	Reserved										Base Page	Parallel Detect Fault	Link Partner Next Page Able	Next Page Able	Page Received	Link Partner A/N Able	**6**
Auto-Negotiation Next Page Transmit Register																	
A/N Next Page Txmit	Next Page	Reserved	Message Page	Ack 2	Toggle	Message / Unformatted Code Field											**7**
Auto-Negotiation Link Partner Next Page Ability Register																	
A/N Next Page Rcv	Next Page	Ack	Message Page	Ack 2	Toggle	Message / Unformatted Code Field											**8**

Table 37: Register Bit Map – continued

Reg Title	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Addr
Port Configuration Register																	
Port Config	Reserved	Link Disable	Txmit Disable	Bypass Scrambler (100TX)	Bypass 4B/5B (100TX)	Jabber (10T)	SQE (10T)	TP Loopback (10T)	CRS Select (10T)	FIFO Size	PRE_EN	Reserved	Reserved	Reserved	Alternate Next Page	Fiber Select	**16**
Quick Status Register																	
Quick Status	Reserved	10/100 Mode	Transmit Status	Receiver Status	Collision Status	Link	Duplex Mode	Auto-Neg	Auto-Neg Complete	Reserved	Polarity	Pause	Error	PLL Lock Error	Reserved	Reserved	**17**
Interrupt Enable Register																	
Interrupt Enable	Reserved							Counter Mask	Auto-Neg Mask	Speed Mask	Duplex Mask	Link Mask	Reserved	Reserved	Interrupt Enable	Test Interrupt	**18**
Interrupt Status Register																	
Interrupt Status	Reserved							Counter Full	Auto-Neg Done	Speed Change	Duplex Change	Link Change	Reserved	MD Interrupt	XTAL OK	Reserved	**19**
LED Configuration Register																	
LED Config	LED1				LED2				LED3				LED Freq		Pulse Stretch	Reserved/ Invalid Polarity	**20**
Transmit Control Register #1																	
Analog #1	Line Length			Reserved									Bandwidth Control		Slew Control		**28**
Transmit Control Register #2																	
Analog #2	Reserved		Driver Amp	Reserved													**30**

Table 38: Control Register (Address 0)

Bit	Name	Description	Type [1]	Default
0.15	Reset	1 = PHY reset. 0 = Normal operation.	R/W SC	0
0.14	Loopback	1 = Enable loopback mode. 0 = Disable loopback mode.	R/W	0
0.13	Speed Selection	<u>0.6</u> <u>0.13</u> 1 1 = Reserved. 1 0 = 1000 Mbps (not allowed). 0 1 = 100 Mbps. 0 0 = 10 Mbps.	R/W	Note 2 00
0.12	Auto-Negotiation Enable[3]	1 = Enable Auto-Negotiation Process. 0 = Disable Auto-Negotiation Process.	R/W	Note 2 0
0.11	Power-Down	1 = Power-down. 0 = Normal operation.	R/W	0
0.10	Isolate	1 = Electrically isolate PHY from MII. 0 = Normal operation.	R/W	0
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process. 0 = Normal operation.	R/W SC	0
0.8	Duplex Mode	1 = Full-Duplex. 0 = Half-Duplex.	R/W	Note 2 0
0.7	Collision Test	This bit is ignored by the LXT9763. 1 = Enable COL signal test. 0 = Disable COL signal test.	R/W	0
0.6	Speed Selection 1000 Mb/s	<u>0.6</u> <u>0.13</u> 1 1 = Reserved. 1 0 = 1000 Mbps (not allowed). 0 1 = 100 Mbps. 0 0 = 10 Mbps.	R/W	00
0.5:0	Reserved	Write as 0, ignore on Read	R/W	00000

1. R/W = Read/Write.
   RO = Read Only.
   SC = Self Clearing when read.
2. Default value of bits 0.12, 0.13 and 0.8 are determined by the LED/CFG pins (refer to Table 7 on page 16).
3. Do not enable Auto-Negotiation if Fiber Mode is selected.

Table 39: Status Register (Address 1)

Bit	Name	Description	Type [1]	Default
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4. 0 = PHY not able to perform 100BASE-T4.	RO	0
1.14	100BASE-X Full-Duplex	1 = PHY able to perform full-duplex 100BASE-X. 0 = PHY not able to perform full-duplex 100BASE-X.	RO	1
1.13	100BASE-X Half-Duplex	1 = PHY able to perform half-duplex 100BASE-X. 0 = PHY not able to perform half-duplex 100BASE-X.	RO	1
1.12	10 Mbps Full-Duplex	1 = PHY able to operate at 10 Mbps in full-duplex mode. 0 = PHY not able to operate at 10 Mbps full-duplex mode.	RO	1
1.11	10 Mbps Half-Duplex	1 = PHY able to operate at 10 Mbps in half-duplex mode. 0 = PHY not able to operate at 10 Mbps in half-duplex.	RO	1
1.10	100BASE-T2 Full-Duplex	1 = PHY able to perform full-duplex 100BASE-T2. 0 = PHY not able to perform full-duplex 100BASE-T2.	RO	0
1.9	100BASE-T2 Half-Duplex	1 = PHY able to perform half duplex 100BASE-T2. 0 = PHY not able to perform half-duplex 100BASE-T2.	RO	0
1.8	Extended Status	1 = Extended status information in register 15. 0 = No extended status information in register 15.	RO	0
1.7	Reserved	1 = ignore when read.	RO	0
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed. 0 = PHY will not accept management frames with preamble suppressed.	RO	0
1.5	Auto-Negotiation complete	1 = Auto-Negotiation complete. 0 = Auto-Negotiation not complete.	RO	0
1.4	Remote Fault[2]	1 = Remote fault condition detected. 0 = No remote fault condition detected.	RO/LH	0
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation. 0 = PHY is not able to perform Auto-Negotiation.	RO	1
1.2	Link Status	1 = Link is up. 0 = Link is down.	RO/LL	0
1.1	Jabber Detect	1 = Jabber condition detected. 0 = Jabber condition not detected.	RO/LH	0
1.0	Extended Capability	1 = Extended register capabilities. 0 = Extended register capabilities.	RO	1

1. RO = Read Only.
   LL = Latching Low.
   LH = Latching High.
2. Bit 1.4 is not valid if Auto-Negotiation is selected while operating in Fiber mode.

Table 40: PHY Identification Register 1 (Address 2)

Bit	Name	Description	Type [1]	Default
2.15:0	PHY ID Number	The PHY identifier composed of bits 3 through 18 of the OUI.	RO	0013 hex

1. RO = Read Only.

Table 41: PHY Identification Register 2 (Address 3)

Bit	Name	Description	Type [1]	Default
3.15:10	PHY ID number	The PHY identifier composed of bits 19 through 24 of the OUI.	RO	011110
3.9:4	Manufacturer's model number	6 bits containing manufacturer's part number.	RO	001001
3.3:0	Manufacturer's revision number	4 bits containing manufacturer's revision number.	RO	XXXX

1. RO = Read Only.

Figure 35: PHY Identifier Bit Mapping

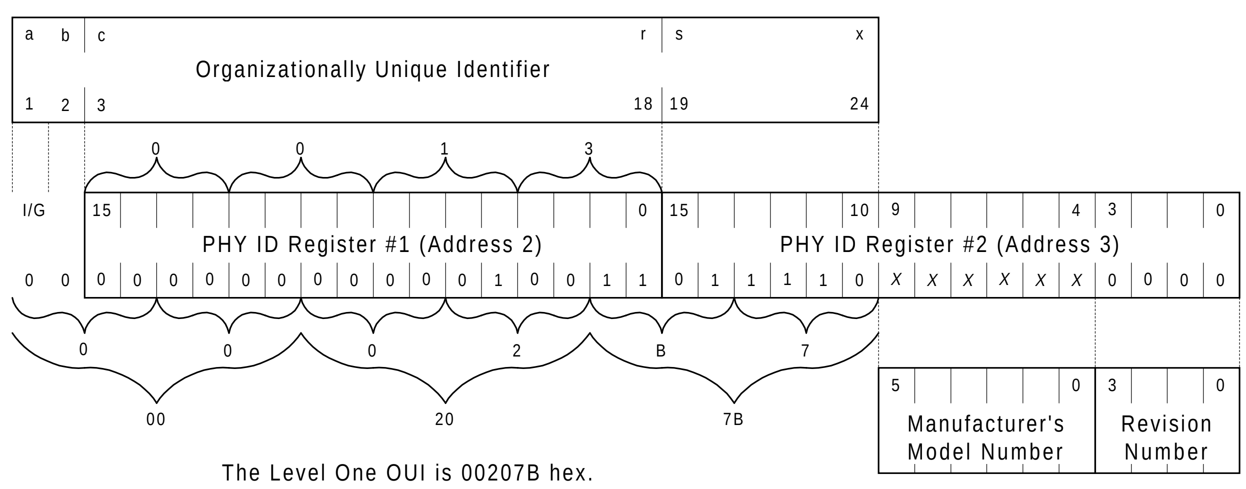


Table 42: Auto Negotiation Advertisement Register (Address 4)

Bit	Name	Description	Type [1]	Default
4.15	Next Page	1 = Port has ability to send multiple pages. 0 = Port has no ability to send multiple pages.	R/W	0
4.14	Reserved	Ignore.	RO	0
4.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	R/W	0
4.12	Reserved	Ignore.	R/W	0
4.11	Asymmetric Pause	Pause operation defined in Clause 40 and 27.	R/W	0
4.10	Pause	1 = Pause operation enabled for full-duplex links. 0 = Pause operation disabled.	R/W	0
4.9	100BASE-T4	1 = 100BASE-T4 capability is available. 0 = 100BASE-T4 capability is not available. (The LXT9763 does not support 100BASE-T4 but allows this bit to be set to advertise in the Auto-Negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver could be switched in if this capability is desired.)	R/W	0
4.8	100BASE-TX full-duplex	1 = Port is 100BASE-TX full-duplex capable. 0 = Port is not 100BASE-TX full-duplex capable.	R/W	0 Note 2
4.7	100BASE-TX	1 = Port is 100BASE-TX capable. 0 = Port is not 100BASE-TX capable.	R/W	0 Note 2
4.6	10BASE-T full-duplex	1 = Port is 10BASE-T full-duplex capable. 0 = Port is not 10BASE-T full-duplex capable.	R/W	0 Note 2
4.5	10BASE-T	1 = Port is 10BASE-T capable. 0 = Port is not 10BASE-T capable.	R/W	0 Note 2
4.4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future Auto-Negotiation development. <11111> = Reserved for future Auto-Negotiation development. Unspecified or reserved combinations should not be transmitted.	R/W	00001

1. R/W = Read/Write.
   RO = Read Only.
2. Default value of bits 4.8:5 are determined by hardware pins at Reset. Refer to Reset discussion on page 15.

Table 43: Auto Negotiation Link Partner Base Page Ability Register (Address 5)

Bit	Name	Description [1]	Type [2]	Default
5.15	Next Page	1 = Link Partner has ability to send multiple pages. 0 = Link Partner has no ability to send multiple pages.	RO	0
5.14	Acknowledge	1 = Link Partner has received Link Code Word from LXT9763. 0 = Link Partner has not received Link Code Word from the LXT9763.	RO	0
5.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	RO	0
5.12	Reserved	Ignore.	RO	0
5.11	Asymmetric Pause	Pause operation defined in Clause 40 and 27. 1 = Link Partner is Pause capable. 0 = Link Partner is not Pause capable.	RO	0
5.10	Pause	1 = Link Partner is Pause capable. 0 = Link Partner is not Pause capable.	RO	0
5.9	100BASE-T4	1 = Link Partner is 100BASE-T4 capable. 0 = Link Partner is not 100BASE-T4 capable.	RO	0
5.8	100BASE-TX full-duplex	1 = Link Partner is 100BASE-TX full-duplex capable. 0 = Link Partner is not 100BASE-TX full-duplex capable.	RO	0
5.7	100BASE-TX	1 = Link Partner is 100BASE-TX capable. 0 = Link Partner is not 100BASE-TX capable.	RO	0
5.6	10BASE-T full-duplex	1 = Link Partner is 10BASE-T full-duplex capable. 0 = Link Partner is not 10BASE-T full-duplex capable.	RO	0
5.5	10BASE-T	1 = Link Partner is 10BASE-T capable. 0 = Link Partner is not 10BASE-T capable.	RO	0
5.4:0	Selector Field S<4:0>	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future Auto-Negotiation development. <11111> = Reserved for future Auto-Negotiation development. Unspecified or reserved combinations shall not be transmitted.	RO	00000

1. Per the 1997 revision of IEEE 802.3, this register is no longer used to store Link Partner next pages. Register 8 (Table 46 on page 60) is now used for that purpose.
2. RO = Read Only.

Table 44: Auto Negotiation Expansion (Address 6)

Bit	Name	Description	Type [1]	Default
6.15:6	Reserved	Ignore on read.	RO	0
6.5	Base Page	This bit indicates the status of the Auto_Negotiation variable, base page. It flags synchronization with the Auto_Negotiation state diagram allowing detection of interrupted links. This bit is only used if bit 16.1 (Alternate NP feature) is set. 1 = base_page = true. 0 = base_page = false.	RO	0
6.4	Parallel Detection Fault	1 = Parallel detection fault has occurred. 0 = Parallel detection fault has not occurred.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link partner is next page able. 0 = Link partner is not next page able.	RO	0
6.2	Next Page Able	1 = Local device is next page able. 0 = Local device is not next page able.	RO	1
6.1	Page Received	1 = Indicates that a new page has been received as and the received code word has been loaded into register 5 (base pages) or register 8 (next pages) as specified in clause 28 of 802.3. This bit will be cleared on read. If bit 16.1 is set, the Page Received bit will also be cleared when mr_page_rx = false or transmit_disable = true.	RO LH	0
6.0	Link Partner A/N Able	1 = Link partner is auto-negotiation able. 0 = Link partner is not auto-negotiation able.	RO	0

1. RO = Read Only.
LH = Latching High.

Table 45: Auto Negotiation Next Page Transmit Register (Address 7)

Bit	Name	Description	Type [1]	Default
7.15	Next Page (NP)	1 = Additional next pages follow. 0 = Last page.	R/W	0
7.14	Reserved	Write as 0, ignore on read.	RO	0
7.13	Message Page (MP)	1 = Message page. 0 = Unformatted page.	R/W	1

1. RO = Read Only.
R/W = Read/Write

Table 45: Auto Negotiation Next Page Transmit Register (Address 7) – continued

Bit	Name	Description	Type [1]	Default
7.12	Acknowledge 2 (ACK2)	1 = Will comply with message. 0 = Can not comply with message.	R/W	0
7.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero. 0 = Previous value of the transmitted Link Code Word equalled logic one.	R/W	0
7.10:0	Message/Unformatted Code Field		R/W	0000000 0001

1. RO = Read Only.
R/W = Read/Write

Table 46: Auto Negotiation Link Partner Next Page Receive Register (Address 8)

Bit	Name	Description	Type [1]	Default
8.15	Next Page (NP)	1 = Link Partner has additional next pages to send. 0 = Link Partner has no additional next pages to send.	RO	0
8.14	Acknowledge (ACK)	1 = Link Partner has received Link Code Word from LXT9763 .0 = Link Partner has not received Link Code Word from LXT9763.	RO	0
8.13	Message Page (MP)	1 = Page sent by the Link Partner is a Message Page. 0 = Page sent by the Link Partner is an Unformatted Page.	RO	0
8.12	Acknowledge 2 (ACK2)	1 = Link Partner Will comply with the message. 0 = Link Partner can not comply with the message.	RO	0
8.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero. 0 = Previous value of the transmitted Link Code Word equalled logic one.	RO	0
8.10:0	Message/Unformatted Code Field	User definable.	RO	0

1. RO = Read Only.

NOTE

Registers 9, 10 and 15 are not implemented.
These registers only have meaning for 100BASE-T2 and 1000BASE-T, neither of which are supported by this device.

Table 47: Port Configuration Register (Address 16, Hex 10)

Bit	Name	Description	Type [1]	Default
16.15	Reserved	Write as zero, ignore on read.	R/W	0
16.14	Force Link Pass	1 = Force Link Pass. Sets appropriate registers, state machines and LEDs to Pass condition, regardless of actual link state. 0 = Normal operation.	R/W	0
16.13	Transmit Disable	1 = Disable Twisted Pair transmitter. 0 = Normal Operation.	R/W	0
16.12	Bypass Scrambler (100BASE-TX)	1 = Bypass Scrambler and Descrambler. 0 = Normal Operation.	R/W	0
16.11	Bypass 4B5B (100BASE-TX)	1 = Bypass 4B5B encoder and decoder. 0 = Normal Operation.	R/W	0
16.10	Jabber (10BASE-T)	1 = Disable Jabber. 0 = Normal operation.	R/W	0
16.9	SQE (10BASE-T)	1 = Enable Heart Beat. 0 = Disable Heart Beat.	R/W	0
16.8	TP Loopback (10BASE-T)	1 = Disable TP loopback during half-duplex operation. 0 = Normal Operation.	R/W	0
16.7	CRS Select (10BASE-T)	1 = CRS deassert extends to RX_DV deassert. 0 = Normal Operation.	R/W	1
16.6	Reserved	Write as zero, ignore on read.	R/W	0
16.5	Preamble Enable (10BASE-T)	0 = Set RX_DV high coincident with SFD. (Strip off received preamble before sending data stream to MAC via MII.) 1 = Set RX_DV high and RXD=preamble when CRS is asserted.	R/W	0
16.4	Reserved	Write as zero, ignore on read.	R/W	0
16.3	Reserved	Write as zero, ignore on read.	R/W	0
16.2	Reserved	Write as zero, ignore on read.	R/W	0
16.1	Alternate NP feature	1 = Enable alternate auto negotiate next page feature. 0 = Disable alternate auto negotiate next page feature.	R/W	0
16.0	Fiber Select	1 = Select fiber mode for this port. 0 = Select TP mode for this port.	R/W	0

1. R/W = Read /Write.

Table 48: Quick Status Register (Address 17, Hex 11)

Bit	Name	Description	Type [1]	Default
17.15	Reserved	Always 0.	RO	0
17.14	10/100 Mode	1 = LXT9763 is operating in 100BASE-TX mode. 0 = LXT9763 is not operating 100BASE-TX mode.	RO	0
17.13	Transmit Status	1 = LXT9763 is transmitting a packet. 0 = LXT9763 is not transmitting a packet.	RO	0
17.12	Receive Status	1 = LXT9763 is receiving a packet. 0 = LXT9763 is not receiving a packet.	RO	0
17.11	Collision Status	1 = Collision is occurring. 0 = No collision.	RO	0
17.10	Link	1 = Link is up. 0 = Link is down.	RO	0
17.9	Duplex Mode	1 = Full-duplex. 0 = Half-duplex.	RO	0
17.8	Auto-Negotiation	1 = LXT9763 is in Auto-Negotiation Mode. 0 = LXT9763 is in manual mode.	RO	0
17.7	Auto-Negotiation Complete	1 = Auto-negotiation process completed. 0 = Auto-negotiation process not completed. This bit is only valid when auto negotiate is enabled, and is equivalent to bit 1.5.	RO	0
17.6	Reserved	Reserved.	RO	0
17.5	Polarity	1= Polarity is reversed. 0= Polarity is not reversed.	RO	0
17.4	Pause	1 = Link Partner Pause capable. 0 = Link Partner not Pause capable. This bit is equivalent to bit 5.10.	RO	0
17:3	Error	1 = Error Occurred (Remote Fault, X,Y,Z). 0 = No error occurred.	RO	0
17.2:0	Reserved	Write as zero, ignore on read.	RO	0

1. RO = Read Only.

Table 49: Interrupt Enable Register (Address 18, Hex 12)

Bit	Name	Description	Type [1]	Default
18.15:8	Reserved	Write as 0; ignore on read.	R/W	N/A
18.7	ANMSK	Mask for Auto Negotiate Complete. 1 = Enable event to cause interrupt. 0 = Do not allow event to cause interrupt.	R/W	0
18.6	SPEEDMSK	Mask for Speed Interrupt. 1 = Enable event to cause interrupt. 0 = Do not allow event to cause interrupt.	R/W	0
18.5	DUPLEXMSK	Mask for Duplex Interrupt. 1 = Enable event to cause interrupt. 0 = Do not allow event to cause interrupt.	R/W	0
18.4	LINKMSK	Mask for Link Status Interrupt. 1 = Enable event to cause interrupt. 0 = Do not allow event to cause interrupt.	R/W	0
18.3	Reserved	Write as zero, ignore on read.	R/W	0
18.2	Reserved	Write as 0, ignore on read.	R/W	0
18.1	INTEN	Interrupt Enable. 1 = Enable interrupts on this port. 0 = Disable interrupts on this port.	R/W	0
18.0	TINT	Test Interrupt. 1 = Force interrupt on $\overline{\text{MDINT}}$. 0 = Normal operation.	R/W	0

1. R/W = Read /Write.

Table 50: Interrupt Status Register (Address 19, Hex 13)

Bit	Name	Description	Type [1]	Default
19.15:8	Reserved	Ignore.	RO	N/A
19.7	ANDONE	Auto Negotiation Status. 1= Auto Negotiation has completed. 0= Auto Negotiation has not completed.	RO/SC	N/A
19.6	SPEEDCHG	Speed Change Status. 1 = A Speed Change has occurred since last reading this register. 0 = A Speed Change has not occurred since last reading this register.	RO/SC	0
19.5	DUPLEXCHG	Duplex Change Status. 1 = A Duplex Change has occurred since last reading this register. 0 = A Duplex Change has not occurred since last reading this register.	RO/SC	0
19.4	LINKCHG	Link Status Change Status. 1 = A Link Change has occurred since last reading this register. 0 = A Link Change has not occurred since last reading this register.	RO/SC	0
19.3	Reserved	Write as zero, ignore on read.	RO/SC	0
19.2	MDINT	1 = MII interrupt pending. 0 = No MII interrupt pending.	RO/SC	
19.1:0	Reserved	Ignore.	RO	0

1. R/O = Read Only.
SC = Self Clearing when read.

Table 51: LED Configuration Register (Address 20, Hex 14)

Bit	Name	Description	Type [1]	Default
20.15:12	LED1 Programming bits	0000 = Display Speed Status (Continuous, Default) 0001 = Display Transmit Status (Stretched) 0010 = Display Receive Status (Stretched) 0011 = Display Collision Status (Stretched) 0100 = Display Link Status (Continuous) 0101 = Display Duplex Status (Continuous)[5] 0110 = Reserved 0111 = Display Receive or Transmit Activity (Stretched) 1000 = Test mode- turn LED on (Continuous) 1001 = Test mode- turn LED off (Continuous) 1010 = Test mode- blink LED fast (Continuous) 1011 = Test mode- blink LED slow (Continuous) 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3,5] 1111 = Reserved	R/W	0000
20.11:8	LED2 Programming bits	0000 = Display Speed Status 0001 = Display Transmit Status 0010 = Display Receive Status 0011 = Display Collision Status 0100 = Display Link Status (Default) 0101 = Display Duplex Status 0110 = Reserved 0111 = Display Receive or Transmit Activity 1000 = Test mode- turn LED on 1001 = Test mode- turn LED off 1010 = Test mode- blink LED fast 1011 = Test mode- blink LED slow 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3,5] 1111 = Reserved	R/W	0100

1. R/W = Read /Write.
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up.
   The secondary LED driver (Receive, Activity or Isolate) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full duplex.
   Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Duplex LED maybe active for a brief time after loss of link.

Table 51: LED Configuration Register (Address 20, Hex 14) – continued

Bit	Name	Description	Type [1]	Default
20.7:4	LED3 Programming bits	0000 = Display Speed Status 0001 = Display Transmit Status 0010 = Display Receive Status (Default) 0011 = Display Collision Status 0100 = Display Link Status 0101 = Display Duplex Status[5] 0110 = Reserved 0111 = Display Receive or Transmit Activity 1000 = Test mode- turn LED on 1001 = Test mode- turn LED off 1010 = Test mode- blink LED fast 1011 = Test mode- blink LED slow 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3,5] 1111 = Reserved	R/W	0010
20.3:2	LEDFREQ	00 = Stretch LED events to 30 ms. 01 = Stretch LED events to 60 ms. 10 = Stretch LED events to 100 ms. 11 = Reserved.	R/W	00
20.1	PULSE-STRETCH	0 = Disable pulse stretching of all LEDs. 1 = Enable pulse stretching of all LEDs.	R/W	1
20.0	Reserved		R/W	0

1. R/W = Read /Write.
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up.
The secondary LED driver (Receive, Activity or Isolate) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full duplex.
Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Duplex LED maybe active for a brief time after loss of link.

Table 52: Transmit Control Register #1 (Address 28)

Bit	Name	Description	Type[2]	Default
28.15:4	Reserved	Ignore.	R/W	N/A
28.3:2	Bandwidth Control [1]	00 = Nominal Differential Amp Bandwidth 01 = Slower 10 = Fastest 11 = Faster	R/W	00
28.1:0	Risetime Control	00 = 2.5ns 01 = 3.1ns 10 = 3.7ns 11 = 4.3ns	R/W	Note 3

1. Transmit Control functions are approximations. They are not guaranteed and not subject to production testing.
2. RO = Read Only.
   R/W = Read/Write.
3. The default setting of bits 28.1:0 (Risetime) are determined by pins 77 and 76.

Table 53: Transmit Control Register #2 (Address 30)

Bit	Name	Description	Type	Default
30.15:14	Reserved		R/W	N/A
30.13	Increase Driver Amplitude	1 = Increase Driver Amplitude 5% in all modes. 0 = Normal operation.	R/W	0
30.12:0	Reserved		R/W	N/A

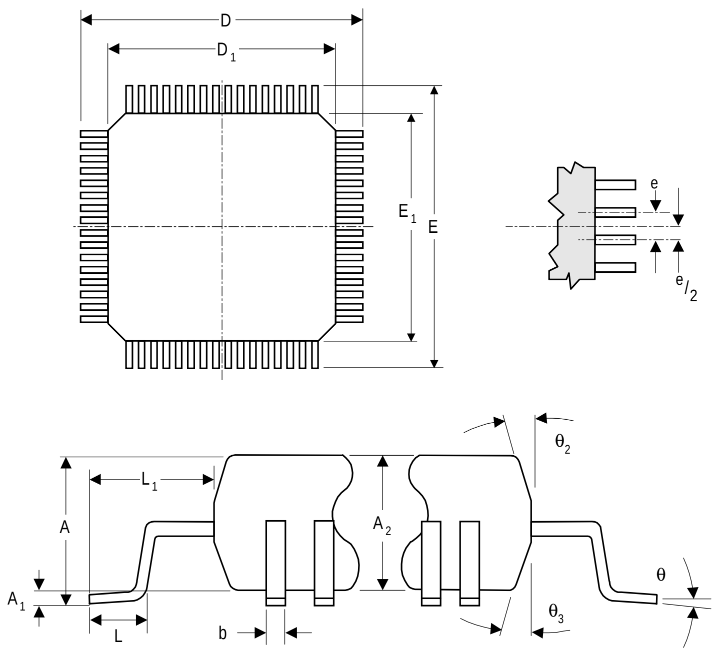
1. RO = Read Only.

PACKAGE SPECIFICATIONS

Figure 36: LXT9763 Package Specification

208-Pin Plastic Quad Flat Package

- Part Number LXT9763HC
- Commercial Temperature Range (0°C to 70°C)



Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
q	0°	7°
θ_2	5°	16°
θ_3	5°	16°

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REVISION HISTORY

Table 54: Changes from Rev 1.1 to Rev 1.2 (04/20/00)

Section	Page	Change	Text
MII Operation	18	Delete	Remove 4th sentence in 2nd para: “A serial MII mode is available via bit 16.3 for 10M operation.”
Figure 25 and Table 28 10BASE-T Receive Timing (Parameters)	45	Delete	Remove “Parallel Mode” from headings of both figure and table.
Figure 26 and Figure 29 10BASE-T Transmit Timing (Parameters)	46	Delete	Remove “Parallel Mode” from headings of both figure and table.
Old Figure 27 and Table 30 10BASE-T Transmit Timing (Parameters) Serial Mode	47 (old)	Delete	Delete both figure and table.
Old Figure 28 and Table 31 10BASE-T Receive Start of Frame Timing (Parameters) Serial Mode	48 (old)	Delete	Delete both figure and table.
Old Figure 29 and Table 32 10BASE-T Receive End of Frame Timing (Parameters) Serial Mode	49 (old)	Delete	Delete both figure and table.

Table 55: Changes From Rev 1.0 to Rev 1.1(03/15/00)

Section	Page	Change	Text
Features	1	Modify	Increased power consumption to 380 mW per port.
Table 1: MII Signal Descriptions.	5	Modify	Delete 2.5 MHz for data clock on pin # 95.
Table 4: Power Supply Signal Descriptions	9	Modify	Delete 2.5V reference and “Digital I/O circuits may be supplied with 2.5 or 3.3V.” for VCCIO.
Twisted-Pair Interface description	12	Add	Added statement that high receive impedance has no effect on external termination.
Table 11: Supported JTAG Instructions	28	Modify	Reformat Codes and add Clamp
Boundary Scan description	28	Add	Added Table 12: Device ID Register. Renumbered subsequent tables.
The Twisted-Pair Interface	31	Add	Values added 370mA and 560 mA. (Bullet 6)

Table 55: Changes From Rev 1.0 to Rev 1.1(03/15/00) – continued

Section	Page	Change	Text
Figure 17 Typical Twisted-Pair Interface	33	Add	.01µF Capacitor added to drawing for note 1. and value added for ferrite bead 560mA
Table 14: Absolute Maximum Ratings	35	Add	Added Values for Supply Voltage: Vcc Max 4.0V and Operating Temperature at 70 C Max and O C Min for TOPA.
Table 15: Operating Conditions	35	Add	Added Typical Values for VCCA, VCCD & VCCIO @ 3.3 Typ. Vcc Current 115mA Typ and 130 Max for 100 BASE-TX, 10BASE-TX and Auto-negotiation Icc values. Also delete Power Down Mode. VCCIO to 3.15 V min.
Test Specifications	35	Modify	Changed Test Spec note to indicate product release (from "target specifications... not guaranteed" to "guaranteed by test except where noted 'by design'".
Table 18: Reference Clock Characteristics	36	Modify	Increased clock frequency tolerance from 50 to 100 ppm.
Table 19: 100BASE-TX Transceiver Characteristics	37	Modify	Duty Cycle distortion change to ± 0.5 ns
Table 20: 100BASE-FX Transceiver Characteristics	37	Add	Jitter value added at 1.4 ns Changed max rise/fall time to 1.9 ns. Changed max CMIR to Vcc - 0.7 V.
Table 21: 10BASE-T Transceiver Characteristics	38	Add	Values added for Receiver Link Min & Max Deleted unspecified parameter Zin
Table 22: 100BASE-TX Receiver Timing (4B Mode)	39	Add	Added min and max values for COL and CRS timing.
Table 23: 100BASE-TX Transmit Timing Parameters (4B Mode)	40	Add	Values added for t3 = 44ns Typ. t4 = 52ns Typ.
Table 24: 100BASE-TX Receiver Timing (5B Mode)	41	Modify	Changed typical values for COL and CRS timing.
Table 25: 100BASE-TX Transmit Timing Parameters (5B Mode)	42	Add	Values added for t3 = 44ns Typ. t4 = 52ns Typ. Decreased typical value for t5 (latency).
Table 26: 100BASE-FX Receive Timing Parameters	43	Add	Values added for t6 = 10 BT Typ. t7 = 14 BT Typ.
Table 27: 100BASE-FX Transmit Timing Parameters	44	Add	Values added for t3 = 3 BT Typ. t4 = 4 BT Typ.
Table 28: 10BASE-T Receive Timing Parameters	45	Add	Value added for t4 = 18 BT Typ.
Table 32: Auto-Negotiation and Fast Link Pulse Parameters	48	Add	Values added for t1 = 100 ns Typ. t4 = 2 ms Typ.
Table 33: MDIO Timing Parameters	49	Add	Values added for t1 = 1ns Min. t2 = 1ns Min. t3 = 130 ns Typ. Combined Figures and Tables for MDIO at 2.5 MHz and 8 MHz. Re-numbered subsequent Figures & Tables.

Table 55: Changes From Rev 1.0 to Rev 1.1(03/15/00) – continued

Section	Page	Change	Text
Table 34: Power-Up Timing Parameters	50	Add	Value added for v1 = 2.9 V Typ.
Table 35: Reset and Power-Down Timing Parameters	50	Add	Value added for t1 = 10 ns min.
Table 48: Quick Status Register	62	Modify	Removed reference to PLL Lock indication and marked associated bit 17.2 as Reserved.
Table 50: Interrupt Status Register	64	Modify	Removed reference to XTAL Status indication and marked associated bit 19.1 as Reserved.
Table 51: LED Configuration Register	65	Add	Added note 5.
Table 52: Transmit Control Register #1	67	Modify	Removed reference to Line Length indication and marked associated bits as Reserved.

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Revision	Date	Status
1.2	04/00	See Revision History on page 69.
1.1	03/15	Updated.

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