Lyontek Inc.

LY611024

Rev. 1.4

128K X 8 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Delete Icc1 Spec.	Sep.21.2004
Rev. 1.2	Add E/I grade	Apr.7.2005
Rev. 1.3	Revised V_{TERM} to V_{T1} and V_{T2} Revised Test Condition of I_{SB1}/I_{DR} Added LL Spec.	Feb.2.2009
Rev. 1.4	Revised Test Condition of I_{CC}/I_{SB} Revised **FEATURES** & **ORDERING INFORMATION** **Lead free and green package available** to **Green package available** Deleted T_{SOLDER} in **ABSOLUTE MAXIMUN RATINGS** Added packing type in **ORDERING INFORMATION**	Apr.17.2009

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Rev. 1.4

128K X 8 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 12/15ns
- Low power consumption:
  Operating current : 50/40mA (TYP.)
  Standby current : 1mA (TYP.)
  2μA (TYP.) LL -version
- Single 4.5V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 32-pin 300 mil SOJ
  32-pin 8mm x 20mm TSOP-I
  32-pin 8mm x 13.4mm STSOP

GENERAL DESCRIPTION

The LY611024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

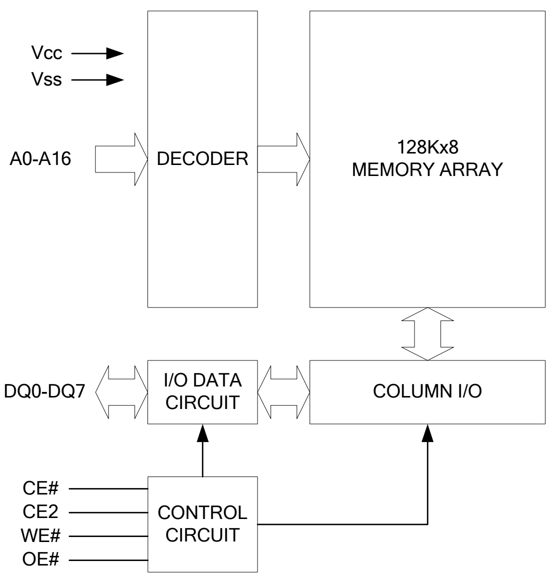
The LY611024 is well designed for very high speed system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY611024 operates from a single power supply of 4.5V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(Icc,TYP.)
LY611024	0 ~ 70℃	4.5 ~ 5.5V	12/15ns	1mA	50/40mA
LY611024(E)	-20 ~ 80℃	4.5 ~ 5.5V	12/15ns	1mA	50/40mA
LY611024(I)	-40 ~ 85℃	4.5 ~ 5.5V	12/15ns	1mA	50/40mA
LY611024(LL)	0 ~ 70℃	4.5 ~ 5.5V	12/15ns	2μA	50/40mA
LY611024(LLE)	-20 ~ 80℃	4.5 ~ 5.5V	12/15ns	2μA	50/40mA
LY611024(LLI)	-40 ~ 85℃	4.5 ~ 5.5V	12/15ns	2μA	50/40mA

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

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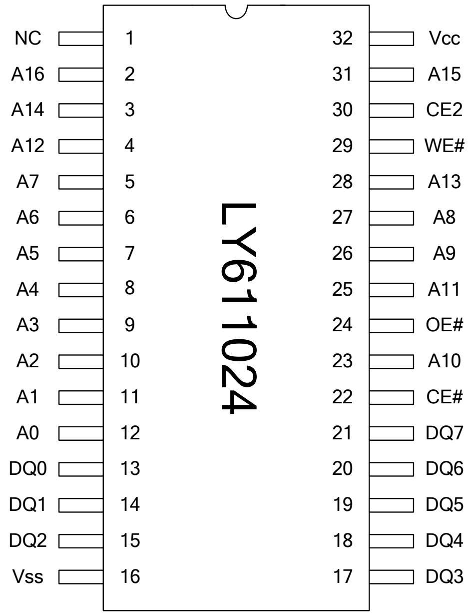
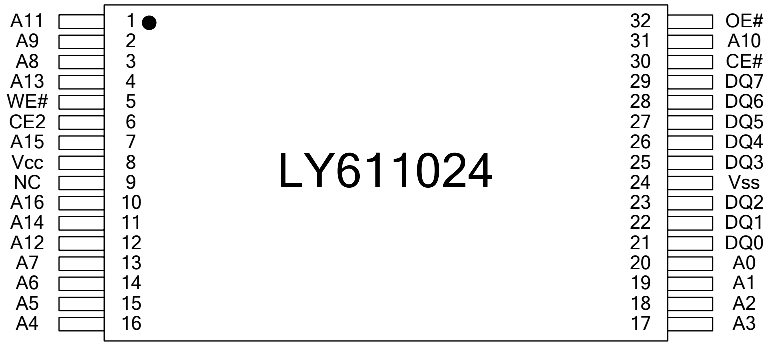
PIN CONFIGURATION



SOJ



TSOP-I/STSOP

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade)	℃
		-20 to 80(E grade)	℃
		-40 to 85(I grade)	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I_{SB},I_{SB1}
	X	L	X	X	High-Z	I_{SB},I_{SB1}
Output Disable	L	H	H	H	High-Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			4.5	5.0	5.5	V
Input High Voltage	V_{IH} *1			2.4	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL} *2			- 0.5	-	0.8	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -4mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = V_{IL} and CE2 = V_{IH}, $I_{I/O}$ = 0mA Others at V_{IL} or V_{IH}	- 12	-	50	80	mA
			- 15	-	40	65	mA
Standby Power Supply Current	I_{SB}	CE# = V_{IH} or CE2 = V_{IL} Others at V_{IL} or V_{IH}		-	3	20	mA
	I_{SB1}	CE# $\geqq V_{CC}$-0.2V or CE2 $\leqq$ 0.2V	Normal	-	1	5	mA
		CE# $\geqq V_{CC}$-0.2V or CE2 $\leqq$ 0.2V Others at 0.2V or V_{CC}-0.2V	LL	-	2	50	µA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -4mA/8mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY611024-12		LY611024-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	12	-	15	-	ns
Address Access Time	t_{AA}	-	12	-	15	ns
Chip Enable Access Time	t_{ACE}	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	6	-	7	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	3	-	4	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	0	-	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	6	-	7	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	ns

(2) WRITE CYCLE

PARAMETER	SYM.	LY611024-12		LY611024-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	10	-	12	-	ns
Chip Enable to End of Write	t_{CW}	10	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	7	-	8	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	3	-	4	-	ns
Write to Output in High-Z	t_{WHZ}*	-	7	-	8	ns

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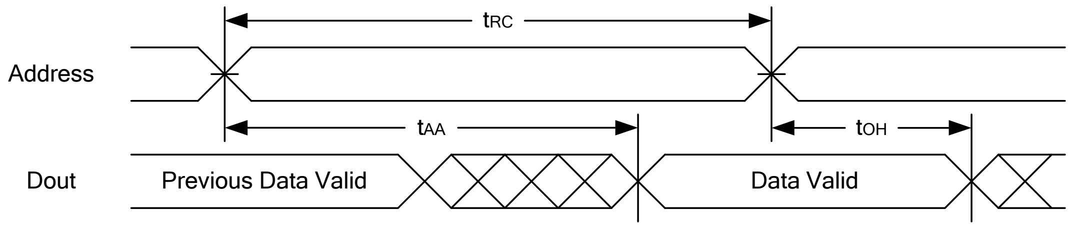
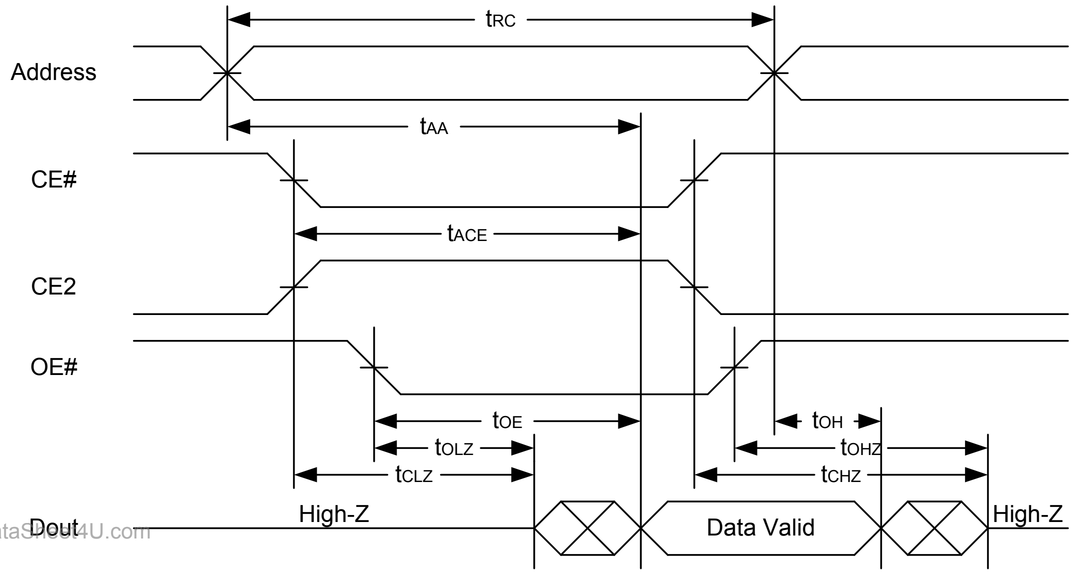
TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

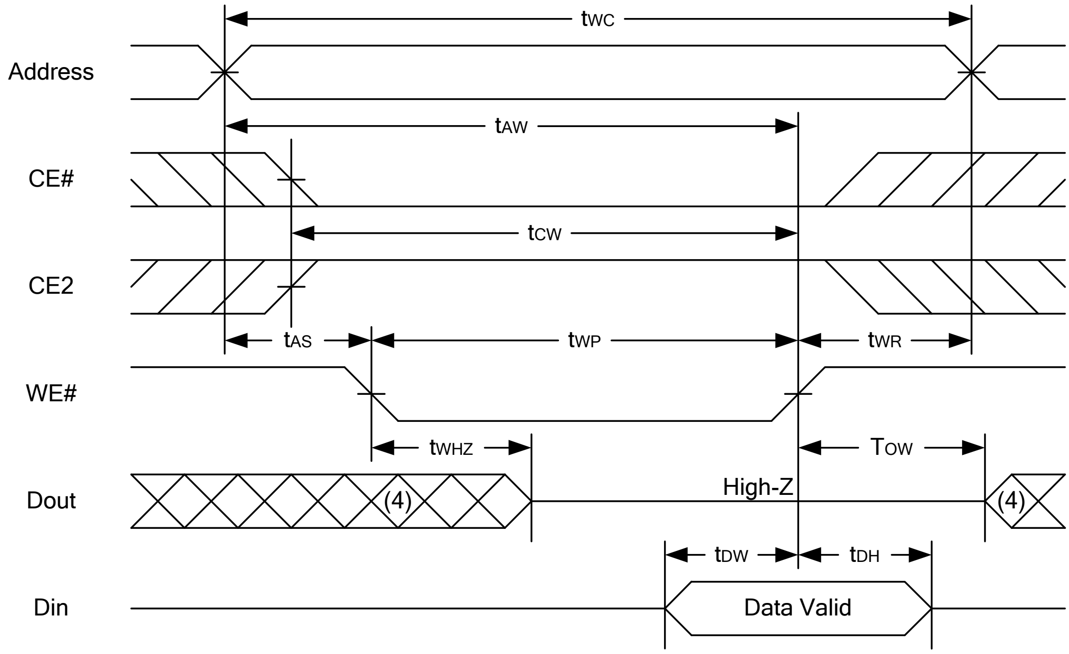


READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

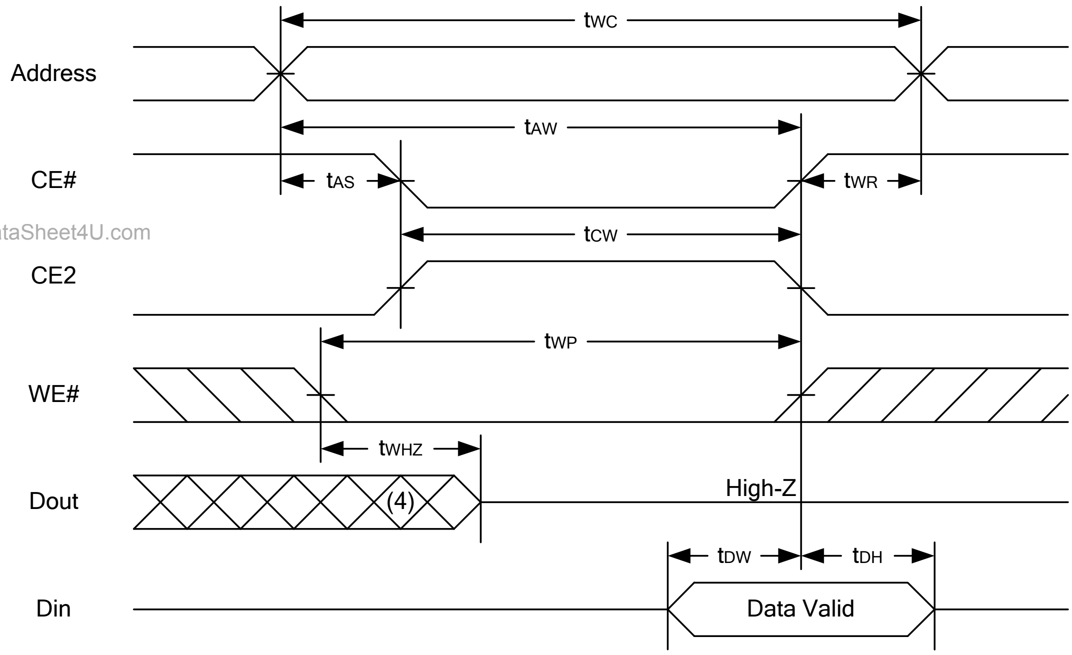


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low., CE2 = high.
3.Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)



Notes :
1.WE#, CE# must be high or CE2 must be low during all address transitions.
2.A write occurs during the overlap of a low CE#, high CE2, low WE#.
3.During a WE#controlled write cycle with OE# low, t_{WP} must be greater than t_{WHZ} + t_{DW} to allow the drivers to turn off and data to be placed on the bus.
4.During this period, I/O pins are in the output state, and input signals must not be applied.
5.If the CE#low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

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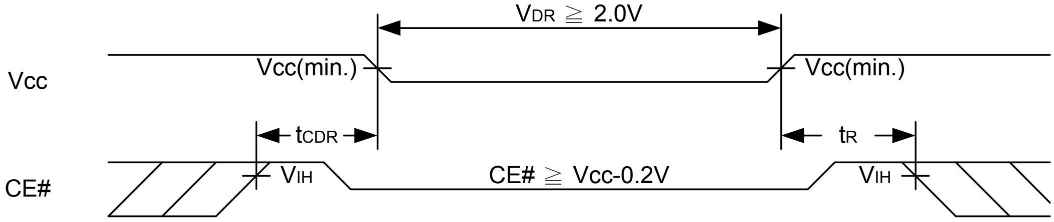
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V		2.0	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 2.0V CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V	Normal	-	0.01	3	mA
		V_{CC} = 2.0V CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V others at 0.2V or V_{CC}-0.2V	LL	-	0.5	30	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC*}	-	-	ns

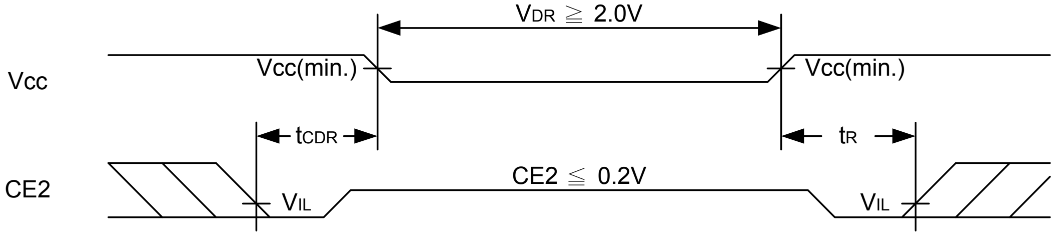
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)



Low Vcc Data Retention Waveform (2) (CE2 controlled)



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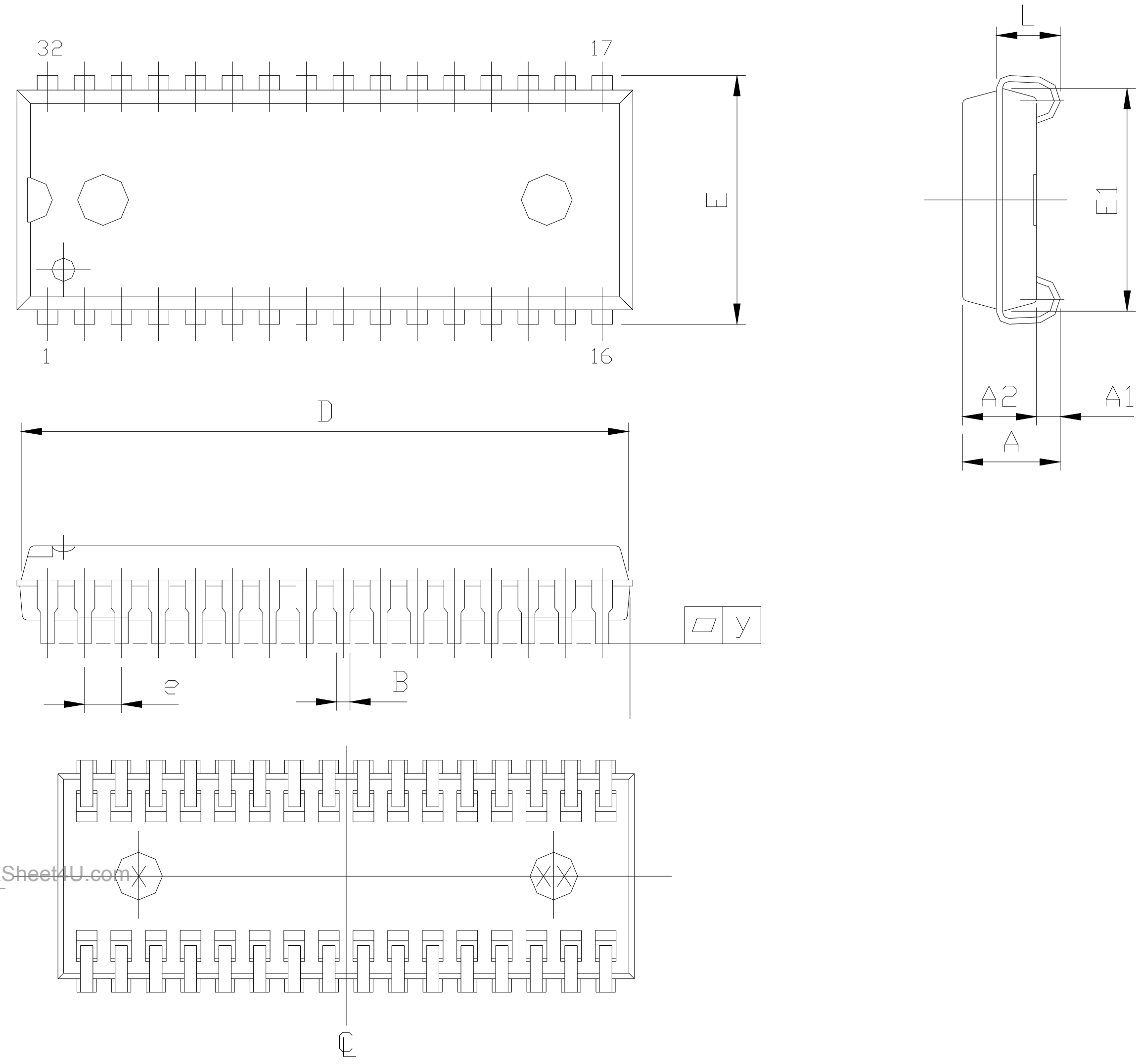
PACKAGE OUTLINE DIMENSION

32 pin 300mil SOJ Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.148 (MAX)	3.759 (MAX)
A1	0.026 (MIN)	0.660 (MIN)
A2	0.100 ±0.005	2.540 ±0.127
B	0.018 (TYP)	0.457 (TYP)
D	0.830 (MAX)	21.082 (MAX)
E	0.335 (TYP)	8.509 (TYP)
E1	0.300 ±0.005	7.620 ±0.127
e	0.050 (TYP)	1.270 (TYP)
L	0.086 ±0.010	2.184 ±0.254
y	0.003 (MAX)	0.076 (MAX)

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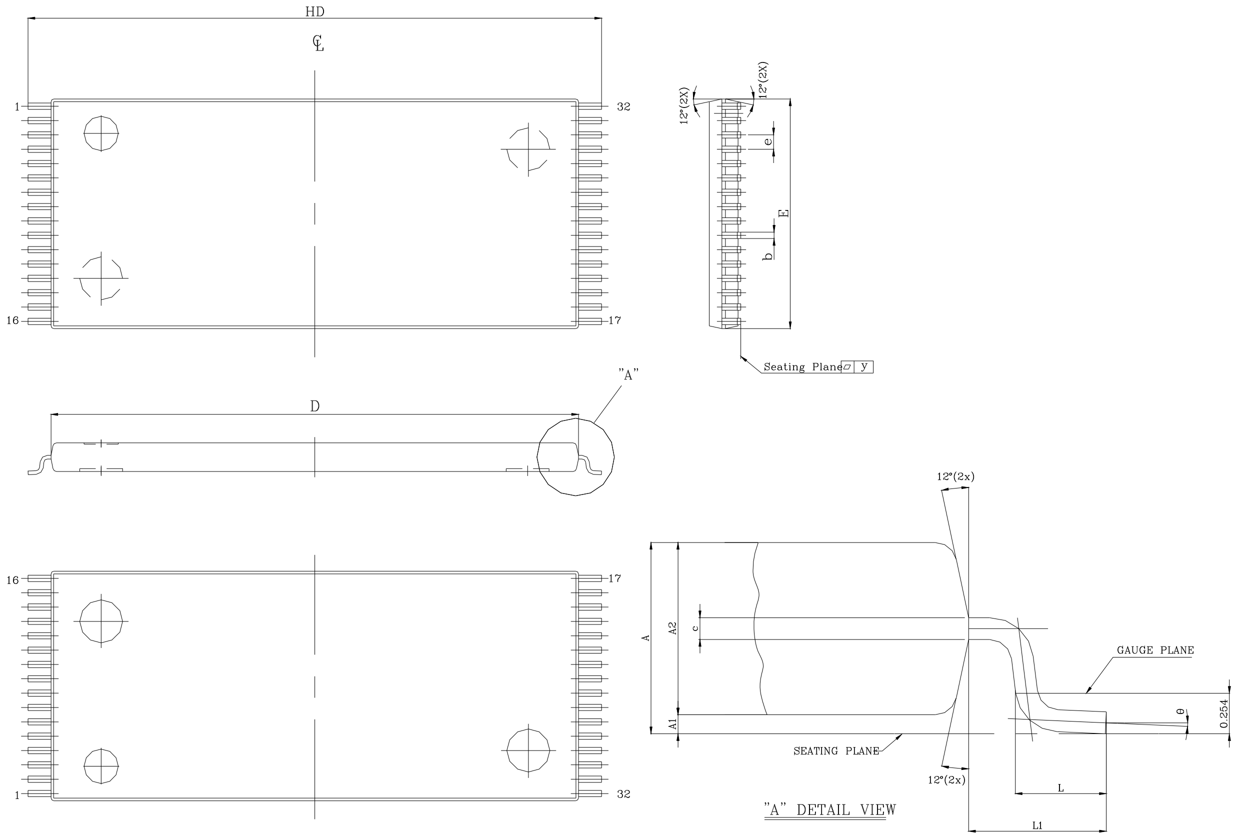
32 pin 8mm x 20mm TSOP-I Package Outline Dimension



SYM. \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
c	0.005 (TYP)	0.127 (TYP)
D	0.724 ±0.004	18.40 ±0.10
E	0.315 ±0.004	8.00 ±0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L	0.0197 ±0.004	0.50 ±0.10
L1	0.0315 ±0.004	0.08 ±0.10
y	0.003 (MAX)	0.076 (MAX)
Θ	$0^{o}\sim5^{o}$	$0^{o}\sim5^{o}$

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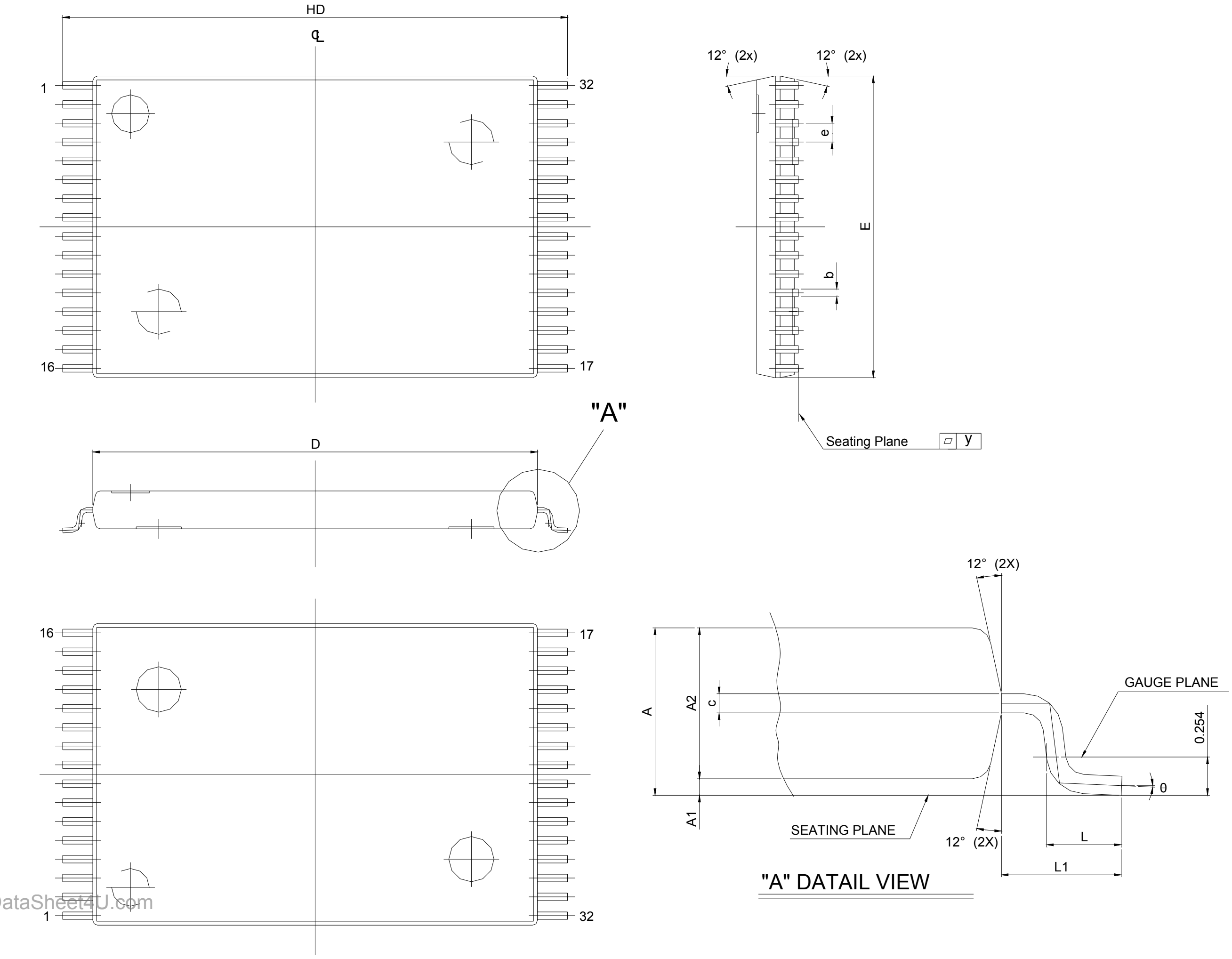
32 pin 8mm x 13.4mm STSOP Package Outline Dimension



SYM. \ UNIT	INCH(BASE)	MM(REF)
A	0.049 (MAX)	1.25 (MAX)
A1	0.005 ±0.002	0.130 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 ±0.01	0.20±0.025
c	0.005 (TYP)	0.127 (TYP)
D	0.465 ±0.004	11.80 ±0.10
E	0.315 ±0.004	8.00 ±0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.528±0.008	13.40 ±0.20.
L	0.0197 ±0.004	0.50 ±0.10
L1	0.0315 ±0.004	0.8 ±0.10
y	0.003 (MAX)	0.076 (MAX)
Θ	$0^\circ \sim 5^\circ$	$0^\circ \sim 5^\circ$

ORDERING INFORMATION

LY611024 U V - WW XX Y Z

Z : Packing Type
Blank : Tube or Tray
T : Tape Reel

Y : Temperature Range
Blank : (Commercial) 0°C ~ 70°C
E : (Extended) -20°C ~ +80°C
I : (Industrial) -40°C ~ +85°C

XX : Power Type
LL : Ultra Low Power

WW : Access Time(Speed)

V : Lead Information
L : Green Package

U : Package Type
J : 32-pin 300 mil SOJ
L : 32-pin 8 mm x 20 mm TSOP-I
R :32-pin 8 mm x 13.4 mm STSOP

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