



LY616416

Rev. 1.1

5V 64K X 16 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Aug.29.2007
Rev. 1.1	Revised Test Condition of Icc Revised <u>FEATURES & ORDERING INFORMATION</u> <u>Lead free and green package available</u> to <u>Green package available</u> Deleted T _{SOLDER} in <u>ABSOLUTE MAXIMUM RATINGS</u> Added packing type in <u>ORDERING INFORMATION</u>	Aug.28.2009



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FEATURES

- Fast access time : 15/20ns
- Low power consumption:
Operating current : 140/110mA(MAX.)
Standby current :
3mA(MAX. for 15/20ns)
100µA((MAX. for 15/20ns LL version)
- Single 5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP-II

GENERAL DESCRIPTION

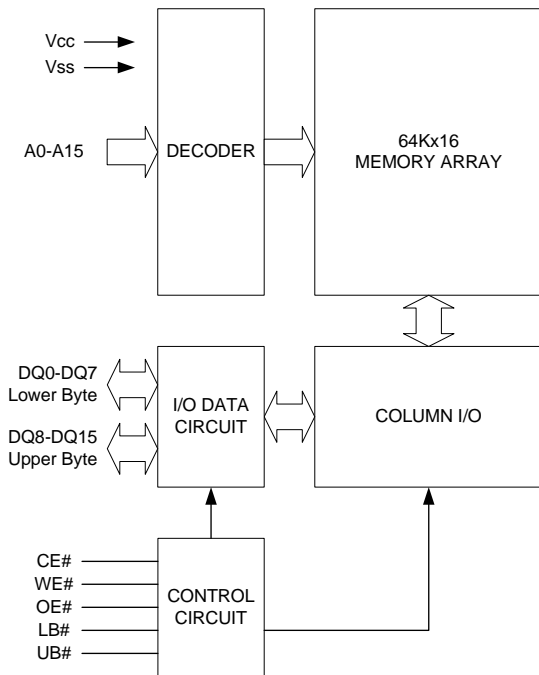
The LY616416 is a 1,048,576-bit low power CMOS static random access memory organized as 65,536 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY616416 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY616416 operates from a single power supply of 5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(IsB1)	Operating(Icc)
LY616416	0 ~ 70°C	4.5 ~ 5.5V	15/20ns	3mA(MAX.)	140/110mA(MAX.)
LY616416(E)	-20 ~ 80°C	4.5 ~ 5.5V	15/20ns	3mA(MAX.)	140/110mA(MAX.)
LY616416(I)	-40 ~ 85°C	4.5 ~ 5.5V	15/20ns	3mA(MAX.)	140/110mA(MAX.)
LY616416(LL)	0 ~ 70°C	4.5 ~ 5.5V	15/20ns	100µA(MAX.)	140/110mA(MAX.)
LY616416(LLE)	-20 ~ 80°C	4.5 ~ 5.5V	15/20ns	100µA(MAX.)	140/110mA(MAX.)
LY616416(LLI)	-40 ~ 85°C	4.5 ~ 5.5V	15/20ns	100µA(MAX.)	140/110mA(MAX.)

FUNCTIONAL BLOCK DIAGRAM**PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground

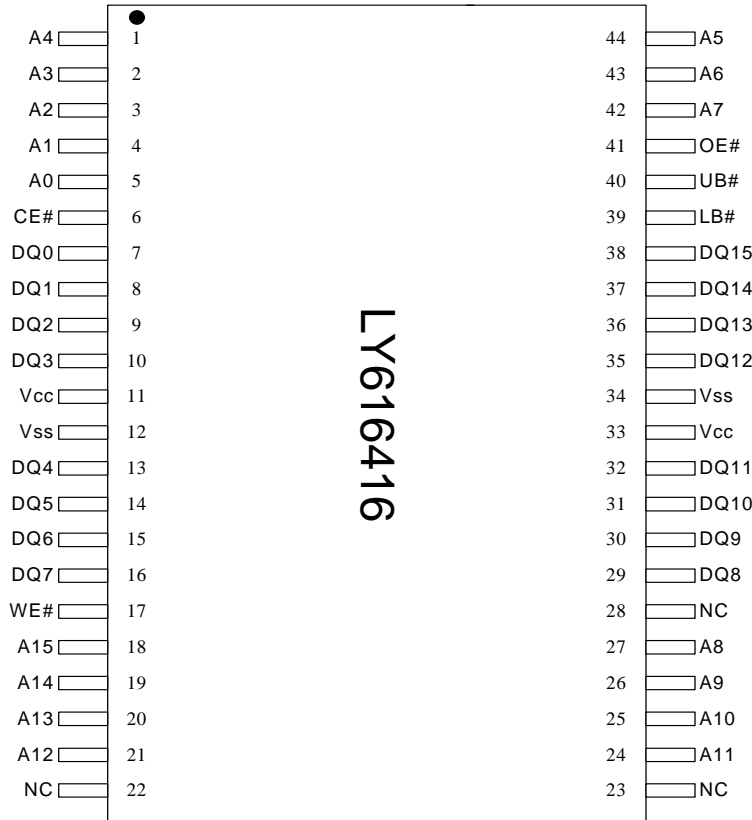


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PIN CONFIGURATION



TSOP II

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



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TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	High - Z	High - Z	I _{SB1}
Output Disable	L	H	H	X	X	High - Z	High - Z	I _{CC}
	L	X	X	H	H	High - Z	High - Z	
Read	L	L	H	L	H	D _{OUT}	High - Z	I _{CC}
	L	L	H	H	L	High - Z	D _{OUT}	
	L	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	X	L	L	H	D _{IN}	High - Z	I _{CC}
	L	X	L	H	L	High - Z	D _{IN}	
	L	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT	
Supply Voltage	V _{CC}		4.5	5.0	5.5	V	
Input High Voltage	V _{IH} ¹		0.6*V _{CC}	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} ²		-0.3	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA Others at V _{IL} or V _{IH}	15	-	100	140	mA
			20	-	80	110	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V Others at 0.2V or V _{CC} -0.2V	15/20	-	0.1	3 ^{*5}	mA
			15/20LL	-	20	100 ^{*6}	μA

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- 1mA for special request
- 50μA for special request

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	8	pF
Input/Output Capacitance	C _{I/O}	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.



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AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -8mA/16mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY616416-15		LY616416-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	15	-	20	-	ns
Address Access Time	t _{AA}	-	15	-	20	ns
Chip Enable Access Time	t _{ACE}	-	15	-	20	ns
Output Enable Access Time	t _{OE}	-	7	-	8	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	4	-	4	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	7	-	8	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	7	-	8	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	ns
LB#, UB# Access Time	t _{BA}	-	7	-	8	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	7	-	8	ns
LB#, UB# to Low-Z Output	t _{BLZ} *	4	-	4	-	ns

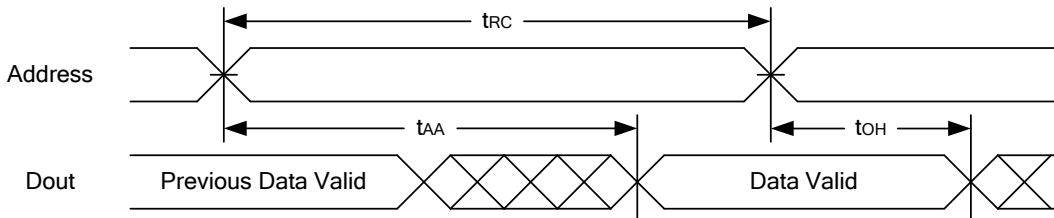
(2) WRITE CYCLE

PARAMETER	SYM.	LY616416-15		LY616416-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	15	-	20	-	ns
Address Valid to End of Write	t _{AW}	12	-	16	-	ns
Chip Enable to End of Write	t _{CW}	12	-	16	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	10	-	11	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	8	-	9	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	4	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	8	-	9	ns
LB#, UB# Valid to End of Write	t _{BW}	12	-	16	-	ns

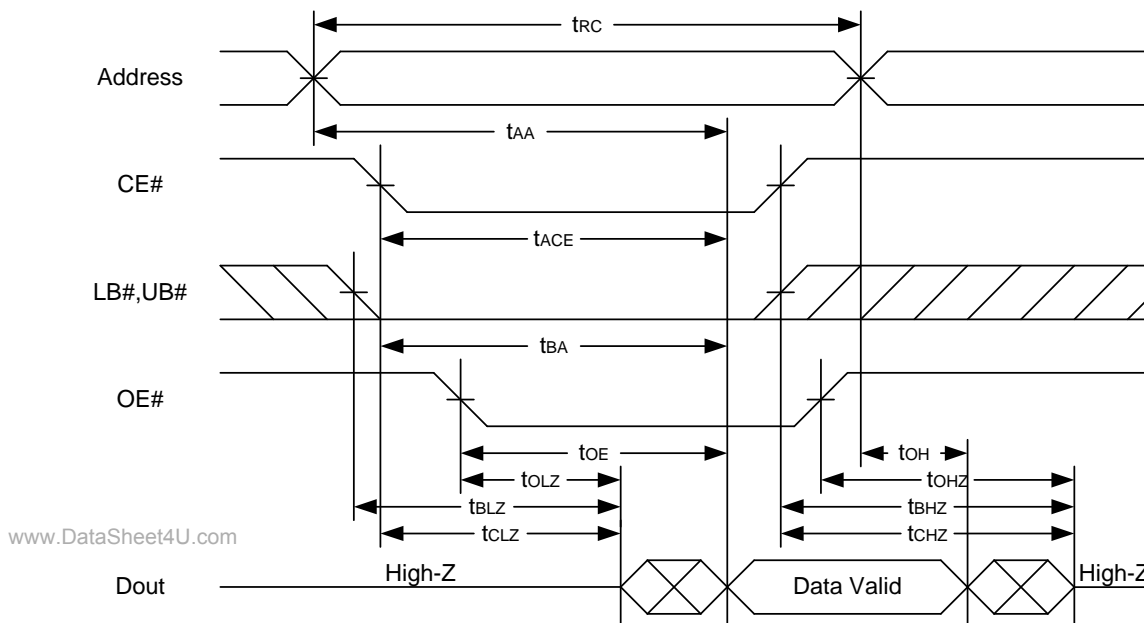
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. tCLZ, tBLZ, tOLZ, tCHZ, tBHZ and tOHZ are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tBHZ is less than tBLZ, tOHZ is less than tOLZ.

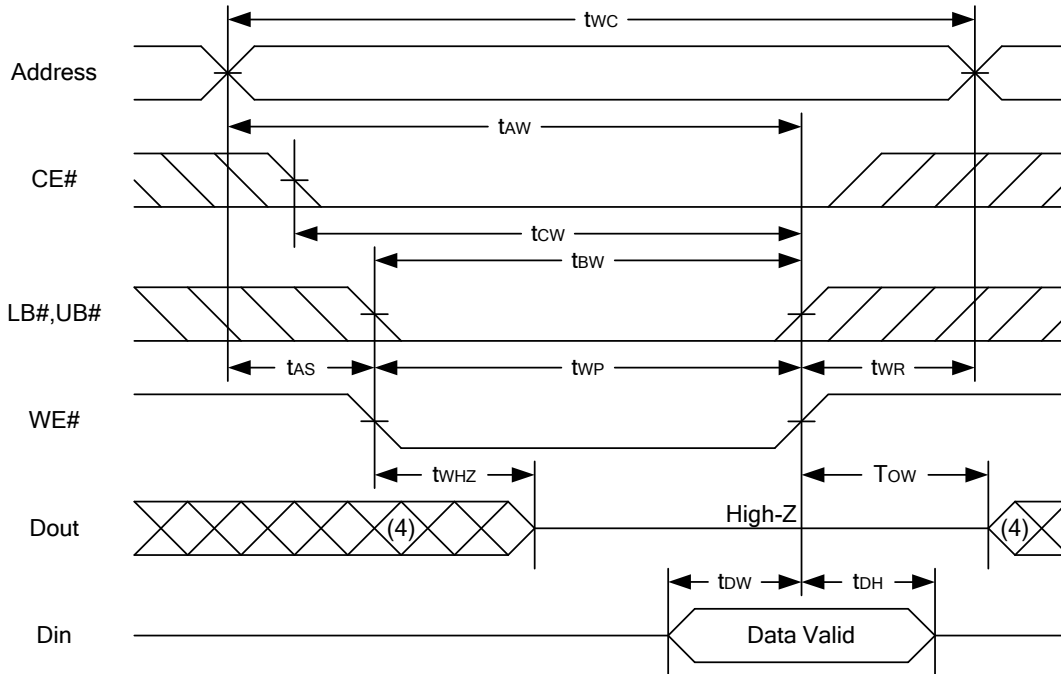


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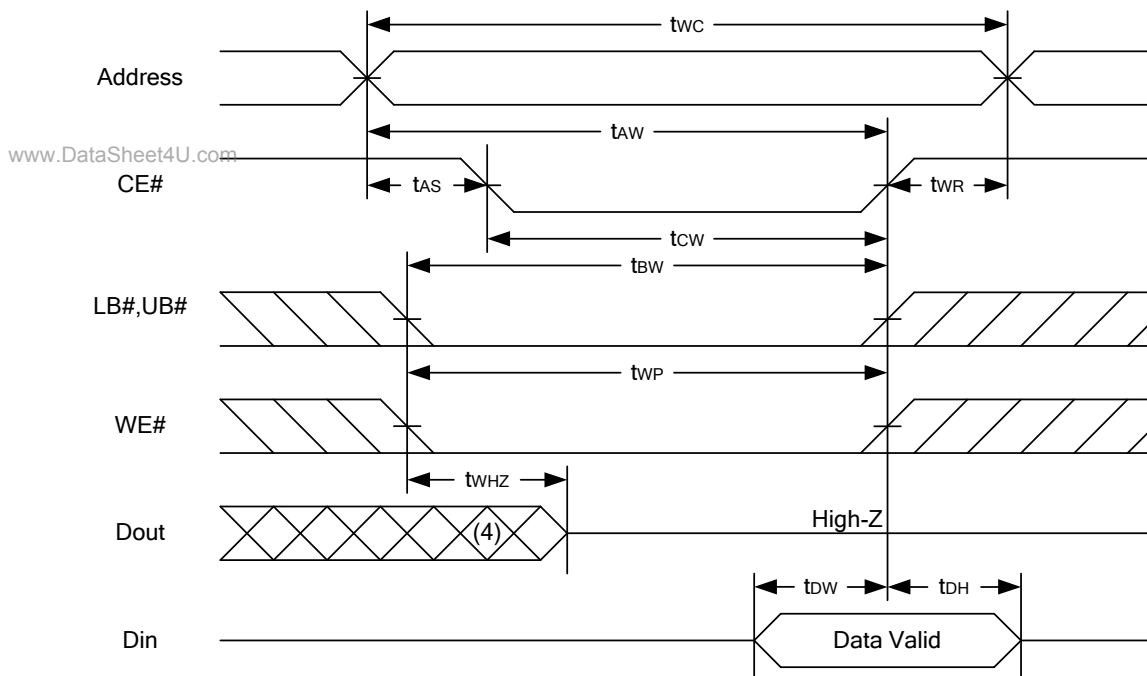
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WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

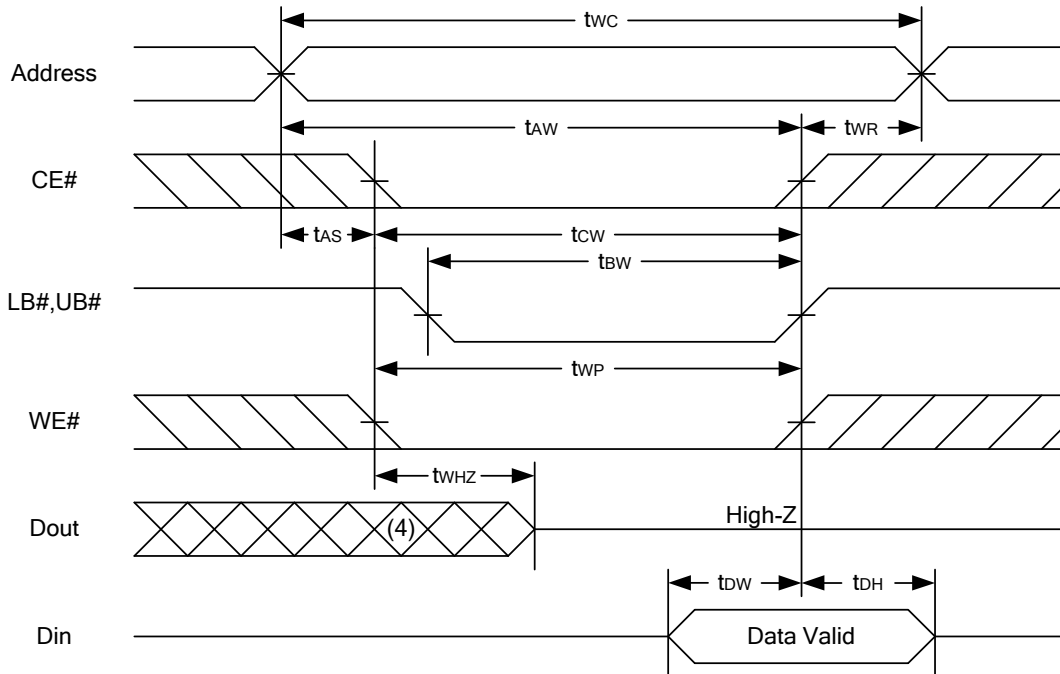


WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)





WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)



Notes :

1. WE#, CE#, LB#, UB# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{ow} and t_{whz} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

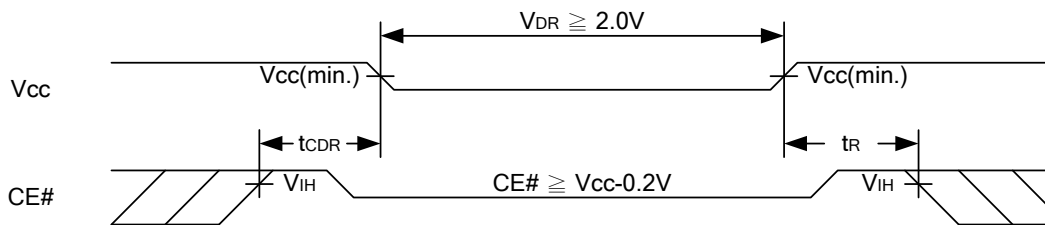


DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V	2.0	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V, CE# ≥ V _{CC} - 0.2V other pins at 0.2V or V _{CC} -0.2V	-	0.05	2	mA
		15/20	-	10	50	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC*}	-	-	ns

t_{RC*} = Read Cycle Time

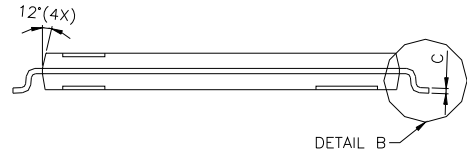
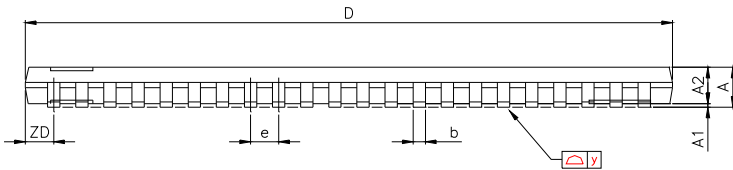
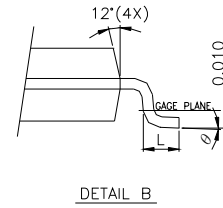
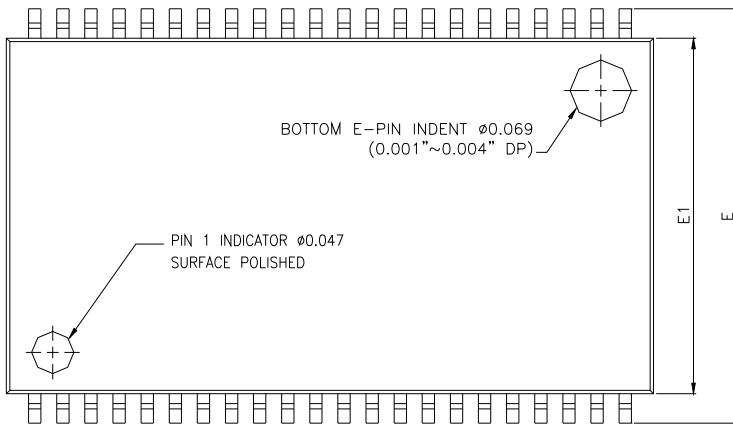
DATA RETENTION WAVEFORM





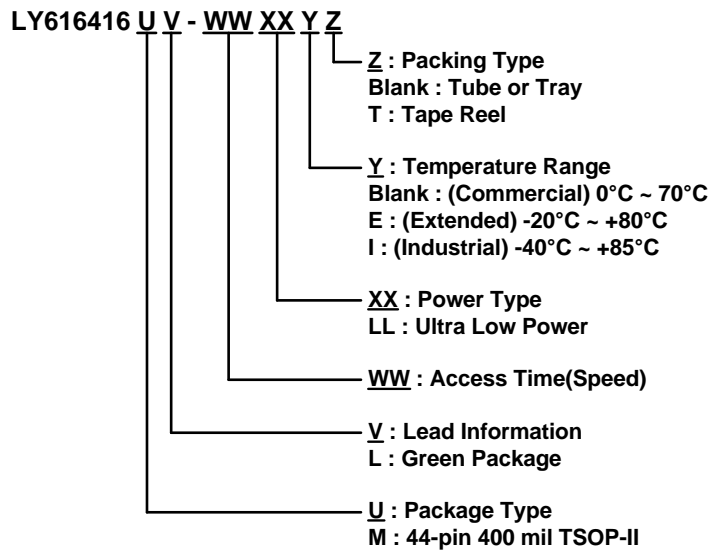
PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-II Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

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ORDERING INFORMATION



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