REVISION HISTORY

Revision	**Description**	**Issue Date**
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Revised **STSOP Package Outline Dimension**	Mar.26.2008
Rev. 1.2	Deleted L Spec. Revised V_{TERM} to V_{T1} and V_{T2} Revised Test Condition of I_{SB1}/I_{DR} Revised **FEATURES** & **ORDERING INFORMATION** **Lead free and green package available** to **Green package available** Added packing type in **ORDERING INFORMATION** Deleted T_{SOLDER} in **ABSOLUTE MAXIMUN RATINGS**	Apr.13.2009

Lyontek Inc.

LY62L256

Rev. 1.2

32K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Fast access time : 35/55/70ns
- Low power consumption:
  Operating current : 20/15/10mA (TYP.)
  Standby current : 0.5µA (TYP.) LL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 28-pin 600 mil PDIP
  28-pin 330 mil SOP
  28-pin 8mm x 13.4mm STSOP

GENERAL DESCRIPTION

The LY62L256 is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

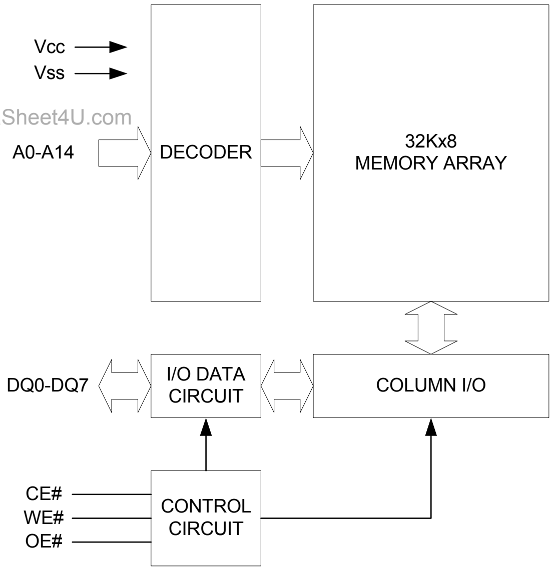
The LY62L256 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L256 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(I_{CC},TYP.)
LY62L256	0 ~ 70℃	2.7 ~ 3.6V	35/55/70ns	0.5µA(LL)	20/15/10mA
LY62L256(E)	-20 ~ 80℃	2.7 ~ 3.6V	35/55/70ns	0.5µA(LL)	20/15/10mA
LY62L256(I)	-40 ~ 85℃	2.7 ~ 3.6V	35/55/70ns	0.5µA(LL)	20/15/10mA

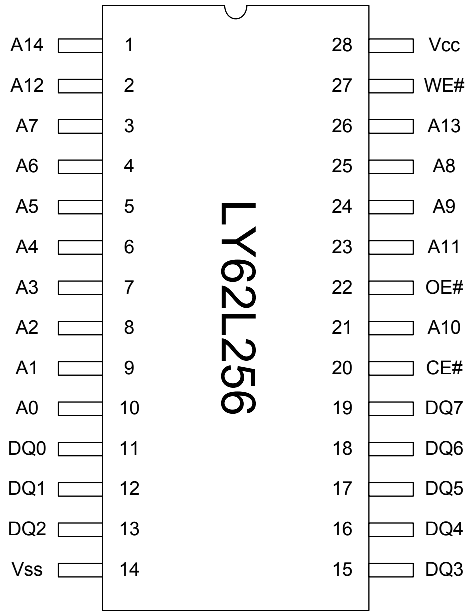
FUNCTIONAL BLOCK DIAGRAM



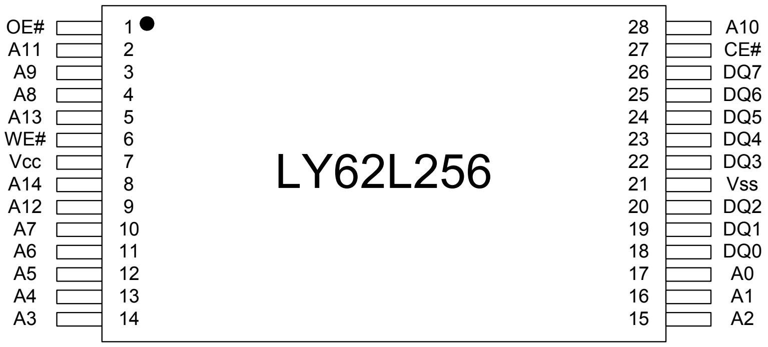
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION



PDIP/SOP



STSOP

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade)	℃
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I_{SB},I_{SB1}
Output Disable	L	H	H	High-Z	I_{CC},I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC},I_{CC1}
Write	L	X	L	D_{IN}	I_{CC},I_{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. [*5]	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.3	3.6	V
Input High Voltage	V_{IH} [*1]			2.0	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL} [*2]			- 0.5	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.4	3.0	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = V_{IL} , $I_{I/O}$ = 0mA Other pins at V_{IL} or V_{IH}	-35	-	20	40	mA
			-55	-	15	30	mA
			-70	-	10	20	mA
	I_{CC1}	Cycle time = 1µs CE#≦0.2V and $I_{I/O}$ = 0mA other pins at 0.2V or V_{CC}-0.2V		-	3	6	mA
Standby Power Supply Current	I_{SB}	CE# = V_{IH}, others at V_{IL} or V_{IH}		-	1	3	mA
	I_{SB1}	CE# ≧V_{CC} - 0.2V Others at 0.2V orV_{CC} - 0.2V	-LL	-	0.5	20 [*4]	µA

Notes:

1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. 10µA for special request
5. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃

CAPACITANCE (TA = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62L256-35		LY62L256-55		LY62L256-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	55	-	70	ns
Chip Enable Access Time	t_{ACE}	-	35	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	15	-	20	-	25	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns

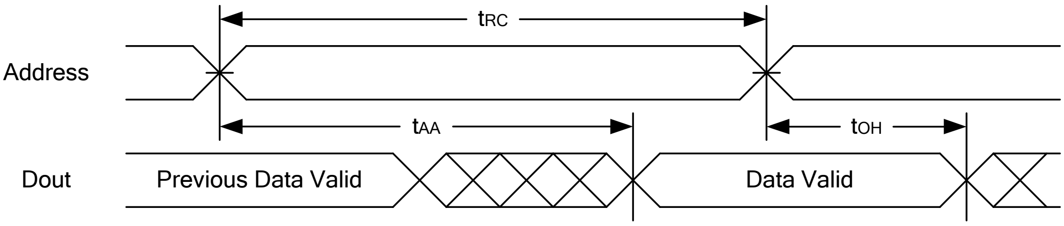
(2) WRITE CYCLE

PARAMETER	SYM.	LY62L256-35		LY62L256-55		LY62L256-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	50	-	60	-	ns
Chip Enable to End of Write	t_{CW}	30	-	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	45	-	55	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	20	-	25	ns

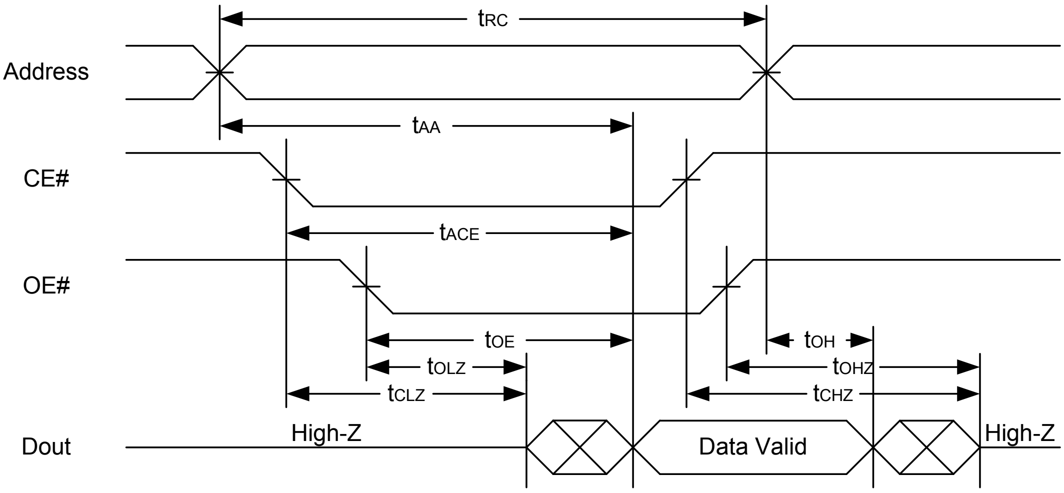
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

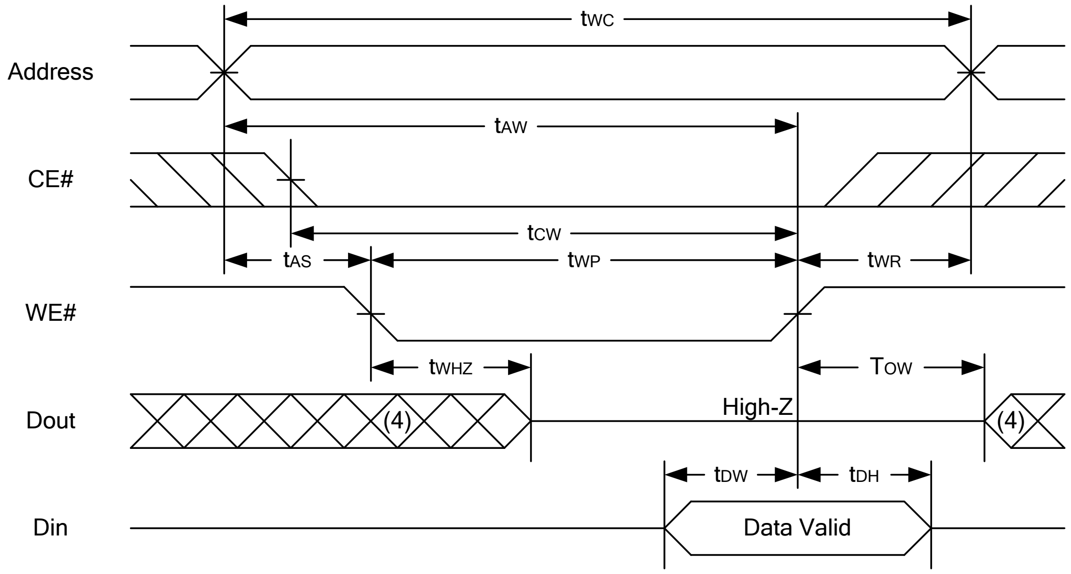


READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

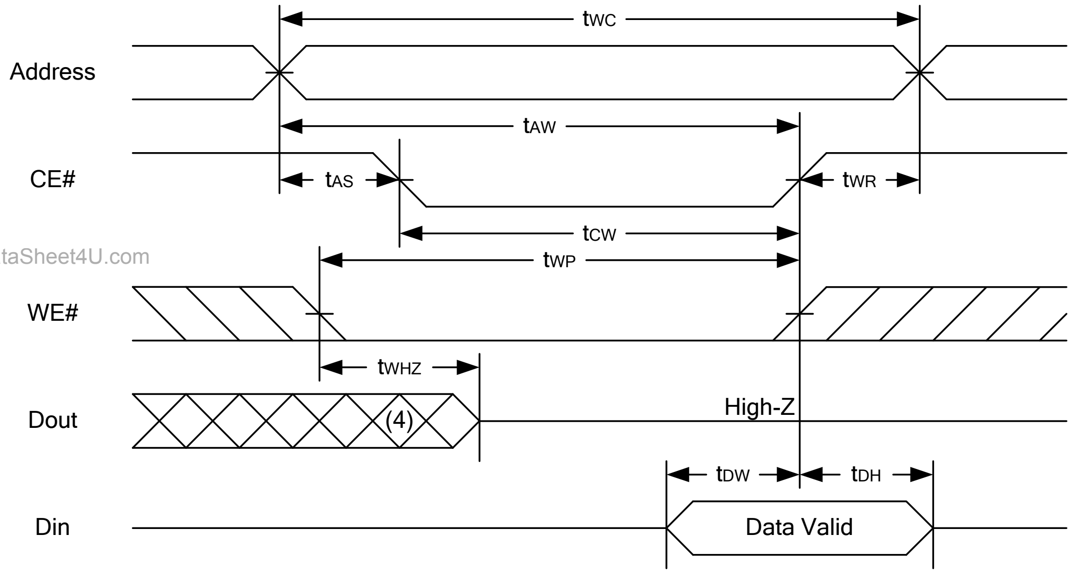


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low.
3.Address must be valid prior to or coincident with CE# = low,; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



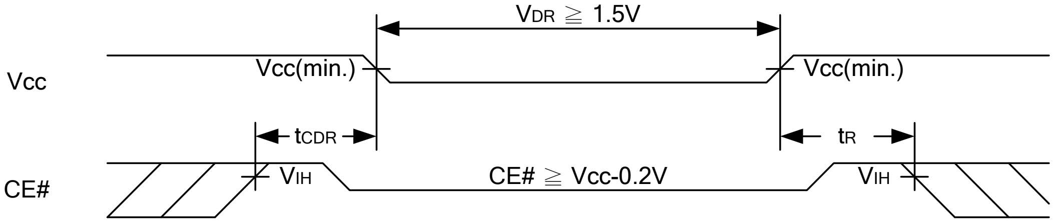
Notes :
1.WE#, CE# must be high during all address transitions.
2.A write occurs during the overlap of a low CE#, low WE#.
3.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than t_{WHZ} + t_{DW} to allow the drivers to turn off and data to be placed on the bus.
4.During this period, I/O pins are in the output state, and input signals must not be applied.
5.If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# ≧ V_{CC} - 0.2V Others at 0.2V or V_{CC}-0.2V	-LL	-	0.5	10	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC*}	-	-	ns

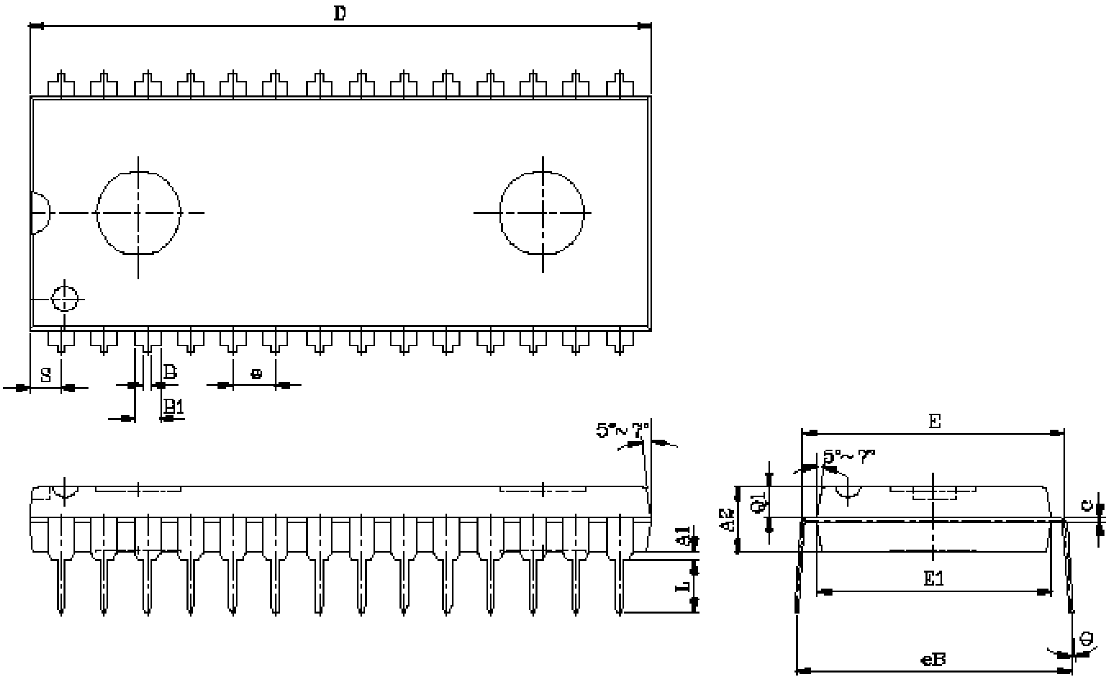
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM



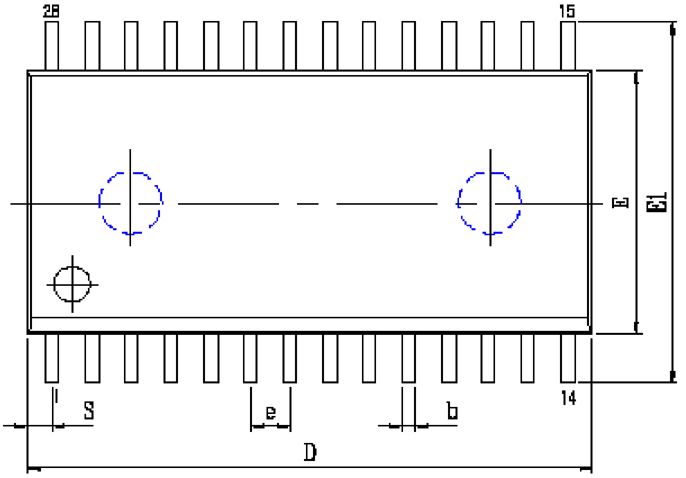
PACKAGE OUTLINE DIMENSION

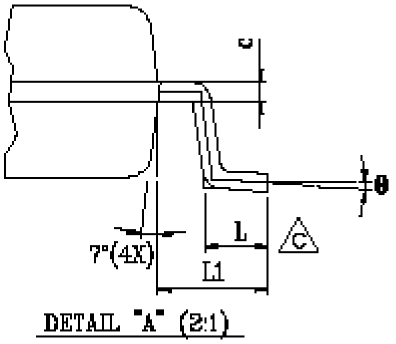
28 pin 600 mil PDIP Package Outline Dimension

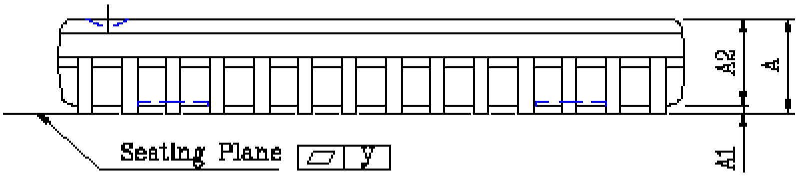


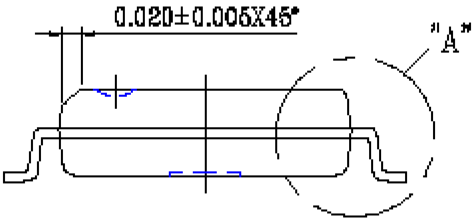
UNIT SYM.	INCH.(BASE)	MM(REF)
A1	0.010 (MIN)	0.254 (MIN)
A2	0.150±0.005	3.810±0.127
B	0.020 (MAX)	0.508(MAX)
B1	0.055 (MAX)	1.397(MAX)
c	0.012 (MAX)	0.304 (MAX)
D	1.430 (MAX)	36.322 (MAX)
E	0.6 (TYP)	15.24 (TYP)
E1	0.52 (MAX)	13.208 (MAX)
e	0.100 (TYP)	2.540(TYP)
eB	0.625 (MAX)	15.87 (MAX)
L	0.180(MAX)	4.572(MAX)
S	0.06 (MAX)	1.524 (MAX)
Q1	0.08(MAX)	2.032(MAX)
Θ	15°(MAX)	15°(MAX)

28 pin 330 mil SOP Package Outline Dimension



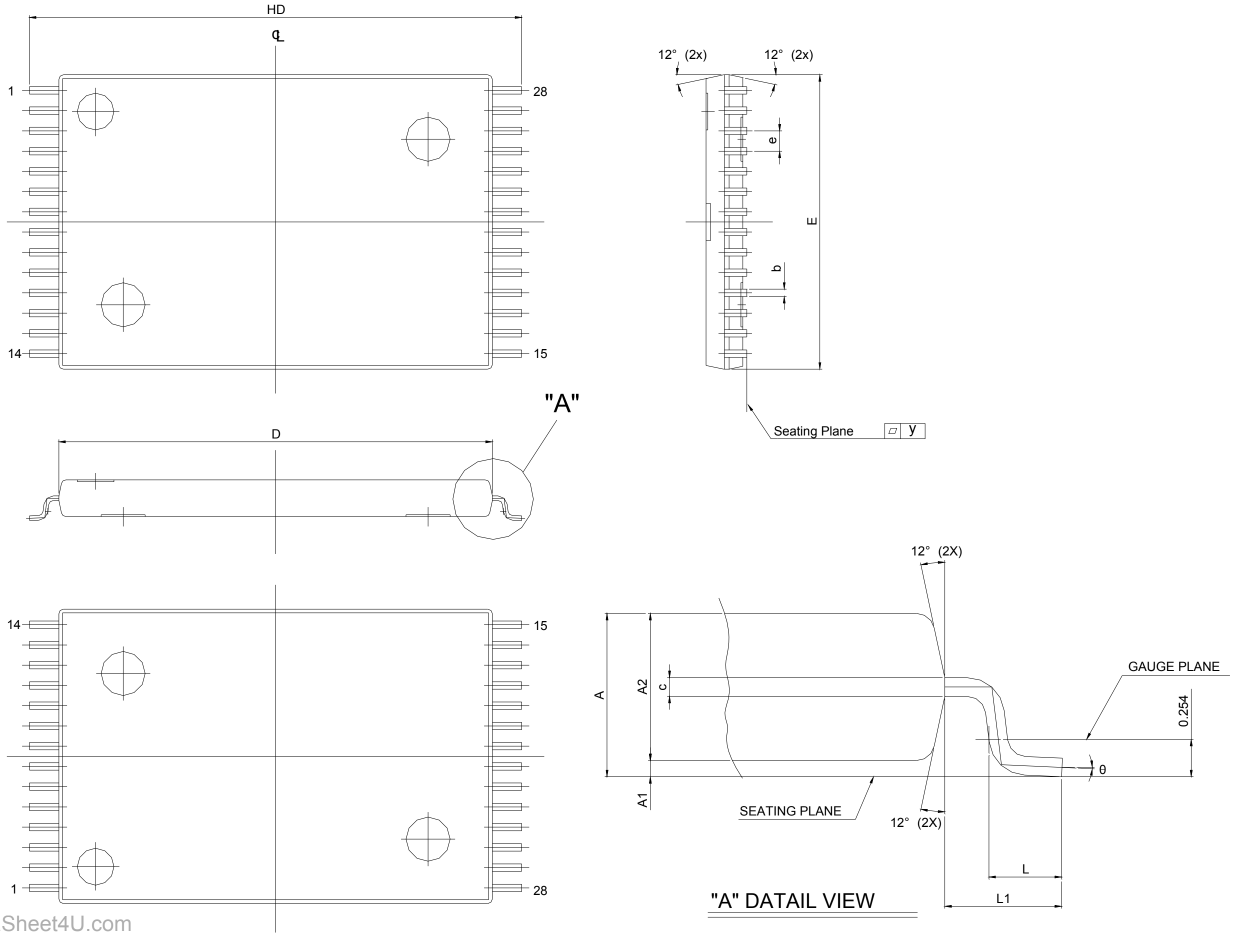






UNIT SYM.	INCH(BASE)	MM(REF)
A	0.120 (MAX)	3.048 (MAX)
A1	0.002(MIN)	0.05(MIN)
A2	0.098±0.005	2.489±0.127
b	0.016 (TYP)	0.406(TYP)
c	0.010 (TYP)	0.254(TYP)
D	0.728 (MAX)	18.491 (MAX)
E	0.340 (MAX)	8.636 (MAX)
E1	0.465±0.012	11.811±0.305
e	0.050 (TYP)	1.270(TYP)
L	0.05 (MAX)	1.270 (MAX)
L1	0.067±0.008	1.702 ±0.203
S	0.047 (MAX)	1.194 (MAX)
y	0.003(MAX)	0.076(MAX)
Θ	0°～10°	0°～10°

28 pin 8x13.4mm STSOP Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	0.15	0.20	0.004	0.006	0.008
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
θ	0°	3°	5°	0°	3°	5°

ORDERING INFORMATION

LY62L256 U V - WW XX Y Z

Z : Packing Type
Blank : Tube or Tray
T : Tape Reel

Y : Temperature Range
Blank : (Commercial) 0°C ~ 70°C
E : (Extended) -20°C ~ +80°C
I : (Industrial) -40°C ~ +85°C

XX : Power Type
LL : Ultra Low Power

WW : Access Time(Speed)

V : Lead Information
L : Green Package

U : Package Type
P : 28-pin 600 mil P-DIP
S : 28-pin 330 mil SOP
R : 28-pin 8 mm x 13.4 mm STSOP

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