Lyontek Inc.

LY8210

Rev. 1.7

2.5 W/CH Stereo Class D Audio power Amplifier (WCSP/ TSSOP)

FEATURES

- 2.5 W/CH Into 4Ω from 5V power supply at THD = 10% (Typ.).
- 2.5V~5.5V Power supply.
- Low shutdown Current.
- Low Quiescent Current.
- Minimum external components.
- No output filter required for inductive loads.
- Output Pin Short-Circuit Protection (Short to Output Pin, Short to GND, Short to VCC)
- Low noise during turn-on and turn-off transitions.
- Lead free and green package available. (RoHS Compliant)
- Wafer Chip Scale (WCSP) and TSSOP 20 pin packaging available.

GENERAL DESCRIPTION

The LY8210 is a high efficiency, 2.5 W stereo class D audio power amplifier. It is a low noise, filterless PWM architecture eliminates the output filter, reducing external component count, system cost, and simplify design.

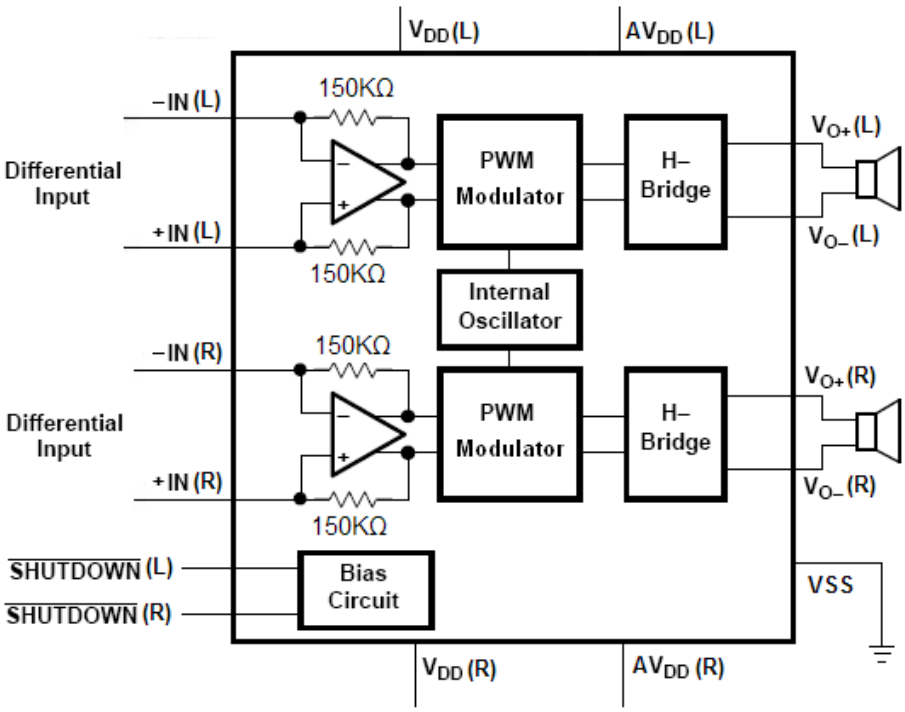
The LY8210 is designed to meet of Multimedia application includes mobile phones and other portable electronic devices. The LY8210 is a single 5V supply, it is capable of driving 4Ω speaker load at a continuous average output of 2.5 W/CH with 10% THD+N.

In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the LY8210. Output pin short circuit (short to output pin, short to ground and short to VDD) protection prevent the device from damage during fault conditions.

APPLICATION

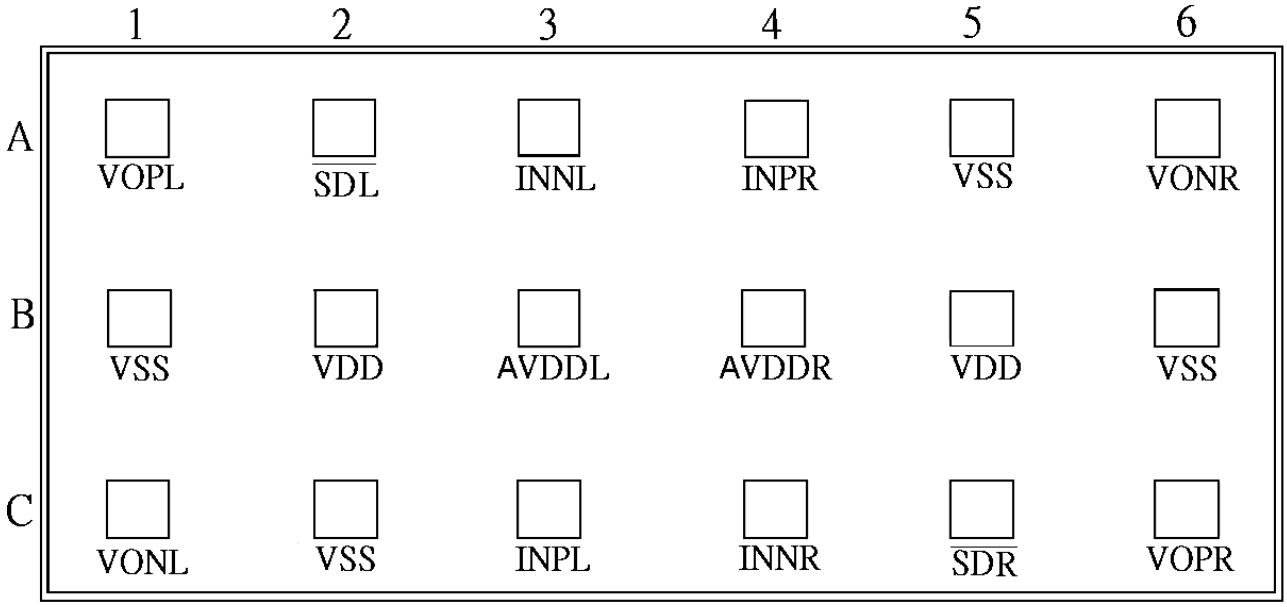
- Portable electronic devices
- Mobile Phones, PDAs
- DVD/CD Players, TFT LCD TVs/Monitors
- USB Audio, 2.1 / 5.1 CH Audio System

BLOCK DIAGRAM

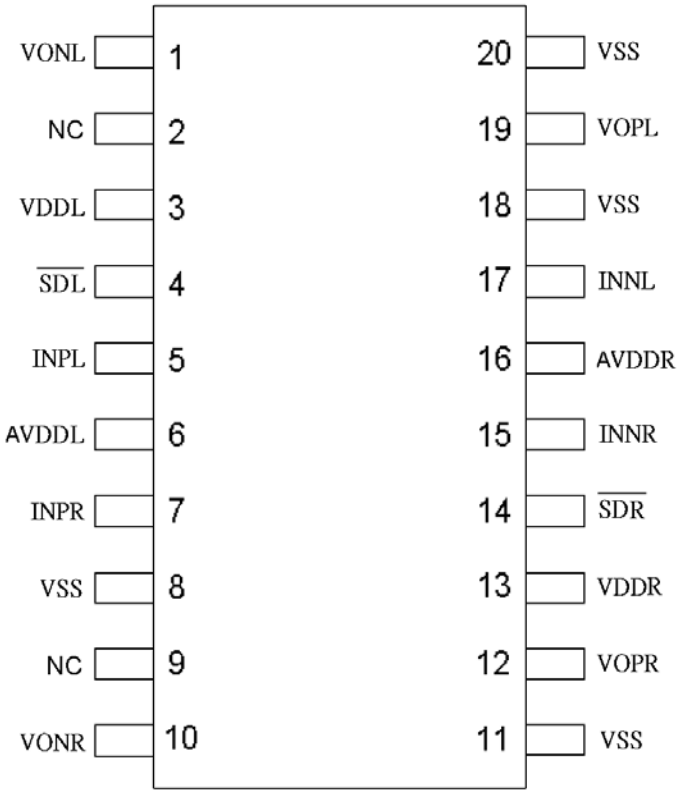


PIN CONFIGURATION

LY8210 WCSP 18 Ball Pin Configuration (Top View)



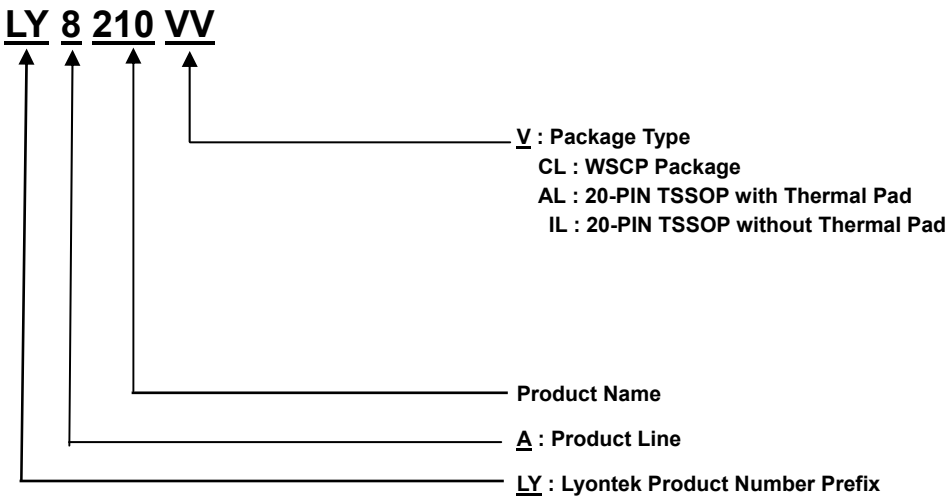
LY8210 TSSOP20 Pin Configuration (Top View)



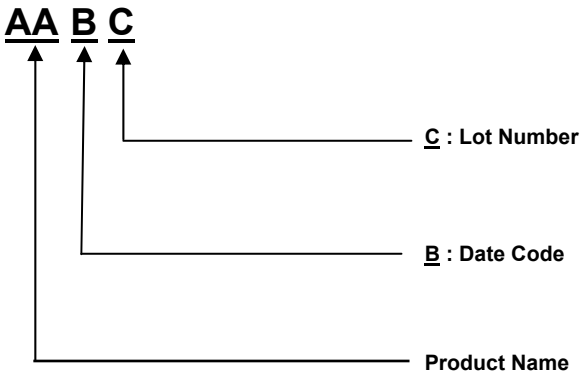
PIN DESCRIPTION

SYMBOL	Pin No.		DESCRIPTION
	WCSP	TSSOP	
SDL	A2	4	Shutdown pin of left channel. (when low level is active the pin).
INPL(+)	C3	5	Positive(+) input of left channel.
INNL(-)	A3	17	Negative(-) input of left channel.
VOPL(+)	A1	19	Positive(+) BTL output of left channel.
VONL(-)	C1	1	Negative(-) BTL output of left channel.
AV_{DD}	B3/B4	6/16	Analog Power supply of left and right channel.
V_{DD}	B2/B5	3/13	Power supply of left and right channel.
Vss	C2/A5 B1/B6	8/11/18/20	Ground
SDR	C5	14	Shutdown pin of right channel. (when low level is active the pin).
INPR(+)	A4	7	Positive(+) input of right channel.
INNR(-)	C4	15	Negative(-) input of right channel.
VOPR(+)	C6	12	Positive(+) BTL output of right channel.
VONR(-)	A6	10	Negative(-) BTL output of right channel.
NC	--	2/9	No Connection.

ORDERING INFORMATION



PACKAGE MARKING FORMAT (For WCSP Package only)



TYPICAL APPLICATION CIRCUIT

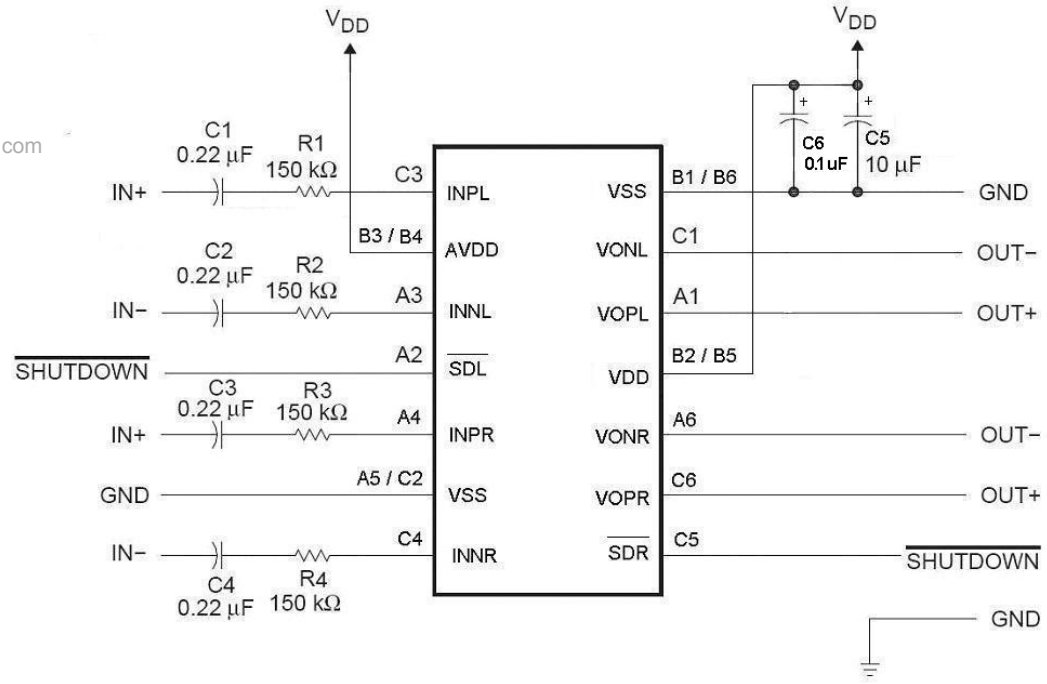


Figure 1. Typical Application Schematic With Differential Input and AVDD Connect to VDD Configuration (WCSP package)

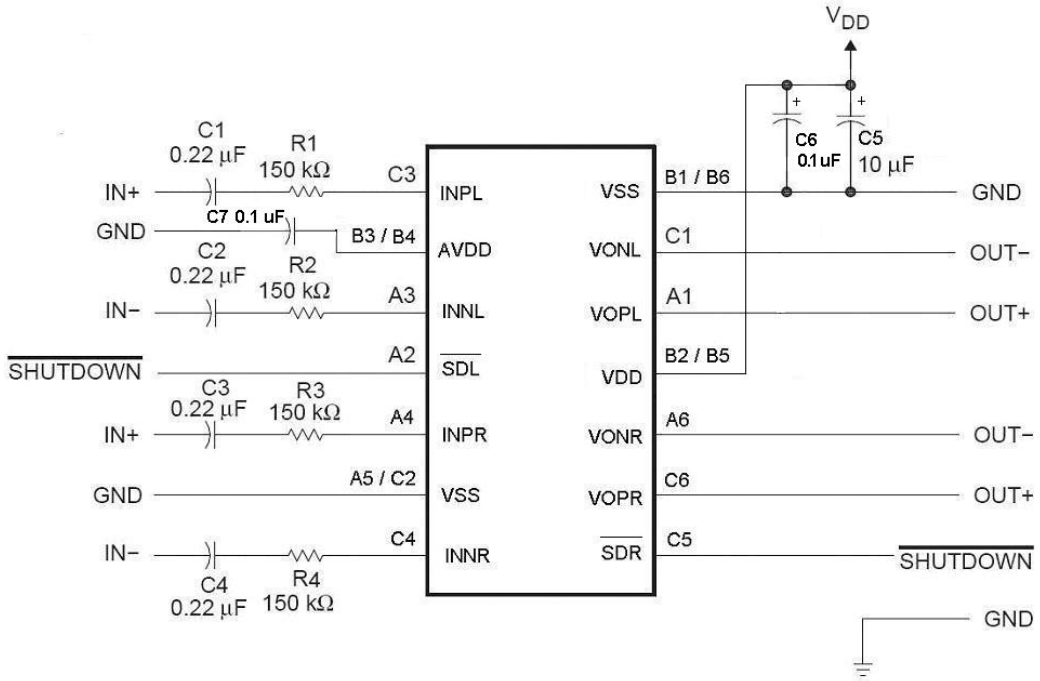


Figure 2. Typical Application Schematic With Differential Input and AVDD Increase Capacitors Configuration(WCSP package).

Note: In case of AVDD and VDD, the use of AVDD Increase Capacitors will optimize the THD+N.

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	6.0	V
Operating Temperature	T_A	-40 to 85 (I grade)	℃
Input Voltage	V_I	-0.3V to V_{DD} +0.3V	V
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	Internally Limited	W
ESD Susceptibility	V_{ESD}	2000	V
Junction Temperature	T_{JMAX}	150	℃
Soldering Temperature (under 10 sec)	T_{SOLDER}	260	℃

ELECTRICAL CHARACTERISTICS (T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output offset voltage (measured differentially)	$\|V_{OS}\|$	V_I = 0 V, Av = 2 V/V, V_{DD} = 2.5 V to 5.5 V	-	-	50	mV
High-level input current	$\|I_{IH}\|$	V_{DD} = 5.5 V, V_I = 5.8 V	-	-	200	uA
Low-level input current	$\|I_{IL}\|$	V_{DD} = 5.5 V, V_I = 0.3 V	-	-	10	uA
Quiescent Current	I_Q	V_{DD} = 5.5V, No Load	-	6.8	9.0	mA
		V_{DD} = 3.6V, No Load	-	5.6	-	
		V_{DD} = 2.5V, No Load	-	4.4	6.4	
Shutdown Current	I_{SD}	$V_{SHUTDOWN}$ = 0.8V, V_{DD} = 2.5V to 5.5V	-	0.6	4	μA

▪ OPERATING CHARACTERISTICS (1)(T_A = 25℃, Gain = 2 V/V)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Out Power / Channel	P_O	THD+N= 10%, f = 1 kHz, R_L= 8Ω	V_{DD}=5.0V	-	1.5	-	W
			V_{DD}=3.6V	-	0.7	-	
			V_{DD}=2.5V	-	0.35	-	
		THD+N= 1%, f = 1 kHz, R_L= 8Ω	V_{DD}=5.0V	-	1.2	-	
			V_{DD}=3.6V	-	0.6	-	
			V_{DD}=2.5V	-	0.3	-	
		THD+N= 10%, f = 1 kHz, R_L= 4Ω	V_{DD}=5.0V	-	2.5	-	
			V_{DD}=3.6V	-	1.2	-	
			V_{DD}=2.5V	-	0.5	-	
		THD+N= 1%, f = 1 kHz, R_L= 4Ω	V_{DD}=5.0V	-	2.0	-	
			V_{DD}=3.6V	-	0.9	-	
			V_{DD}=2.5V	-	0.4	-	
Total harmonic distortion + noise	THD+N	P_O = 1.0 W, f = 1 kHz, R_L = 8Ω	V_{DD}=5.0V	-	0.03	-	%
		P_O = 2.0 W, f = 1 kHz, R_L = 4Ω		-	0.06	-	
		P_O = 0.5 W, f = 1 kHz, R_L = 8Ω	V_{DD}=3.6V	-	0.03	-	
		P_O = 0.8 W, f = 1 kHz, R_L = 4Ω		-	0.04	-	
		P_O = 0.2 W, f = 1 kHz, R_L = 8Ω	V_{DD}=2.5V	-	0.04	-	
		P_O = 0.2 W, f = 1 kHz, R_L = 4Ω		-	0.04	-	
Power supply rejection ratio	PSRR	V_{DD} = 2.5 V to 5.5 V		-	-75	-	dB
Common mode rejection ratio	CMRR	V_{IC} = 1 Vpp , f = 217 Hz	V_{DD}=3.6V	-	-63	-	dB
Signal-to-noise ratio	SNR	PO= 1.0 W, RL = 8Ω	V_{DD}=5.0V	-	91	-	dB
Output voltage noise	Vn	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, Inputs ac-grounded with Ci = 2 μF	No weighting	-	50	-	uV_{RMS}
			A weighting	-	36	-	
Closed-loop Gain	Gv	V_{DD} = 2.5V to 5.5V		-	150kΩ/Ri	-	V/V
Start-up time from shutdown	Z_I	V_{DD} = 2.5V to 5.5V		-	1	-	ms

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3
Total Harmonic Distortion + Noise vs Output Power (R_L = 4Ω, Stereo)

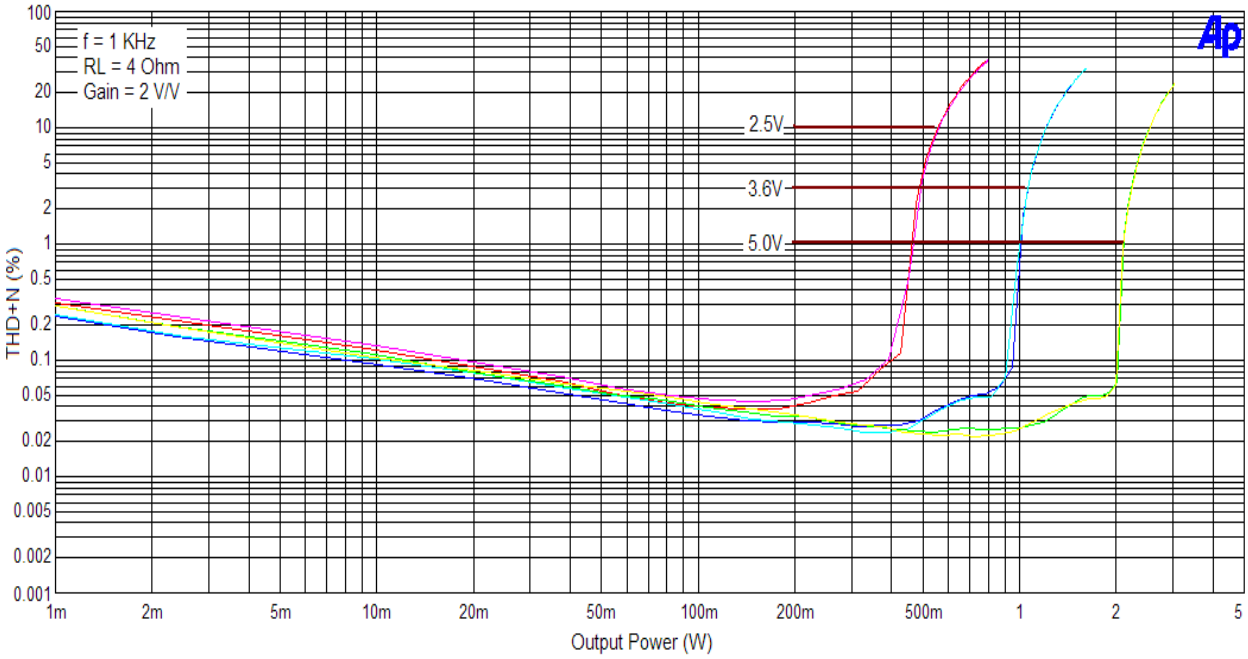


Figure 4
Total Harmonic Distortion + Noise vs Output Power (R_L = 8Ω, Stereo)

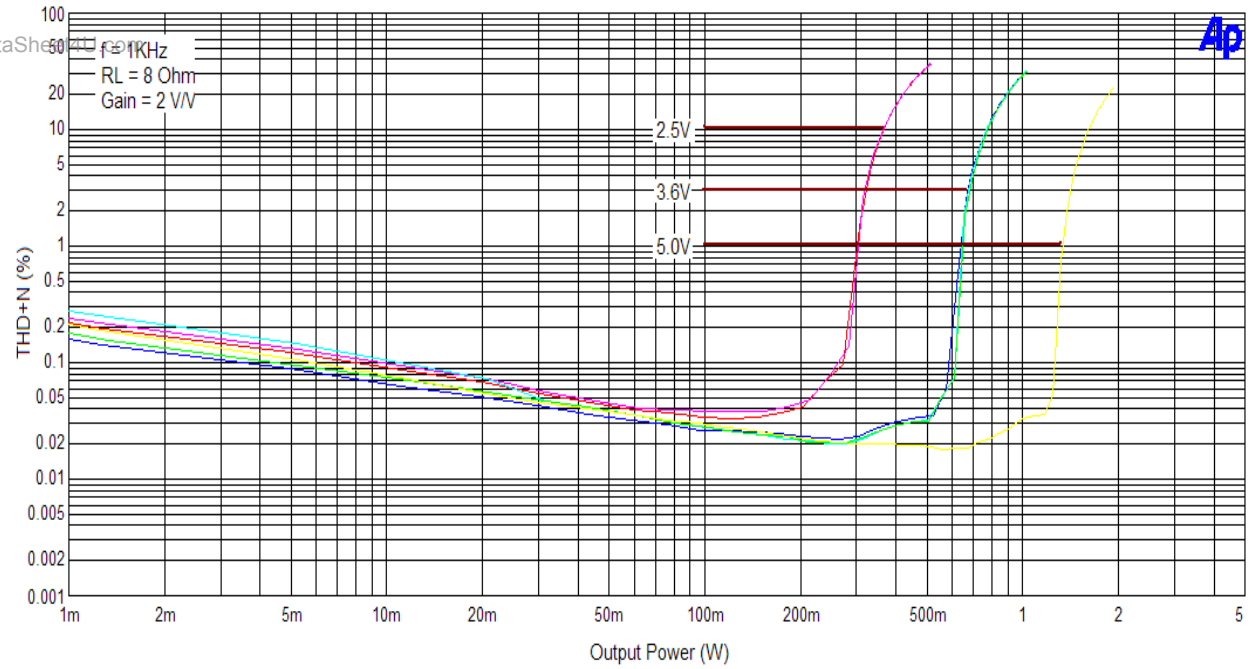


Figure 5
Total Harmonic Distortion + Noise vs Frequency (VDD=5.0V, 4Ω)

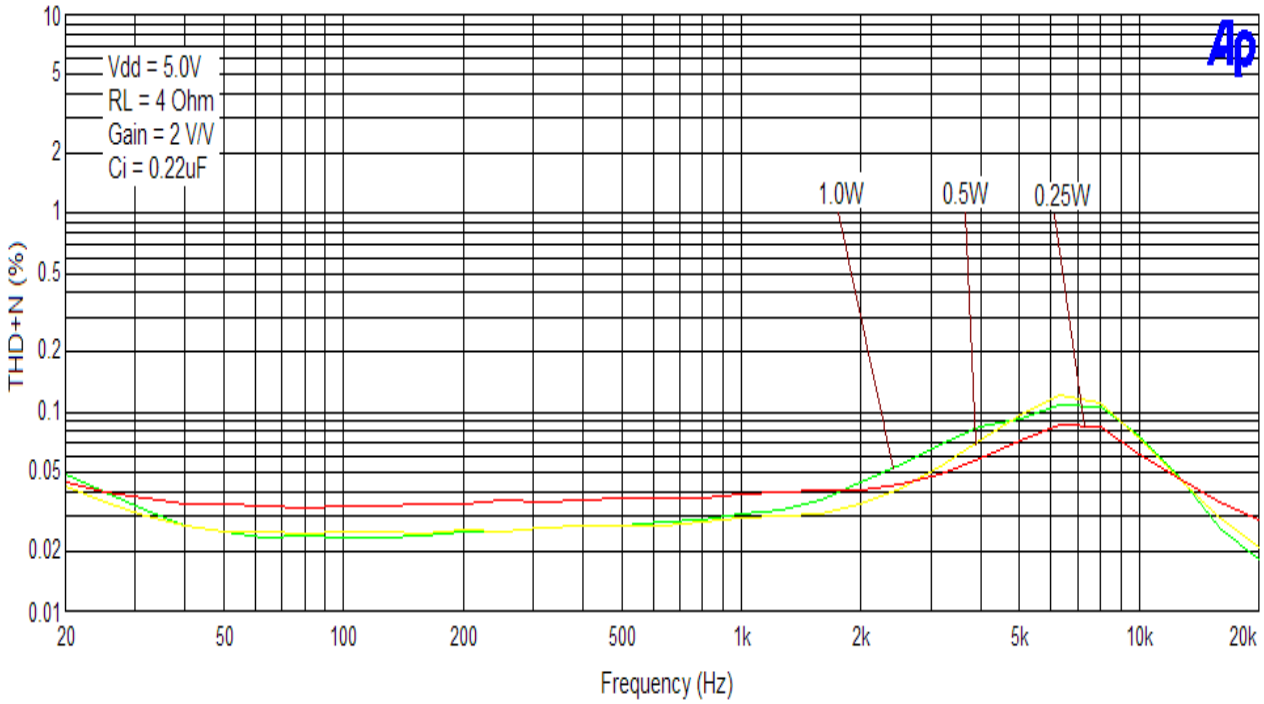


Figure 6
Total Harmonic Distortion + Noise vs Frequency (VDD=3.6V, 4Ω)

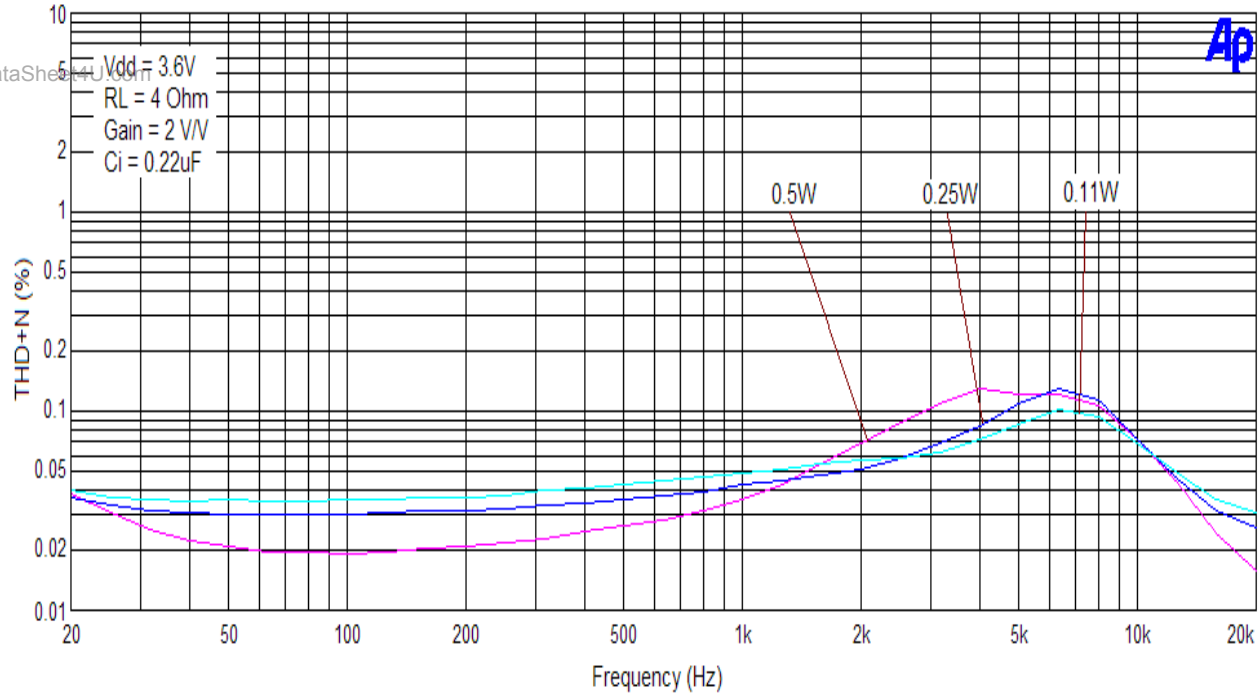


Figure 7
Total Harmonic Distortion + Noise vs Frequency (VDD=2.5V, 4Ω)

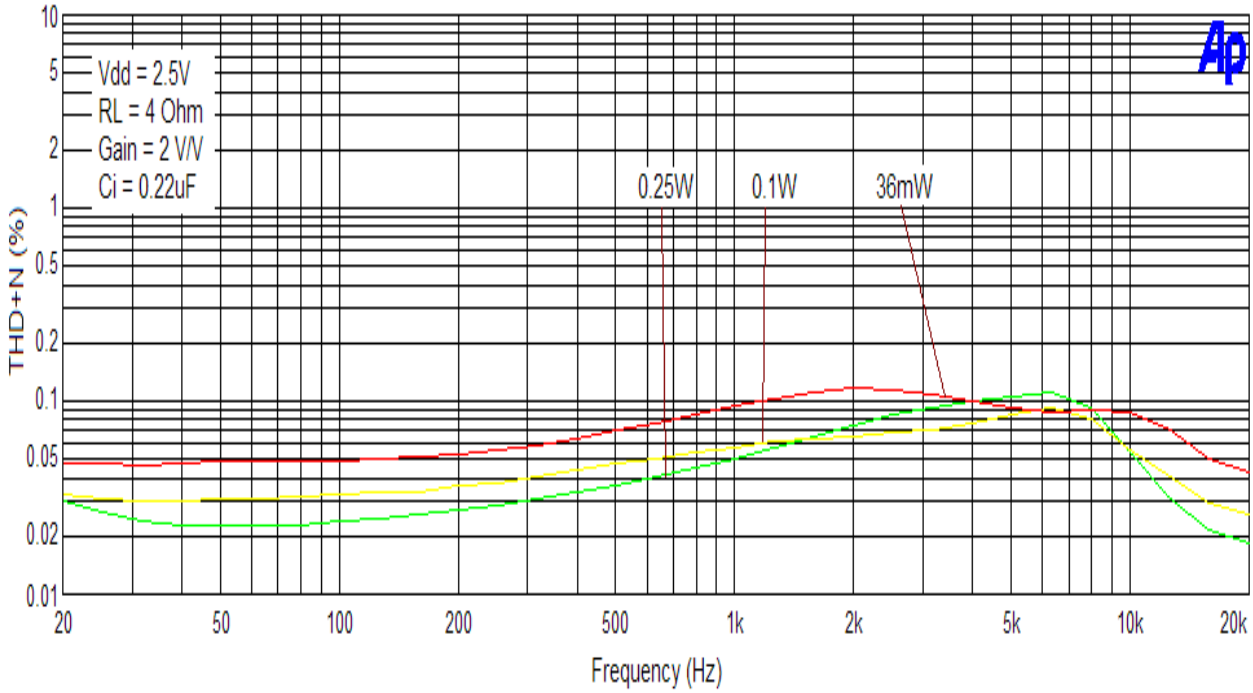


Figure 8
Total Harmonic Distortion + Noise vs Frequency (VDD=5.0V, 8Ω)

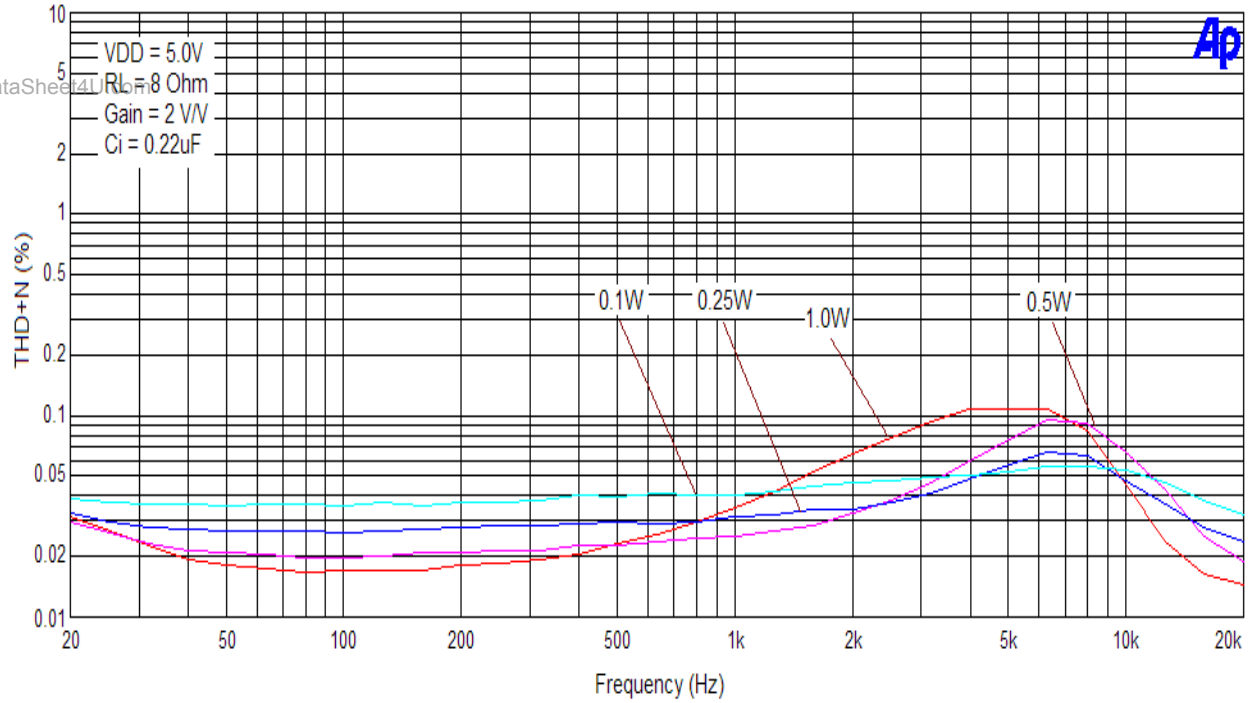


Figure 9
Total Harmonic Distortion + Noise vs Frequency (VDD=3.6V, 8Ω)

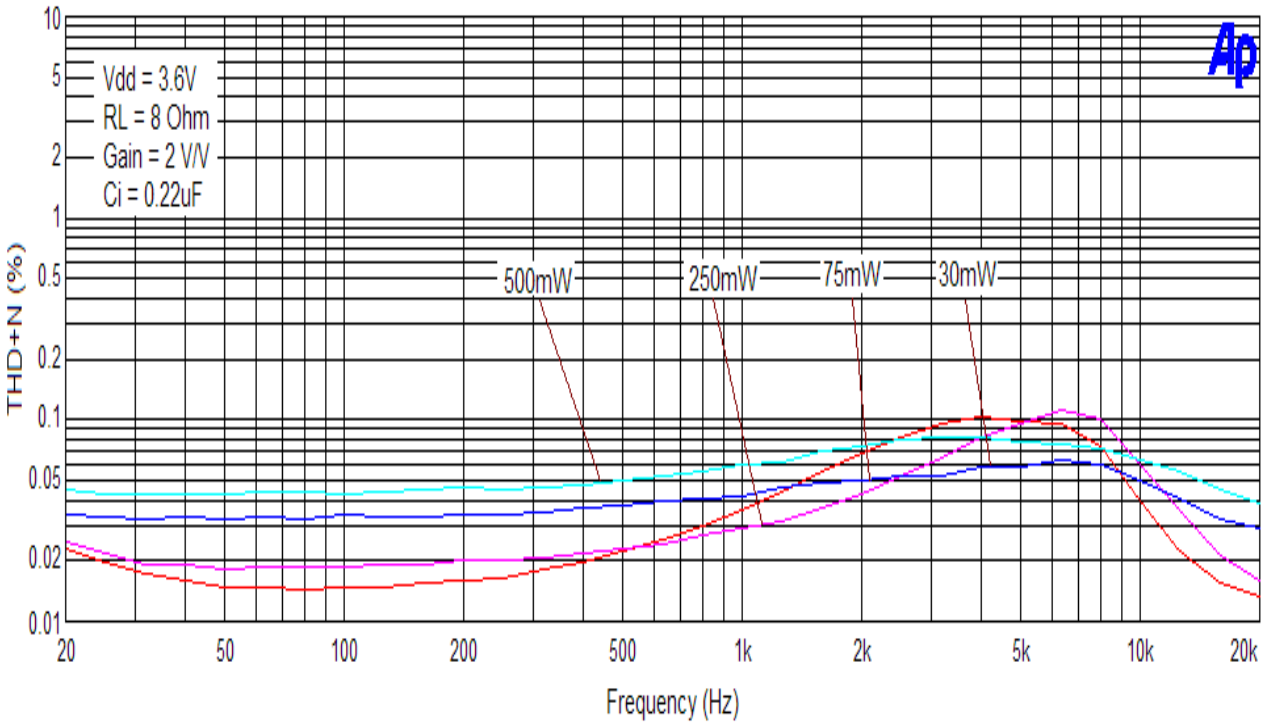


Figure 10
Total Harmonic Distortion + Noise vs Frequency (VDD=2.5V, 8Ω)

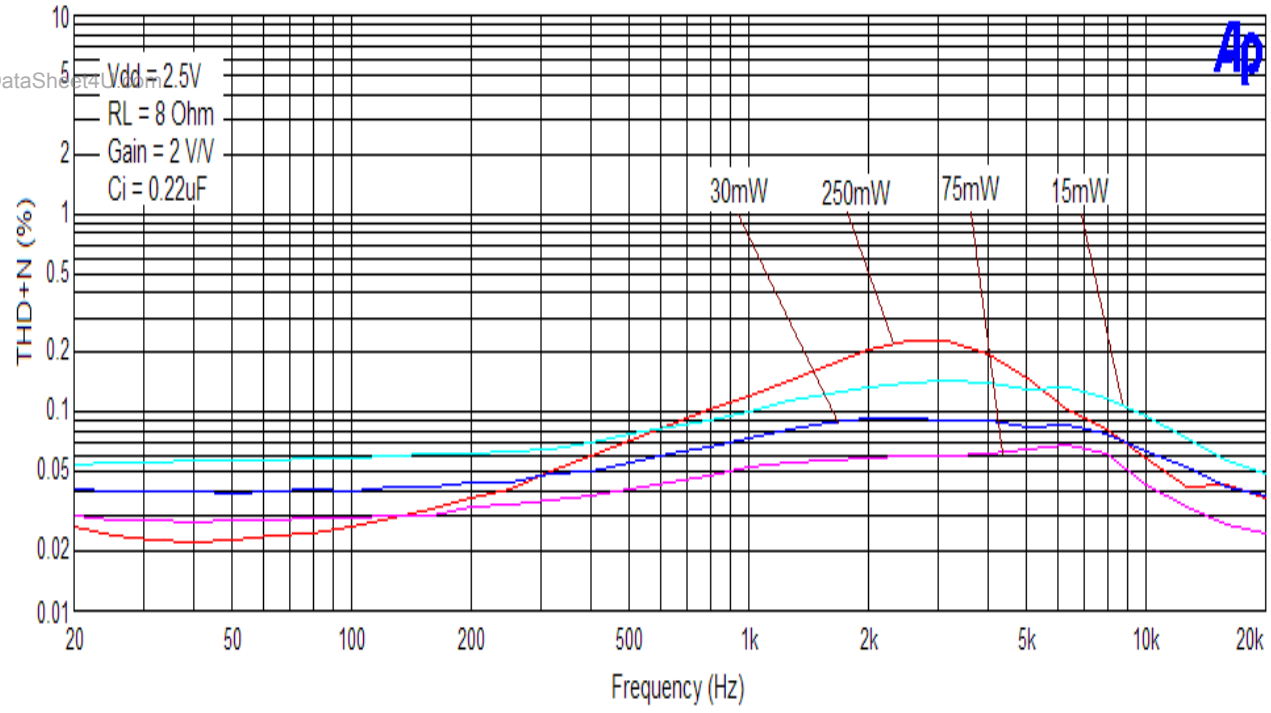


Figure 11
Efficiency vs Output power (RL=4Ω, 33μH)

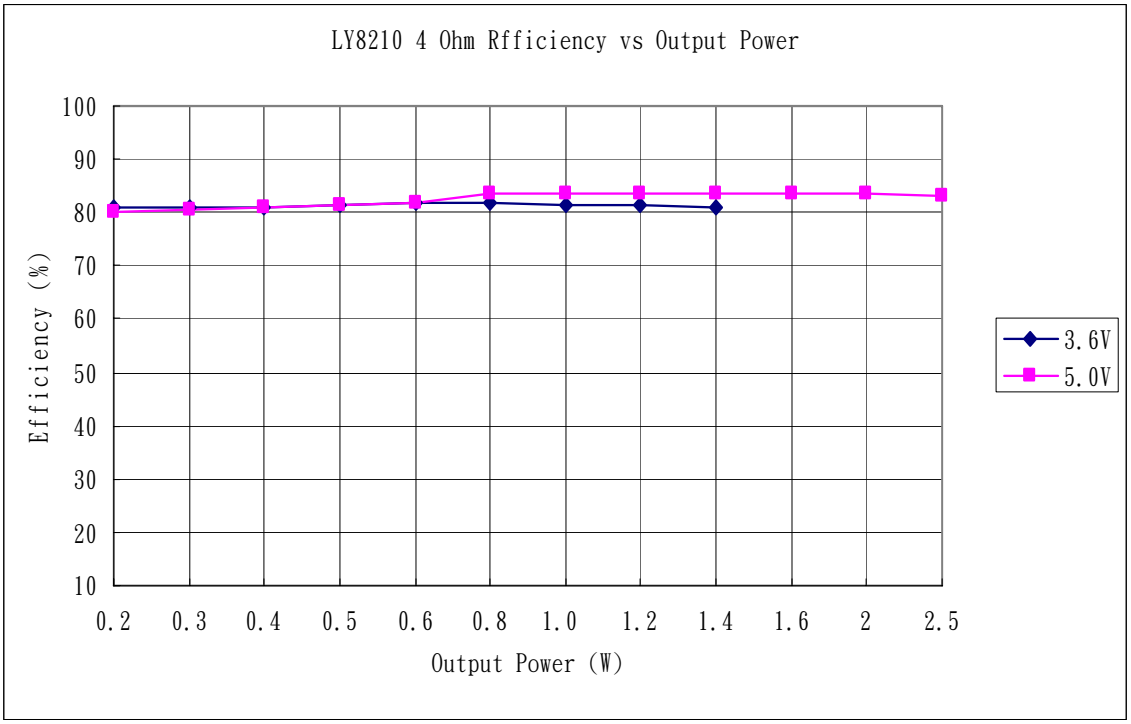
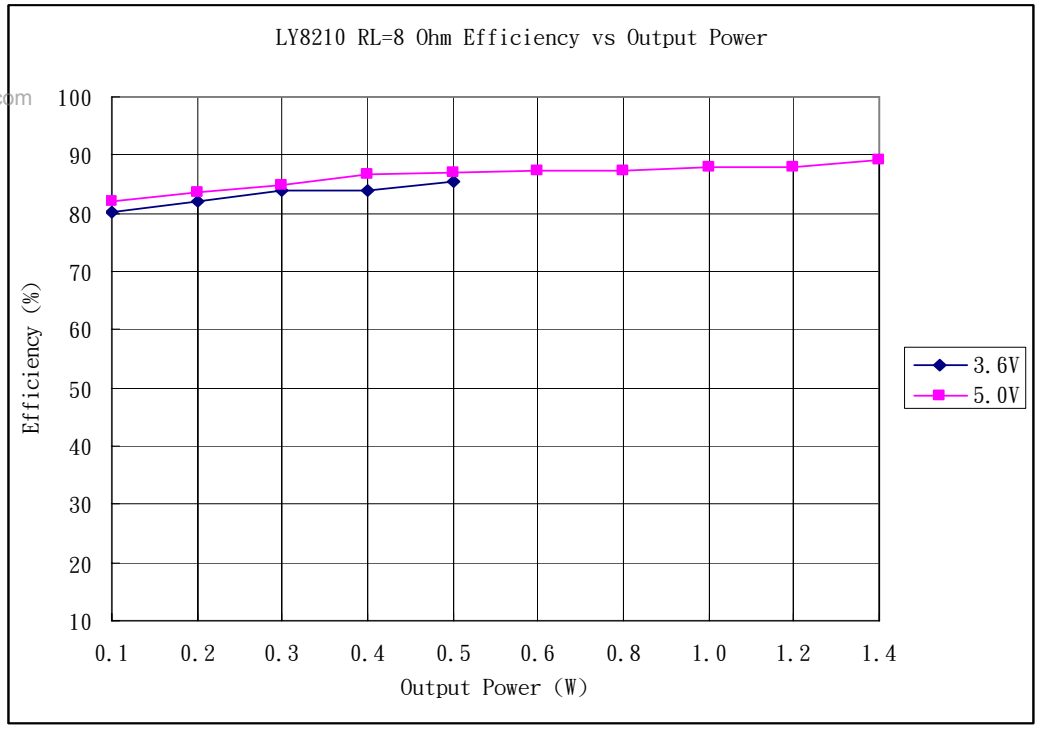


Figure 12
Efficiency vs Output power (RL=8Ω, 33μH)



▪ APPLICATION INFORMATION

Fully Differential Amplifier

The LY8210 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential LY8210 can still be used with a single-ended input; however, the LY8210 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

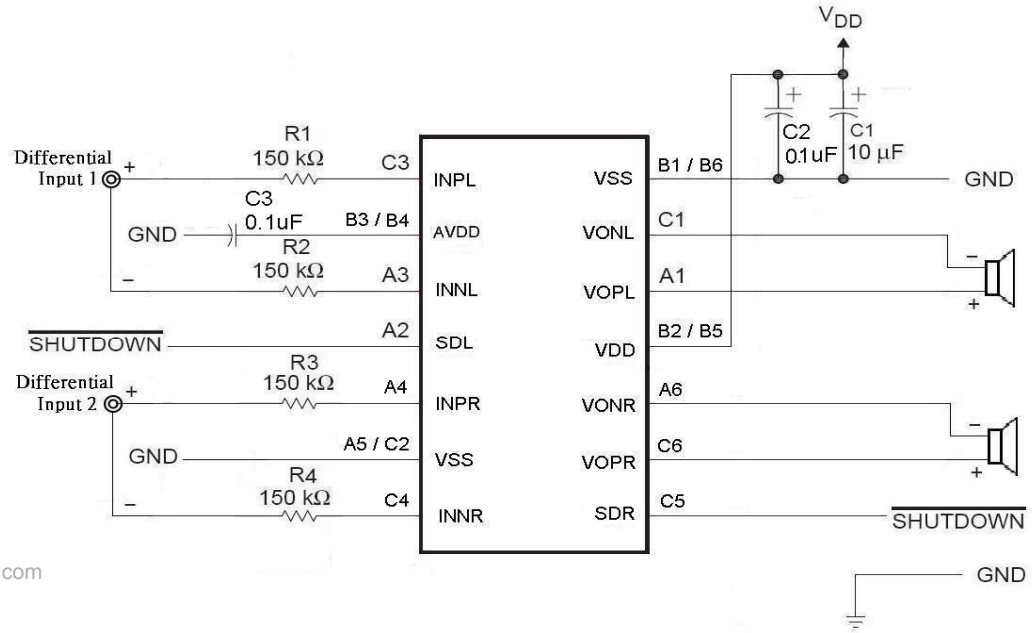


Figure 13. Application Schematic With Differential Input Configuration(WCSP Package)

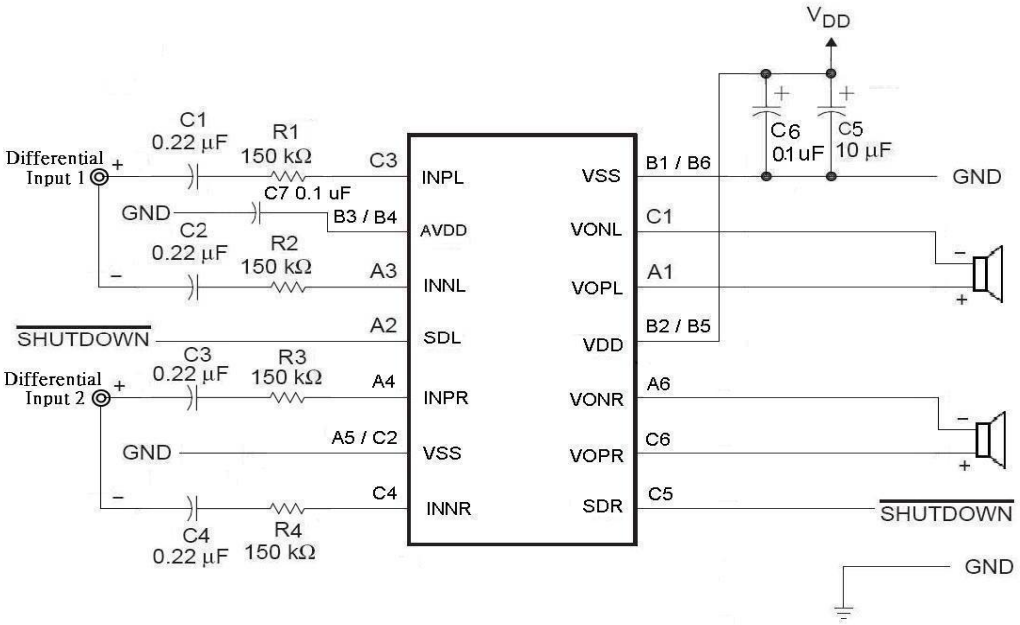


Figure 14. Application Schematic With Differential and Capacitors Input Configuration(WCSP Package)

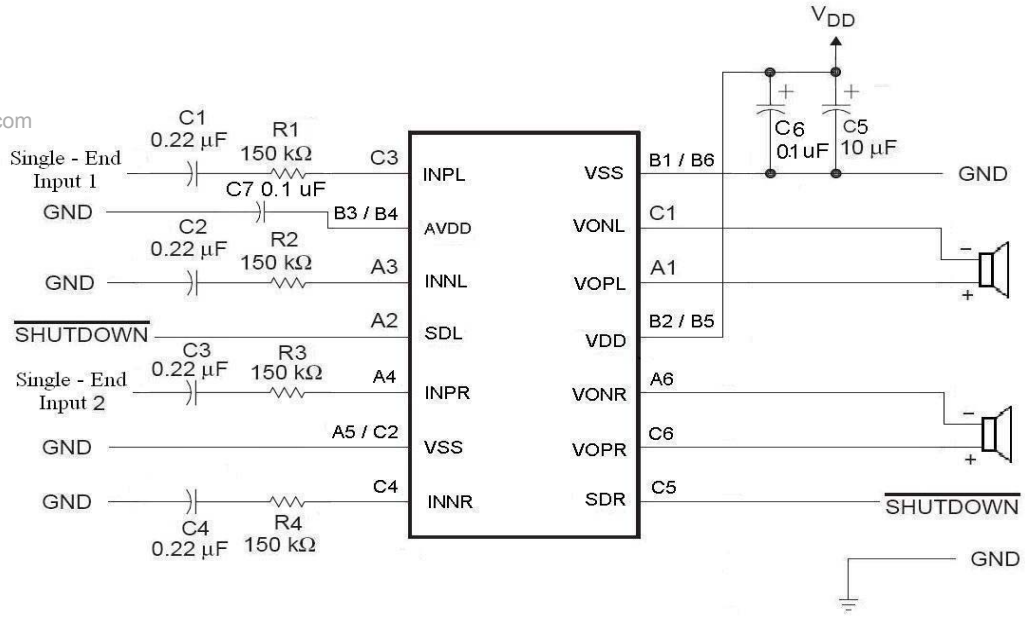


Figure 15. Application Schematic With Single-Ended Input Configuration(WCSP Package)

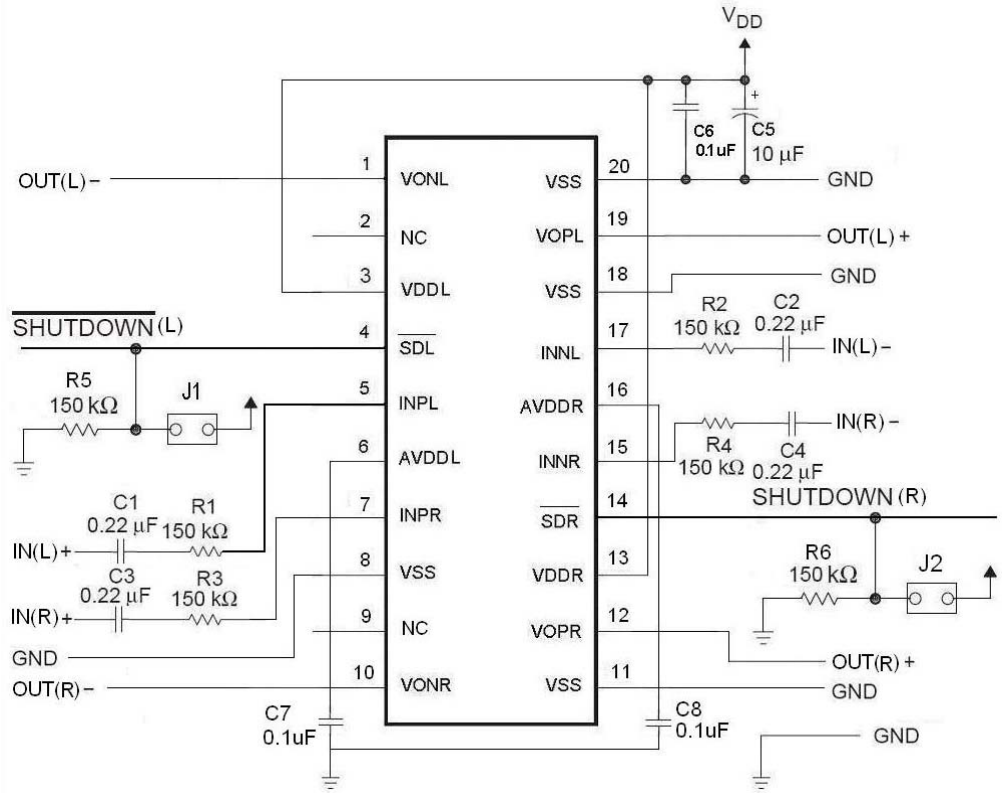


Figure 16. Application Schematic With Differential and Capacitors Input Configuration(TSSOP Package)

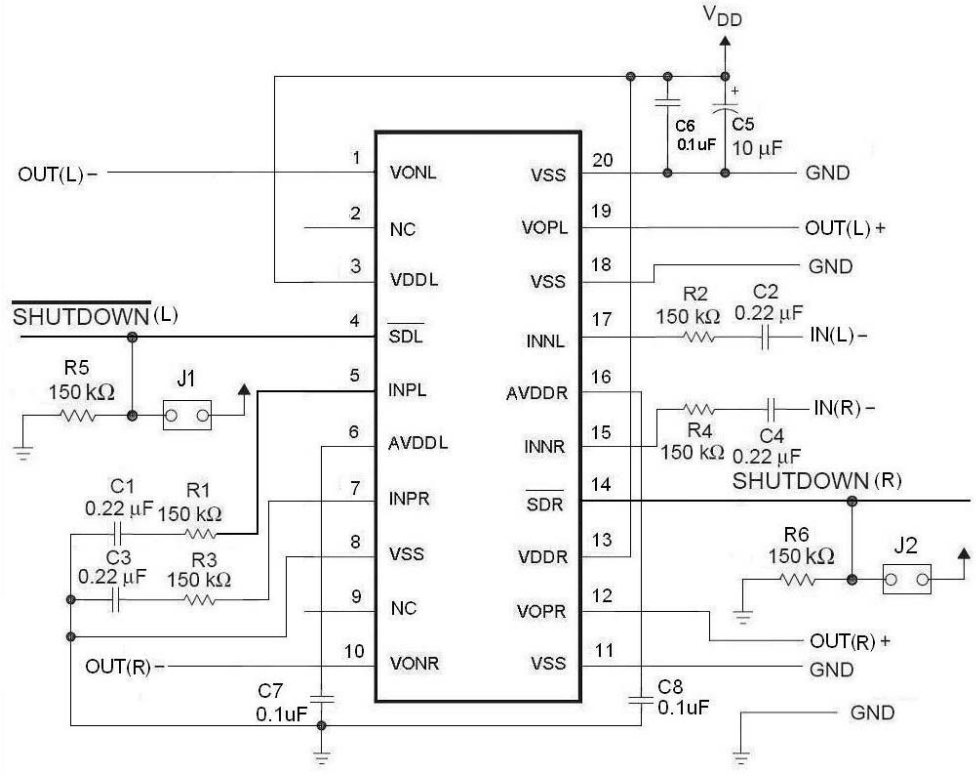


Figure 17. Application Schematic With Single-Ended Input Configuration(TSSOP Package)

Input Resistors (Ri) and Gain

The LY8210 has two internal amplifier stages. The pre-amplifier gain is externally configurable, while the total gain is internally fixed. The closed-loop gain of the pre-amplifier gain is set by selecting the Rf to Ri while the total gain is fixed at 2x. So the input resistors (R_i) set the gain of the amplifier according to the equation.

Pre-Amplifier Gain = Rf / Ri

Total Gain = (Rf / Ri) x 2

A_{VD} = 20 x log [2 x (Rf /Ri)]

The resistor matching is very important in the amplifiers. Balance of the output on the reference voltage depends on matched ratio of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance.
Resistor arrays with 1% matching can be used with a tolerance greater than 1%.Place the input resistors very close to the LY8210 to limit noise injection on the high-impedance nodes. For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the LY8210 to operate at its best,

For example

Table 1. Typical Total Gain and A_{VD} Values

Rf (KΩ)	150	150	150	150	150	150
Ri (KΩ)	150	75	50	37.5	25	18.75
Pre AMP. Gain	1	2	3	4	6	8
Total Gain	2	4	6	8	12	16
A_{VD} (db)	6.02	12.04	15.56	18.06	21.58	24.08

Input Capacitors (Ci)

The LY8210 using fully differential source, So the input coupling capacitors are required. The input capacitors and input resistors form a high-pass filter with the corner frequency(f_c), determined in the equation.

$f_c = 1 / (2\pi R_i C_i)$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Equation is reconfigured to solve for the input coupling capacitance.

$C_i = 1 / (2\pi R_i f_c)$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For example

In the table 2 shows the external components. Rin in connect with Cin to create a high-pass filter.

Table 2. Typical Component Values

Reference	Description	Note
Ri	150KΩ	1% tolerance resistors
Ci	0.22uF	80%/–20%

Ci = 1 / (2πRi fc)

Ci = 1 / (2π x 150KΩ x 4.8Hz)=0.221uF，Use 0.22uF

Decoupling Capacitor (Cs)

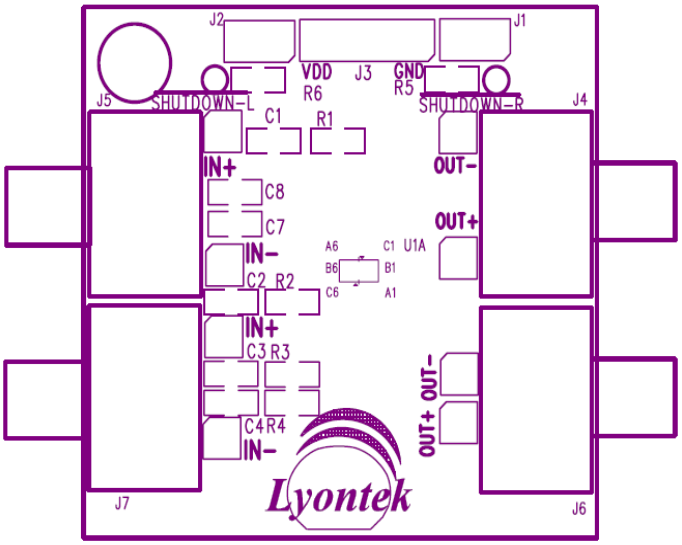
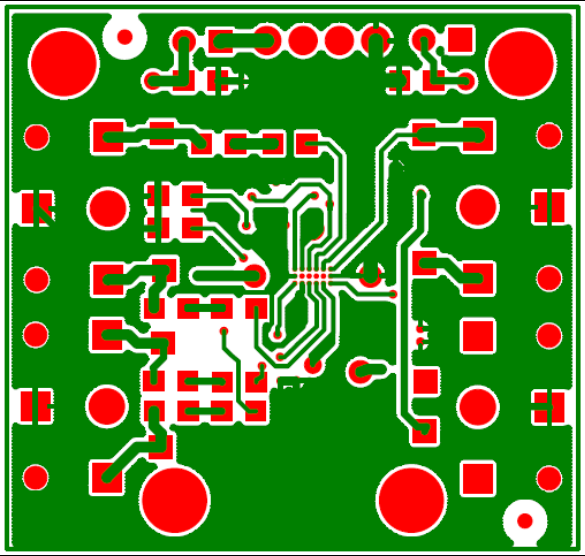
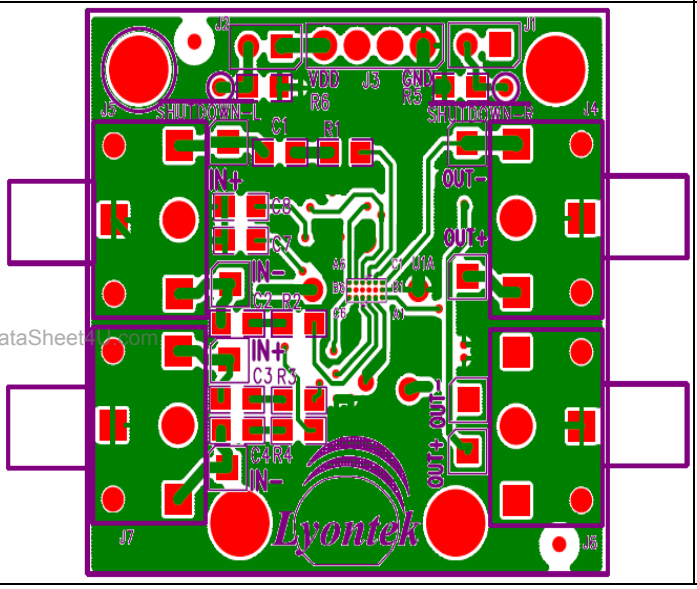
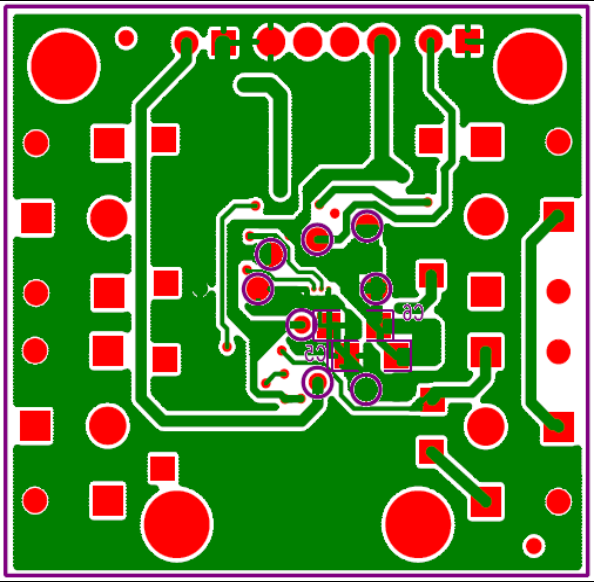
The LY8210 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1.0uF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the LY8210 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10.0uF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

PCB Layout

All the external components must place very close to the LY8210. The input resistors need to be very close to the LY8210 input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the LY8210. Then place the decoupling capacitor Cs, close to the LY8210 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Making the high current traces going to VDD, GND, V_{O+} and V_{O-} pins of the LY8210 should be as wide as possible to minimize trace resistance. If these traces are too thin, the LY8210's performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

LY8210CL Demo Board Artwork

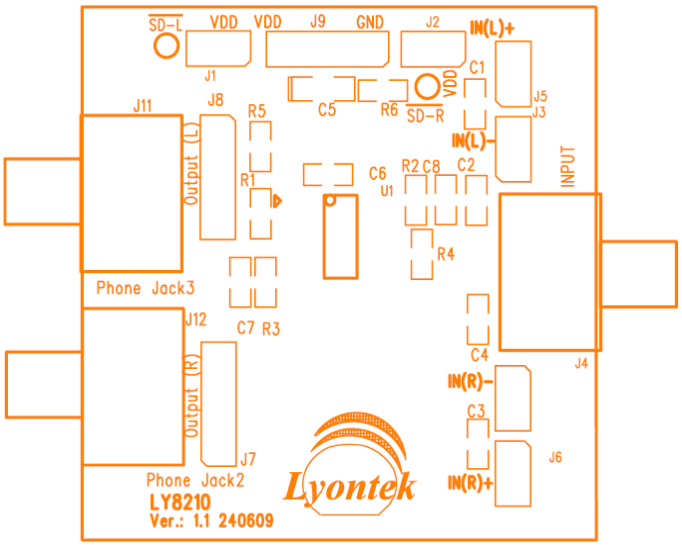
Top Silkscreen	Top Layer
	
Composite view	**Bottom Layer**
	

LY8210 V1.1 BOM List

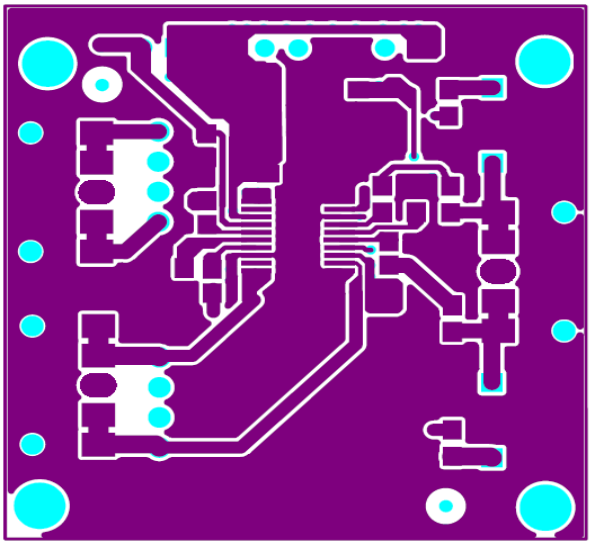
No.	Description	Reference	Note
1	Resistor, 150KΩ	R1,R2,R3,R4,R5,R6	
2	Capacitor, 0.1uF	C6,C7,C8	
3	Capacitor, 0.22uF	C1,C2,C3,C4	
4	Capacitor, 10.0uF	C5	
5	LY8210CL	U1	
6	1*2 Pin Header	J1,J2	Close → Active

LY8210AL/IL Demo Board Artwork

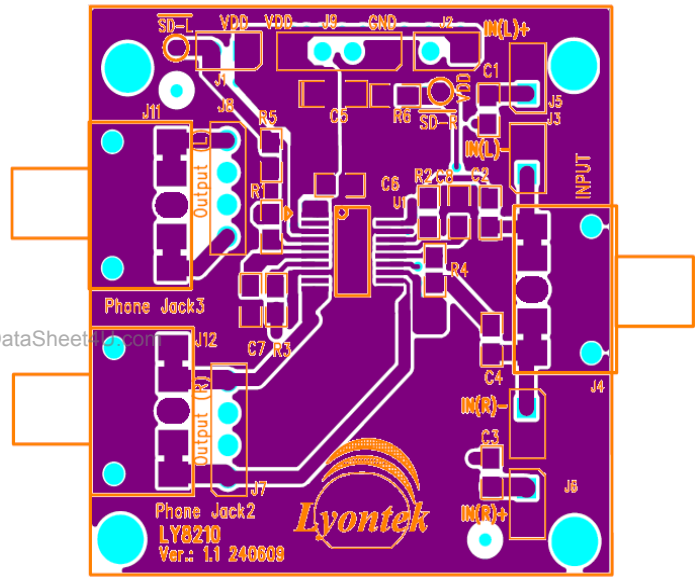
Top Silkscreen



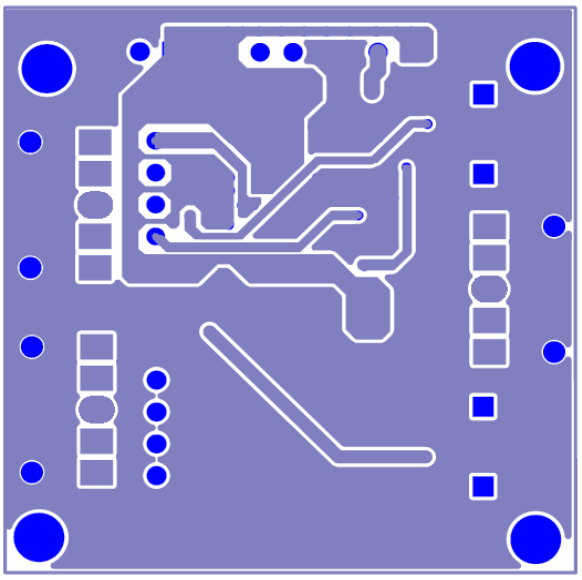
Top Layer



Composite view



Bottom Layer

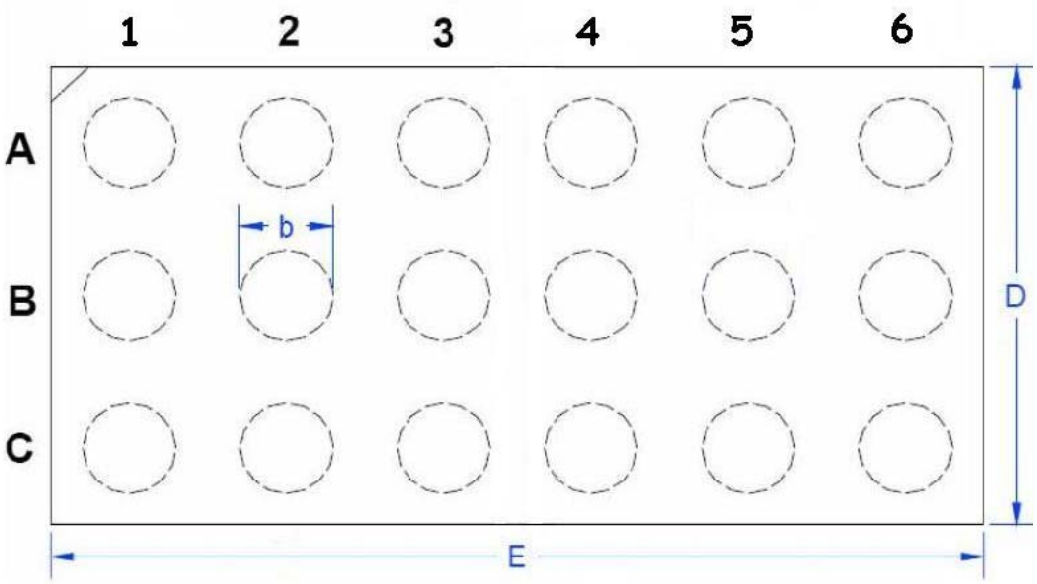


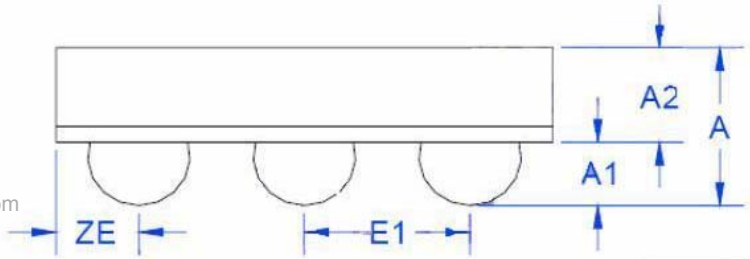
LY8210 V1.1 BOM List

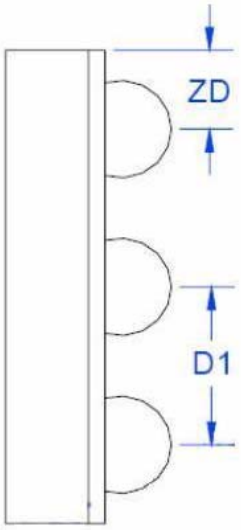
No.	Description	Reference	Note
1	Resistor, 150KΩ	R1,R2,R3,R4,R5,R6	
2	Capacitor, 0.1uF	C6,C7,C8	
3	Capacitor, 0.22uF	C1,C2,C3,C4	
4	Capacitor, 10.0uF	C5	
5	LY8210AL/IL	U1	
6	1*2 Pin Header	J1,J2	Close → Active

PACKAGE OUTLINE DIMENSION

18 Ball WCSP Package Outline Dimension

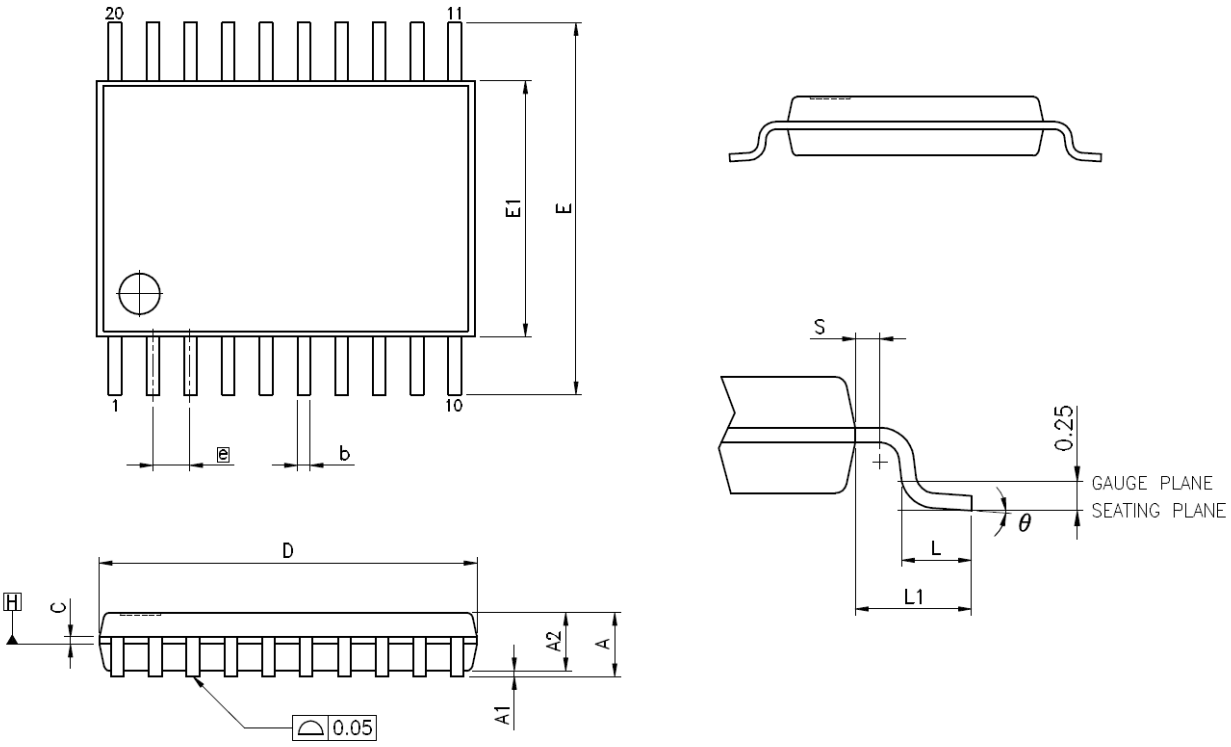






SYMBOL	DIMENSION(mm)		
	MIN	NOM	MAX
A			0.675
A1	0.200	0.230	0.260
A2	0.4000	0.4075	0.4150
b	0.270	0.320	0.370
E	2.900	3.000	3.100
D	1.450	1.500	1.550
D1		0.500	
E1		0.500	
ZD		0.230	
ZE		0.230	

TSSOP 20 Pin Package Outline Dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	0.90	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	–	–
θ	0°	–	8°