LZ92E19 Timing Pulse Generator LSI for 2/3" CCD

Description

The LZ92E19 is a CMOS timing pulse generator LSI. Used in combination with the LZ92B31 defect compensator LSI, it provides drive timing pulses, color separation sampling pulses and signal processing pulses for 2/3" CCD area sensor.

Features

1. Applicable to both NTSC and PAL systems
2. Applicable to both field and frame integration modes
3. Applicable to four different color filter orders
   - Color filter coordinate of RGB order (frame integration mode)

     B G
     R G
     G R
     R B
   - Green stripe order (frame integration mode)

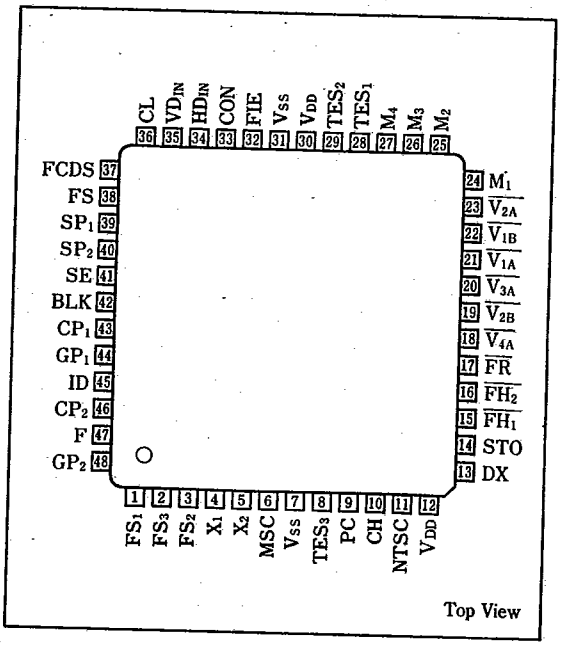
     B G
     B G
     R G
     R G
   - Mg-G alternate and Ye-Cy complement order (field integration mode)

     Ye Cy
     Mg G
     Ye Cy
     G Mg
   - Ye-Cy alternate and Mg-G complement order (field integration mode)

     Ye Cy
     G Mg
     Cy Ye
     G Mg
4. 48-pin quad flat package

*Combination of the LZ92B31 defect compensator LSI, ROM recorded with the address of a defective pixels and the IR3P47 process IC or an S/H circuit allows compensation of signals preceding by one pixel in black-and-white, and by two pixels in color.

Pin Connections



Top View

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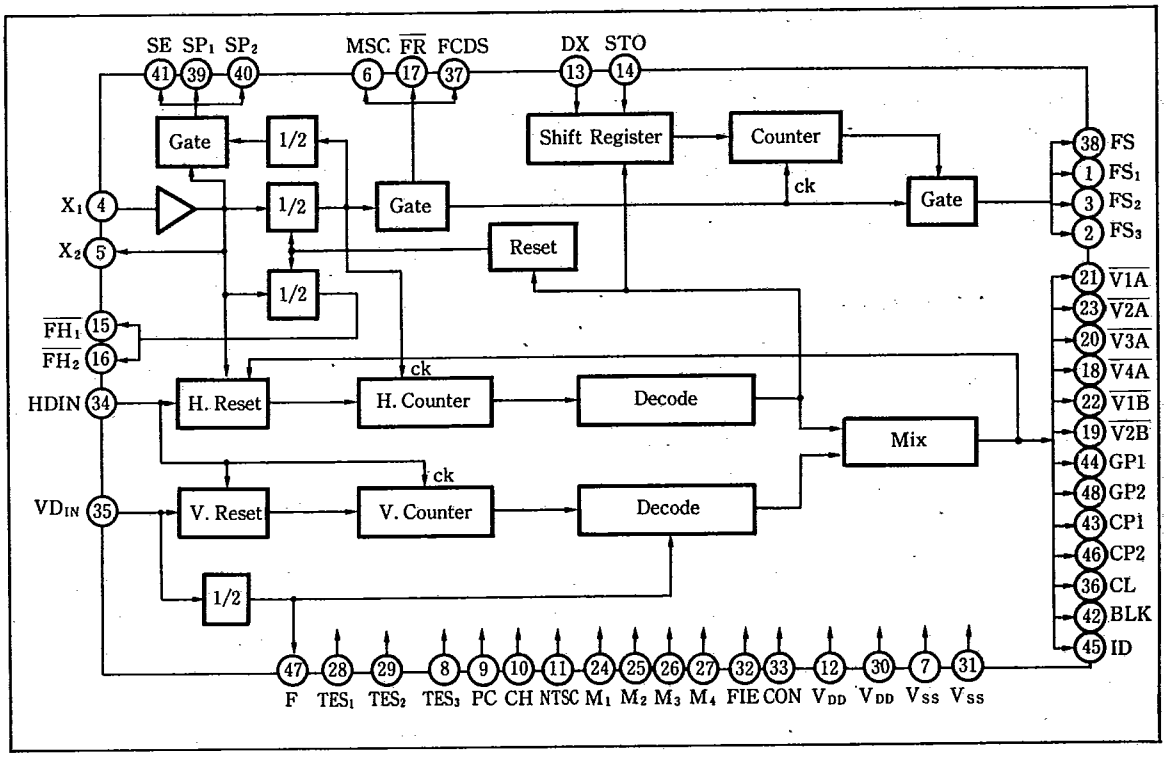
Block Diagram



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■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{CC}	7	V	1
Input voltage	V_I	−0.3 to V_{CC}+0.3	V	2
Output voltage	V_O	−0.3 to V_{CC}+0.3	V	
Operating temperature	T_{opr}	−10 to +70	℃	
Storage temperature	T_{stg}	−55 to +150	℃	

Note 1 : The maximum applicable voltage on any pin with respect to GND.
Note 2 : The maximum applicable voltage on input pin excepting V_{CC} with respect to GND.

■ Recommended Operating Conditions

(V_{CC}=+5V±5%, Ta=−10 to +70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Operating temperature	T_{opr}	−10		+70	℃

■ Electrical Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input "Low" voltage	V_{IL}				0.8	V	1
Input "High" voltage	V_{IH}		2.0			V	1
Output "Low" voltage	V_{OL}	I_{OL}=4mA			0.4	V	2
Output "High" voltage	V_{OH}	I_{OH}=−2mA	4.0			V	2
Input "Low" current	$\lvert I_{IL1} \rvert$	V_I=0V			10	μA	3
	$\lvert I_{IL2} \rvert$	V_I=0V	10		50	μA	4
Input "High" current	I_{IH}	V_I=V_{CC}			10	μA	2
Current consumption 1	I_{CC1}	V_{IN}=V_{CC} or GND			10	μA	
Current consumption 2	I_{CC2}	V_{IN}=V_{CC}, f=19MHz V_{IN}=0V during pattern operation			50	mA	

Note 1 : Applied to all input pins.
Note 2 : Applied to all output pins.
Note 3 : Applied to pins X_1, TES_1, TES_2 and TES_3.
Note 4 : Applied to pins PC, CH, NTSC, DX, STO, M_1, M_2, M_3, M_4, FIE and CON.

Pin Functions

Pin No.	Symbol	I/O	Pin name	Description
1	FS_1	O	Sampling pulse 1	The FS_1 pin outputs a pulse to sample and hold the CCD signal for defect compensation, used in combination with the defect compensation ROM. It does not sample and hold the signals preceding a defective pixels by one and two pixels.
2	FS_3	O	Sampling pulse 3	The FS_3 pin outputs a pulse to sample and hold the CCD signal. It outputs consecutive pulses irrespective of defect compensation.
3	FS_2	O	Sampling pulse 2	The FS_2 pin outputs a pulse to sample and hold a signal preceding a defective pixel by two pixels. It outputs at the position where there is a defective pixel.
4	X_1	I	Clock input	The X_1 pin inputs a reference clock oscillation. Frequency for NTSC system : 19.164333MHz Frequency for PAL system : 19.031250MHz
5	X_2	O	Clock output	The X_2 pin outputs a reference clock oscillation.
6	MSC	O	1/2 dividing output	The MSC pin outputs 1/2 dividing pulse of a reference clock. The output phase is a consecutive signal which has the same phase as the FH_1.
7	V_{SS}	—	Ground	The V_{SS} is a ground pin.
8	TES_3	I	Test 3	The TES_3 input pin is used to test, and is normally kept Low.
9	PC	IU	Pulse control	The PC pin controls the SP_1 (pin 39) and SP_2 (pin 40), The PC pin going Low allows both SP_1 and SP_2 pins to go Low.
10	CH	IU	Color filter order selection	The CH pin selects the timing of SP_1 (pin 39), SP_2 (pin 40), SE (pin 41) and ID (pin 45) in accordance with the CCD color filter order, used in combination with the FIE (pin 32).
11	NTSC	IU	NTSC/PAL	The NTSC pin selects the TV system.
12	V_{DD}	—	+5V power supply	The V_{DD} is a +5V power supply pin.
13	DX	IU	ROM data input	The DX pin inputs the ROM data of defective position on CCD horizontal pixels. It must be kept High or open when not in use.
14	STO	IU	Strobe input	The STO pin inputs strobe pulses used to input the ROM data of defective position on CCD horizontal pixels.
15	$\overline{FH_1}$	O	Horizontal transfer pulse	The $\overline{FH_1}$ pin outputs the CCD horizontal transfer pulse. It is connected to the ϕH1 through the inverted boost driver.
16	$\overline{FH_2}$	O	Horizontal transfer pulse	The $\overline{FH_2}$ pin outputs the CCD horizontal transfer pulse. It is connected to the ϕH2 through the inverted boost driver.
17	$\overline{FR}$	O	Reset pulse	The $\overline{FR}$ pin outputs the CCD reset pulse. It is connected to the ϕ_R through the inverted boost driver.
18	$\overline{V4A}$	O	Vertical transfer pulse	The $\overline{V4A}$ pin outputs the CCD vertical transfer pulse. It is connected to the ϕV4 through the inverted driver.
19	$\overline{V2B}$	O	Vertical transfer pulse	The $\overline{V2B}$ pin outputs a pulse which transfers the CCD photo diode charge to the vertical register.
20	$\overline{V3A}$	O	Vertical transfer pulse	The $\overline{V3A}$ pin outputs the CCD vertical transfer pulse. It is connected to the ϕV3 through the inverted driver.
21	$\overline{V1A}$	O	Vertical transfer pulse	The $\overline{V1A}$ pin outputs the CCD vertical transfer pulse. It is connected to the ϕV1 through the inverted driver.
22	$\overline{V1B}$	O	Vertical transfer pulse	The $\overline{V1B}$ pin outputs the pulse which transfers the CCD photo diode charge to the vertical register.
23	$\overline{V2A}$	O	Vertical transfer pulse	The $\overline{V2A}$ pin outputs the CCD veritical transfer pulse. It is connected to the ϕV2 through the inverted driver.
24	M_1	IU	FCDS phase control	The M_1 and M_2 pins control the phase of the FCDS (pin 37) with respect to the FH_1.
25	M_2	IU		
26	M_3	IU	FS phase control	The M_3 and M_4 pins control the phase of the FS_1 (pin 1), FS_3 (pin 2), FS_2 (pin 3) and FS (pin 38) with respect to the FH_1.
27	M_4	IU		
28	TES_1	I	Test 1	The TES_1 is a test pin, and normally kept Low.
29	TES_2	I	Test 2	The TES_2 is a test pin, and normally kept Low.

Pin No.	Symbol	I/O	Pin name	Description
30	V_{DD}	—	+5V power supply	The V_{DD} is a+5V power supply pin.
31	V_{SS}	—	Ground	The V_{SS} is a ground pin.
32	FIE	IU	Field/Frame selection	The FIE input selects the CCD integration mode. · High level : field integration mode · Low level : frame integration mode The $\overline{V1A}$ (pin 21), $\overline{V2A}$ (pin 23), $\overline{V3A}$ (pin 20), $\overline{V4A}$ (pin 18), $\overline{V1B}$ (pin 22) and $\overline{V2B}$ (pin 19) make a change in pulse output timing. The FIE input in combination with the CH input (pin 10) allows the SP_1 (pin 39), SP_2 (pin 40), SE (pin 41) and ID (pin 45) to be output with the signals according to CCD color filter order.
33	CON	IU	Control	The CON input pin selects the SSG. · High level : LR3740 · Low level : LR3740N MN6064R (NTSC system) MN6160PA, B (PAL system)
34	HD_{IN}	I	H reference input	The HD_{IN} pin is connected to the HP (pin 17) of the defect compensation IC LZ92B31 in order to input an horizontal reference signal synchronized with the X_1 (pin 4).
35	VD_{IN}	I	V reference input	The VD_{IN} pin inputs the vertial reference signal from SSG · NTSC system : LR3740N—VD* LR3740—VD* MN6064R—VP* · PAL system : MN6160PA, PB—VP* *The pulses must be input without changing their polarity. However, the MN system requires level change.
36	CL	O	Cleaning pulse	The CL pin outputs a pulse for cleaning the CCD signal during pause time of horizontal transfer pulse.
37	FCDS	O	CDS pulse	The FCDS pin outputs a pulse to reduce Low band noise of CCD signal.
38	FS	O	Sampling pulse	The FS pin outputs a pulse to sample and hold the CCD signal.
39	SP_1	O	Color sampling pulse	The SP_1 pin outputs a pulse for color separation to sample and hold the CCD signal. · Frame integration : Sample and hold the signal for G · Field integration : Sample and hold the signal for Mg+Cy or Mg+Ye
40	SP_2	O	Color sampling pulse	The SP_2 pin outputs a pulse for color separation to sample and hold the CCD signal. · Frame integration : Sample and hold the signal for G or B · Field integration : Sample and hold the signal for G+Cy or G+Ye
41	SE	O	Color selection signal	The SE pin outputs a pulse which will be inverted for every CCD pixel signal. The pulse is changed by the FIE (pin 32) and the CH (pin 10). It is used in : · Frame integration for formation of high band luminous signal · Field integration for color separation based upon synchronous detection.
42	BLK	O	Pre-blanking pulse	The BLK pin outputs a consecutive blanking pulse with 1H cycle. It is used for the circuit preceding encoder.
43	CP_1	O	Clamp pulse 1	The CP_1 outputs a consecutive clamp pulse with 1H cycle. It is used for in the matrix circuit.
44	GP_1	O	Optical black clamp pulse 1	The GP_1 outputs a pulse to clamp optical black signals from CCD. It is a composite output which goes Low during the absense of effective pixels within the vertical blanking period.
45	ID	O	Index pulse	The ID pin outputs a line index pulse for color separation. To input the FIE (pin 32) and the CH (pin 10) changes the output timing.
46	CP_2	O	Clamp pulse 2	The CP_2 pin outputs a consecutive clamp pulse with 1H cycle. It is used in the encoder circuit.

Pin No.	Symbol	I/O	Pin name	Description
47	F	O	Field pulse	The F pin outputs a field reference pulse. High level : NTSC ODD field PAL 2nd, 4th field Low level : NTSC EVEN field PAL 1st, 3rd field
48	GP_2	O	Optical black pulse 2	The GP_2 outputs a pulse to clamp optical black signals from CCD. It is delayed approx. 600ns in phase with respect to the GP_1 (pin 43).

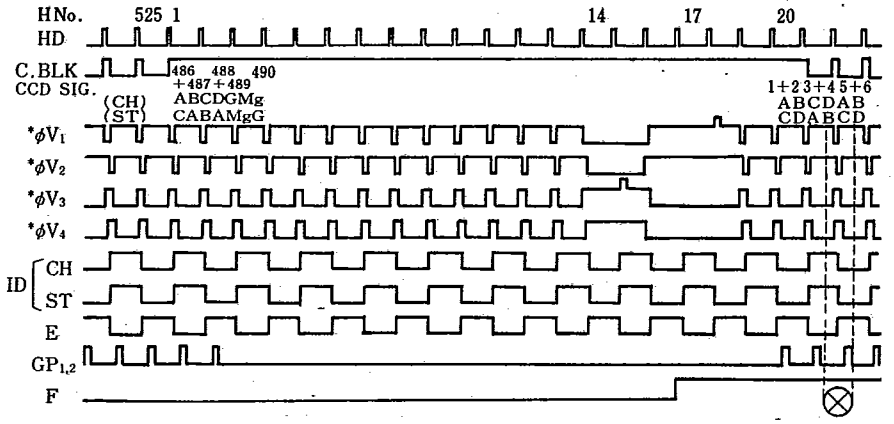
I : Input pin
IU : Input pin with a pull-up resistor
O : Output pin

■ Timing Diagram

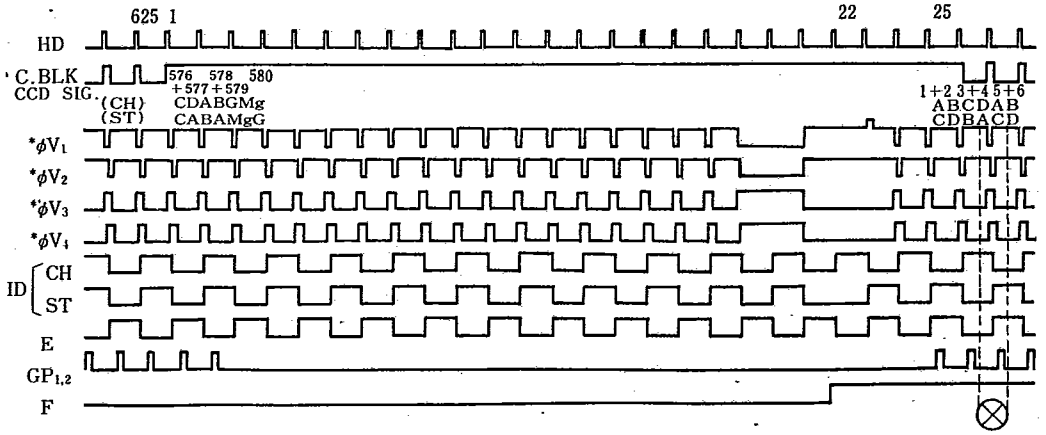
A : Ye+Mg
B : Cy+G
C : Ye+G
D : Cy+Mg

(1) Field transfer

• NTSC (Odd field)

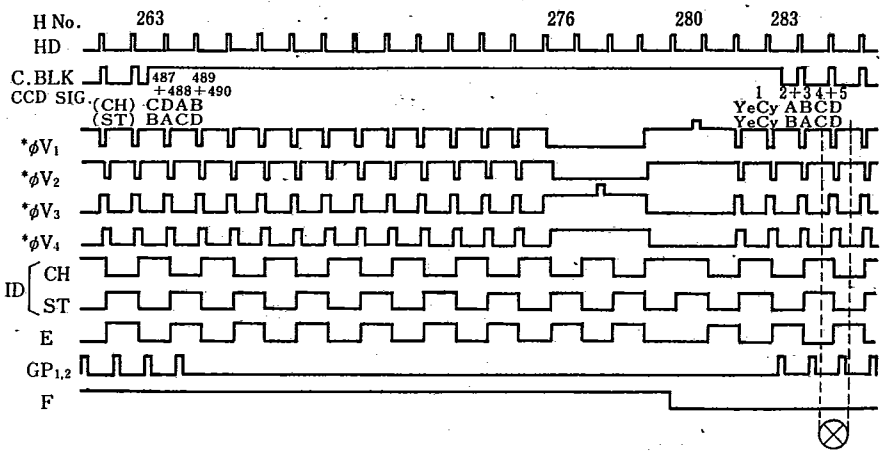


• PAL (2nd and 4th Field)



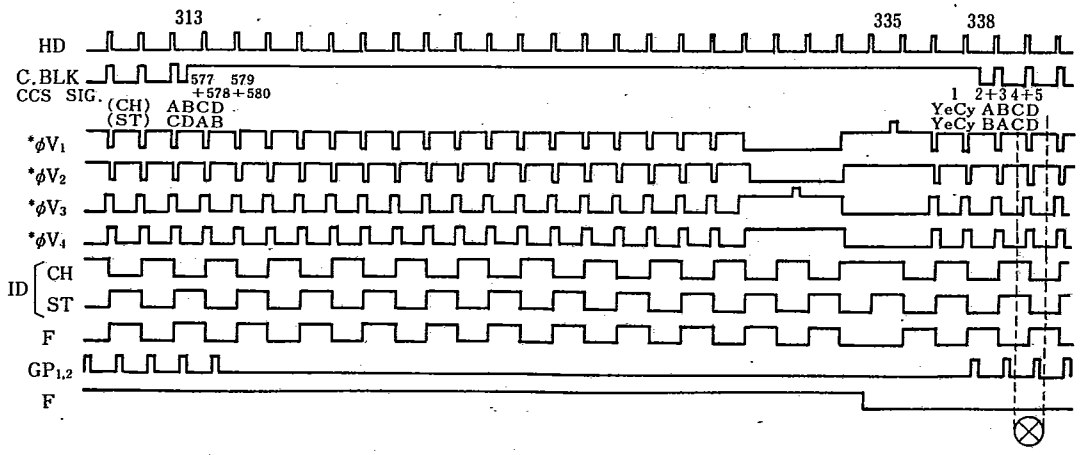
(2) Field transfer

• NTSC (Even field)



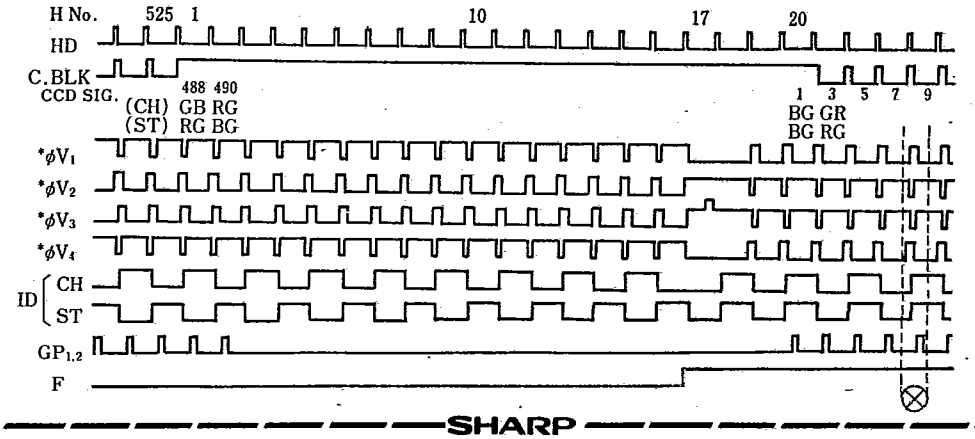
* ϕV_1-ϕV_4 pulses apply to the CCD.

• PAL (1st and 3rd Field)

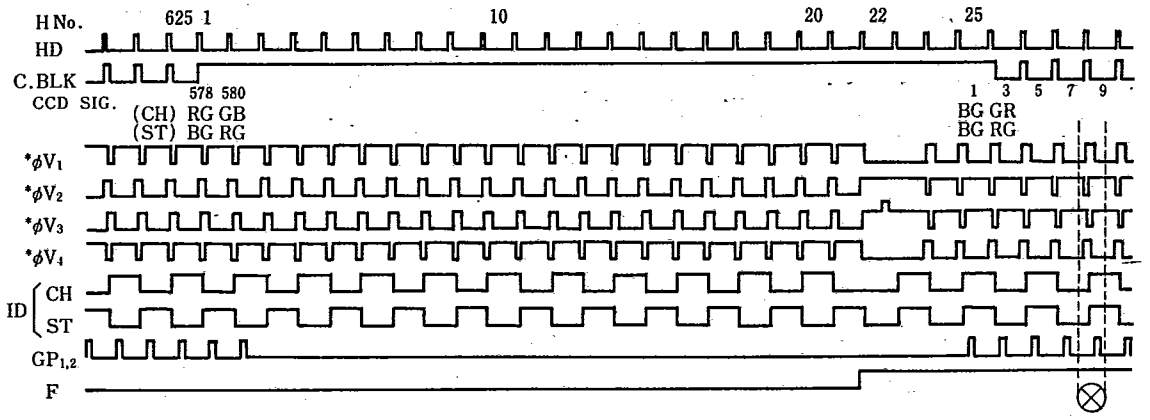


(3) Frame transfer

• NTSC (Odd field)



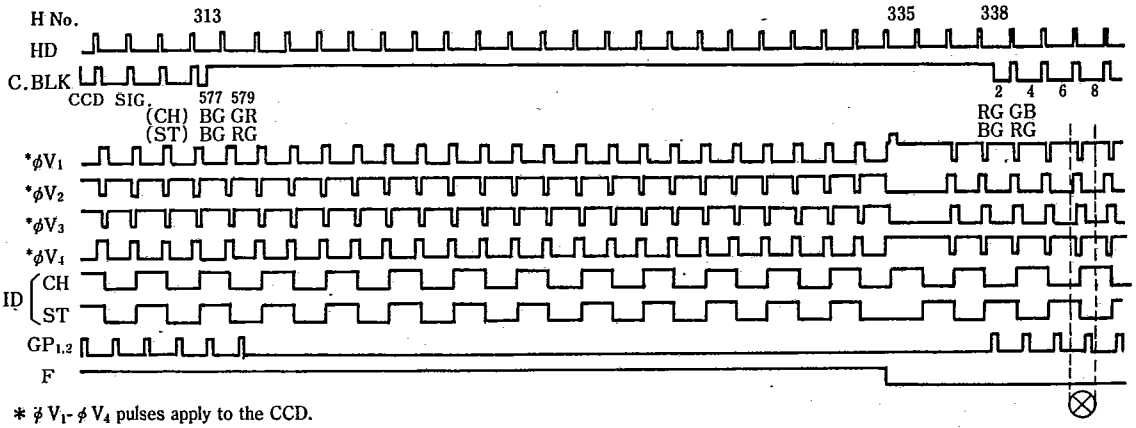
• PAL (2nd and 4th Field)



* φV1-φV4 pulses apply to the CCD.

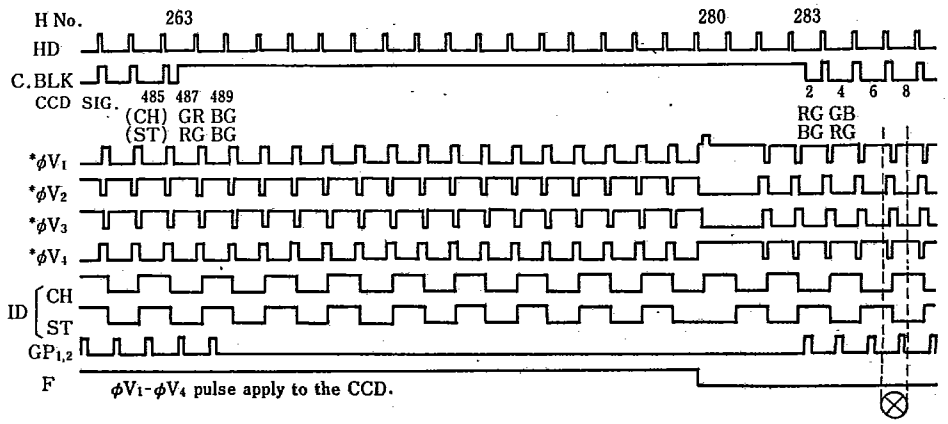
(4) Frame transfer

• NTSC (Even field)



* φV1-φV4 pulses apply to the CCD.

• PAL (1st and 3rd Field)



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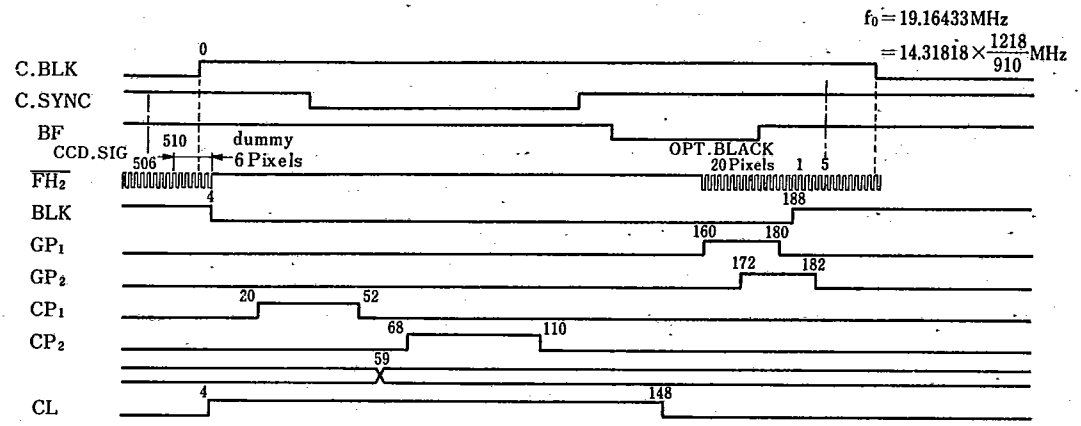
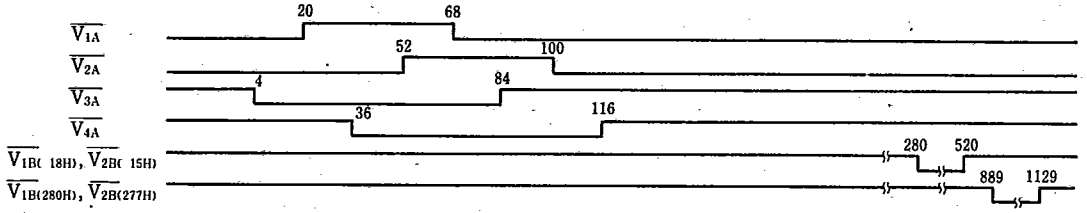
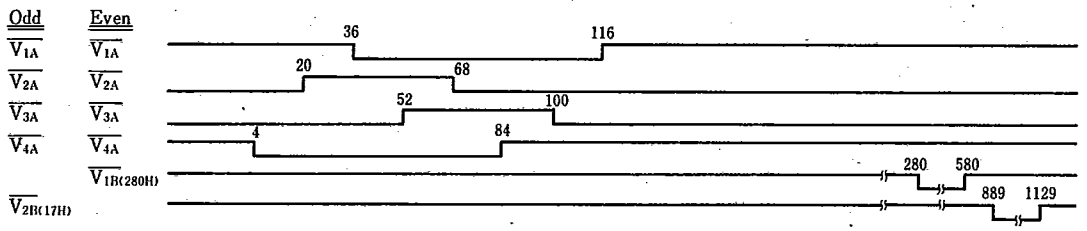
• NTSC (Sharp LR3740N, Panasonic MN6064)



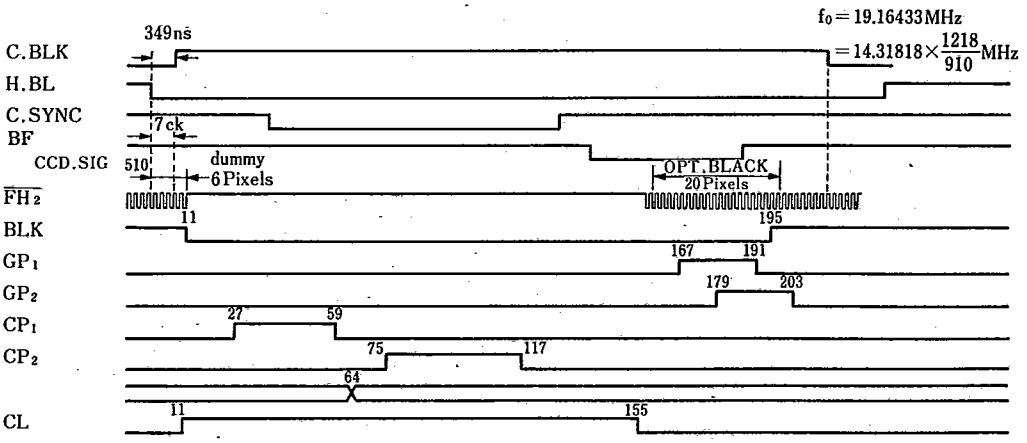
Field transfer (Enlarged timing of the area marked with ⊗)



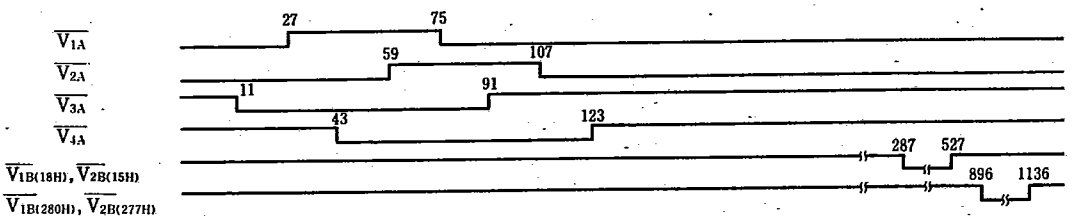
Frame transfer (Enlarged timing of the area marked with ⊗)



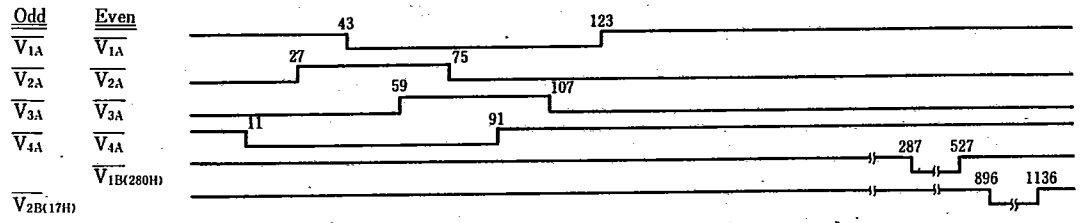
• NTSC (Sharp LR3740)



Field transfer

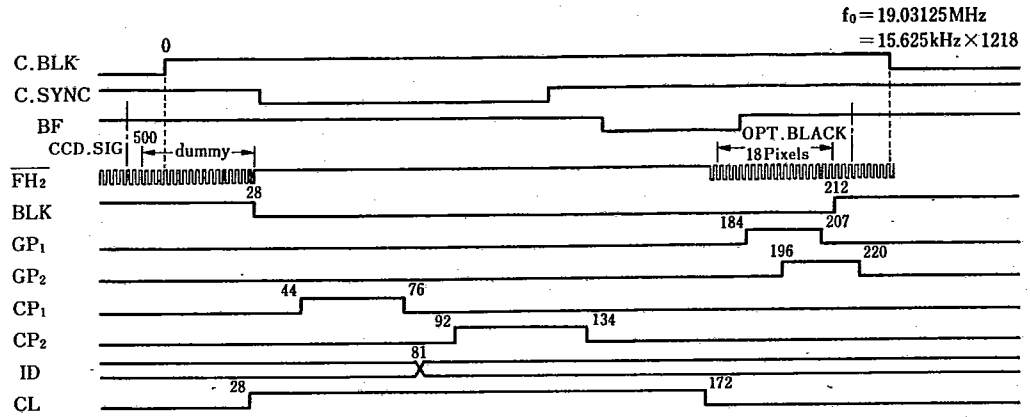


Frame transfer

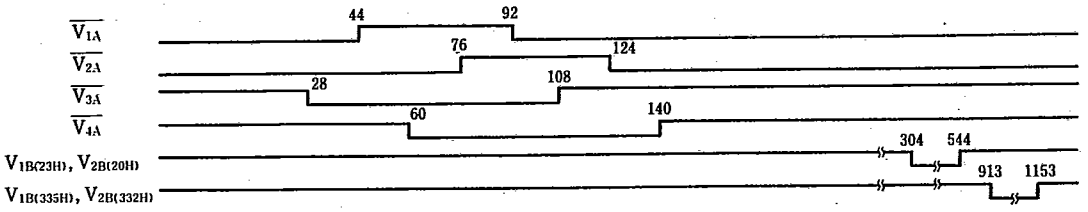


(5) PAL

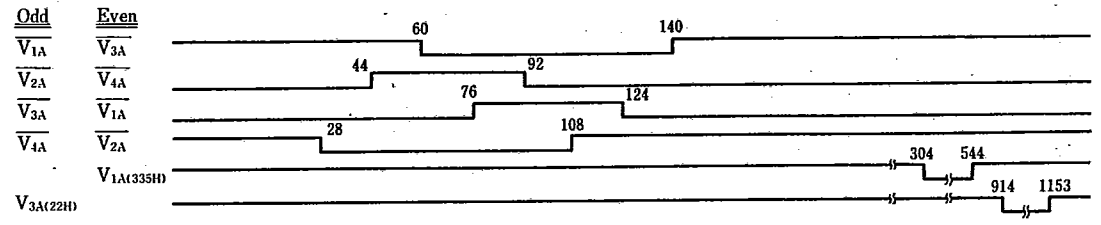
Panasonic MN6160B

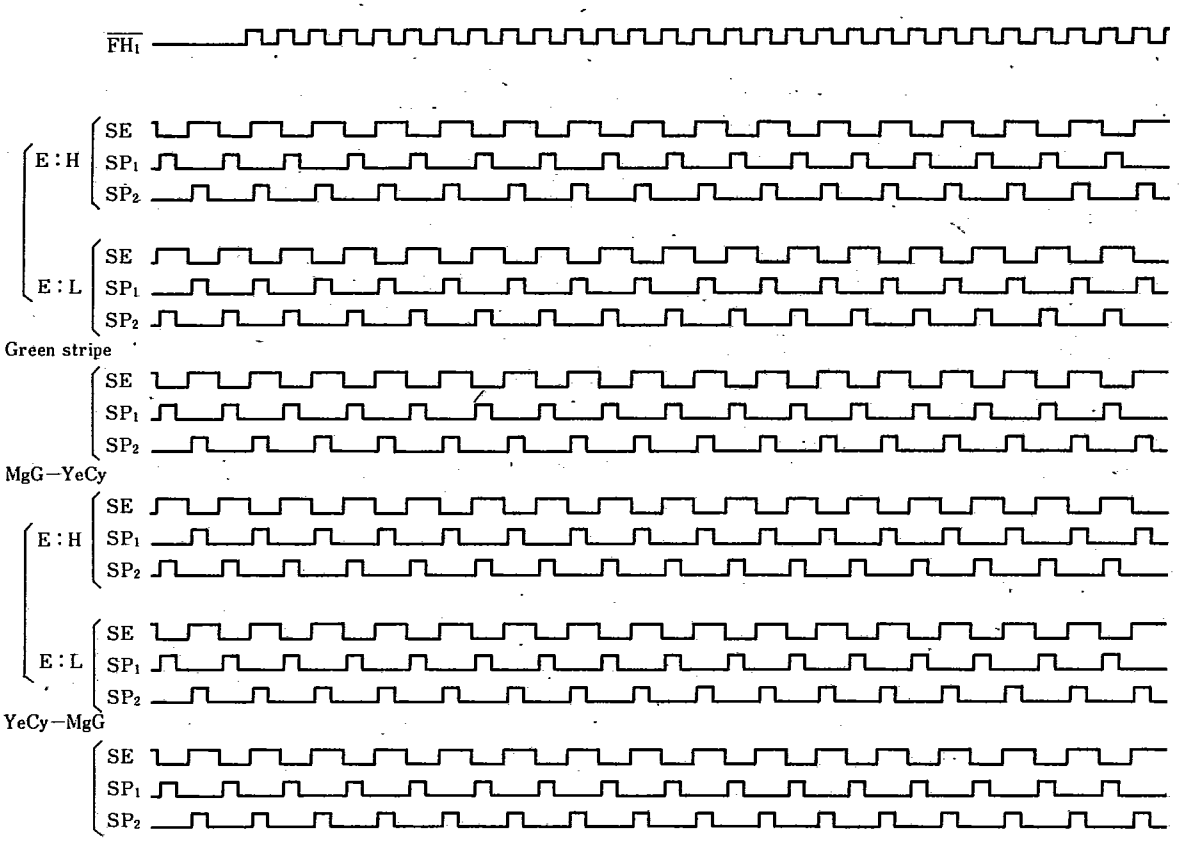


Field transfer

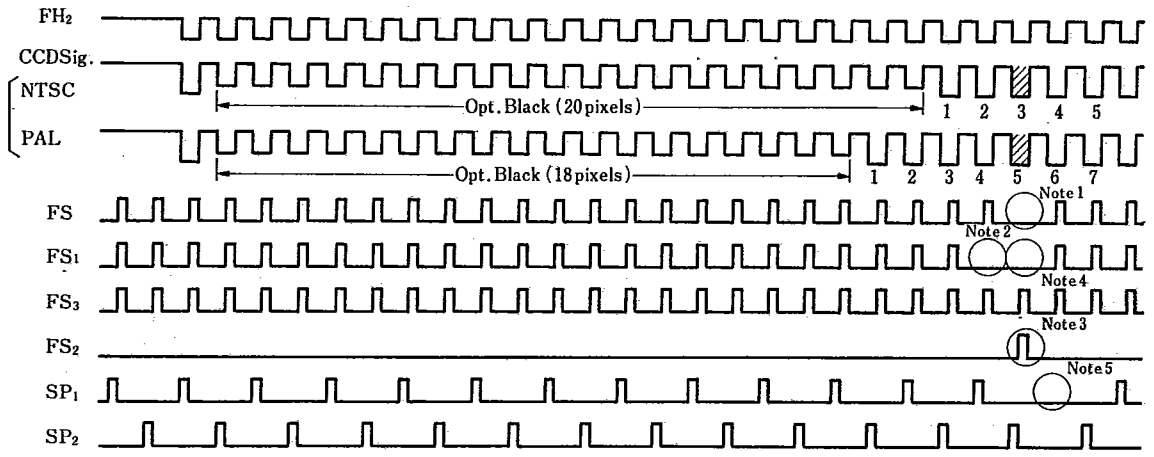


Frame transfer





Pulse output timing of FS, FS_1, FS_2, FS_3, SP_1 and SP_2 for defect compensation



The LZ92B31 defect compensation IC in combination with a ROM recorded with defect pixel addresses will output the following pulses.

Note 1 : The FS_1 will skip one pulse at the position where there is a signal of defective pixel.
Note 2 : The FS_1 will skip two pulses at the position where there are signals of a defective pixel and preceding by one pixel.
Note 3 : The FS_3 will generate one pulse at the position where there is a signal of defective pixel.
Note 4 : The FS_2 always outputs a consecutive pulse.
Note 5 : The SP_1 and SP_2 will skip one pulse at the position to sample and hold a signal of defective pixel.

Application Circuit Example