LZ93BE0

Timing Pulse Generator LSI for CCD

DESCRIPTION

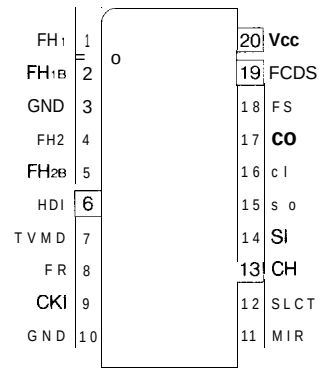
The LZ93BE0 is a CMOS timing generator LSI which provides horizontal transfer pulse, reset pulse, and sample-hold pulse used for separate camera, in combination with single-chip driver LSI (LZ95G55, LZ95G41) and timing LSI (LZ93F33, **LZ93F50, LZ93N61 or** LZ95D37/M).

FEATURES

- Switchable **between 270** 000 **pixels** CCD **and 320000 pixels CCD**
- Switchable **between NTSC** (EIA) **and PAL** (CCIR) **systems**
- **Single +5** V **power supply**
- Switchable **between normal and mirror-image**
- **Suitable for separate camera**
- **Package : 20-pin** MFP(MFP020-P)

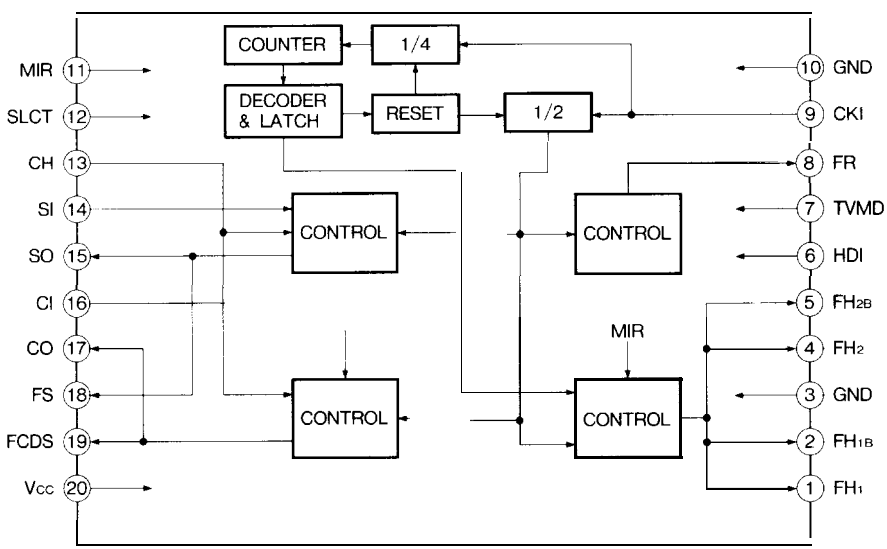
PIN CONNECTIONS

20-PIN MFP TOP VIEW



- **Designed for A-type and B-type CCD area sensors :**
  A-type CCD area sensor : LZ2314J, LZ2324J, LZ231 32, LZ23232
  B-type CCD area sensor : LZ2414J, LZ2424J, LZ2313H5, LZ2323H5, LZ2413, LZ2423

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	Vcc	– 0.3 to 7.0	v
Input voltage	VI	–0,3 to Vcc + 0.3	v
Output voltage	Vo	-0.3 to Vcc + 0.3	v
Operation temperature	Topr	–20 to +70	‘c
Storaae temperature	Tstq	–55 to +150	“c

DC CHARACTERISTICS

(Vcc = +5 V ± 5% Ta=–20 to +70°C)

PRAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Low voltage	V_{IL}				1.5	v	1
Input High voltage	V_{IH}		3.5			v	
Input High threshold voltage	V_{T+}	Schmitt Buffer	2.2		3.8	v	2
Input Low threshold voltage	V_{T-}		1.0		2.4	v	
Hysteresis voltage	$V_{T+} - V_{T-}$		0.4			v	
Input Low current	$\lvert I_{IL1} \rvert$	V_I=0 v			1.0	μA	3
	$\lvert I_{IL2} \rvert$	VI=o v	8.0		60	μA	4
Input High current	$\lvert I_{IH} \rvert$	$V_I = V_{CC}$			1,0	μA	5
Output High voltage	$V_{OH}1$	$I_{OH} = -2$ mA	4.0			v	6
Output Low voltage	V_{OL1}	I_{OL} = 4 mA			0.4	v	
Output High voltage	V_{OH2}	$I_{OH} = -4$ mA	4.0			v	7
Output LOW voltage	V_{OL2}	I_{OL} = 8 mA			0.4	v	
Output High voltage	V_{OH3}	$I_{OH} = -6$ mA	4.0			v	8
Output Low voltage	V_{OL3}	I_{OL} = 12 mA			0.4	v	

NOTES :

1. Applied to inputs (IC, ICU).
2. Applied to input (ICS).
3. Applied to inputs (IC, ICS).
4. Applied to input (ICU).
5. Applied to inputs (IC, ICU, ICS)
6. Applied to output (0)
7. Applied to output (O8M)
8. Applied to output (012M)

PIN FUNCTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	FH_1	012M		Horizontal transfer pulse 1	A horizontal transfer pulse for CCD area sensor. Connect to ϕ_{H1} of CCD area sensor.
2	FH_{1B}	08M		Horizontal transfer pulse 1 B	A horizontal transfer pulse for CCD area sensor, Connect to ϕ_{H1B} of CCD area sensor. If the CCD area sensor which corresponds to Mirror mode is driven at Normal mode (MIR = L), its drive-pulse is the same phase as the pulse of FH_1 (pin 1), and it is the same phase as the pulse of FH2 (pin 4) at Mirror mode (MIR = H).
3	GND	–	–	Ground	A grounding pin.
4	FH2	012M		Horizontal transfer pulse 2	A horizontal transfer pulse for CCD area sensor. Connect to ϕ_{H2} of CCD area sensor,
5	FH_{2B}	08M		Horizontal transfer pulse 2B	A horizontal transfer pulse for CCD area sensor. Connect to ϕ_{H2B} of CCD area sensor. If the CCD area sensor which corresponds to Mirror mode is driven at Normal mode (MIR = L), its drive-pulse is the same phase as the pulse of FH2 (pin 4),and it is the same phase as the pulse of FH_1 (pin 1) at Mirror mode (MIR = H).
6	HDI	ICS	–	Horizontal reference pulse	Put in a horizontal reference pulse from SSG-LSI. Connect to HD terminal of SSG-LSI.
7	TVMD	ICU	–	TV mode select	An input-pin to select TV standards, L level : NTSC mode H level or open : PAL mode
8	FR	08M		Reset pulse	A reset pulse for CCD area sensor, Connect to ϕ_R of CCD area sensor through the DC offset circuit.
9	CKI	ICS		Clock input	An input pin for reference clock. The frequencies are as follows : At EIA mode : 19.06993 MHz (1212 fH) At CCIR mode : 19.31250 MHz (1 236 fH)
10	GND	–	–	Ground	A grounding pin.
11	MIR	ICU	–	Mirror mode select	An input pin to select Mirror mode or Normal mode. L level : Normal Drive mode H level or open : Mirror Drive mode
12	SLCT	ICU	–	CCD type select	An input pin to select the type of CCD area sensor. L level (A type) LZ2314J, LZ2314Z, LZ23t42, LZ2313A9, LZ23132 LZ2324J, LZ2324Z, LZ23242, LZ2323A9, LZ23232 H level or open (B type) LZ2314BK, LZ2414J, LZ2313B5, LZ2313H5, LZ2413 LZ2324BK, LZ2424J, LZ2323B5, LZ2323H5, LZ2423

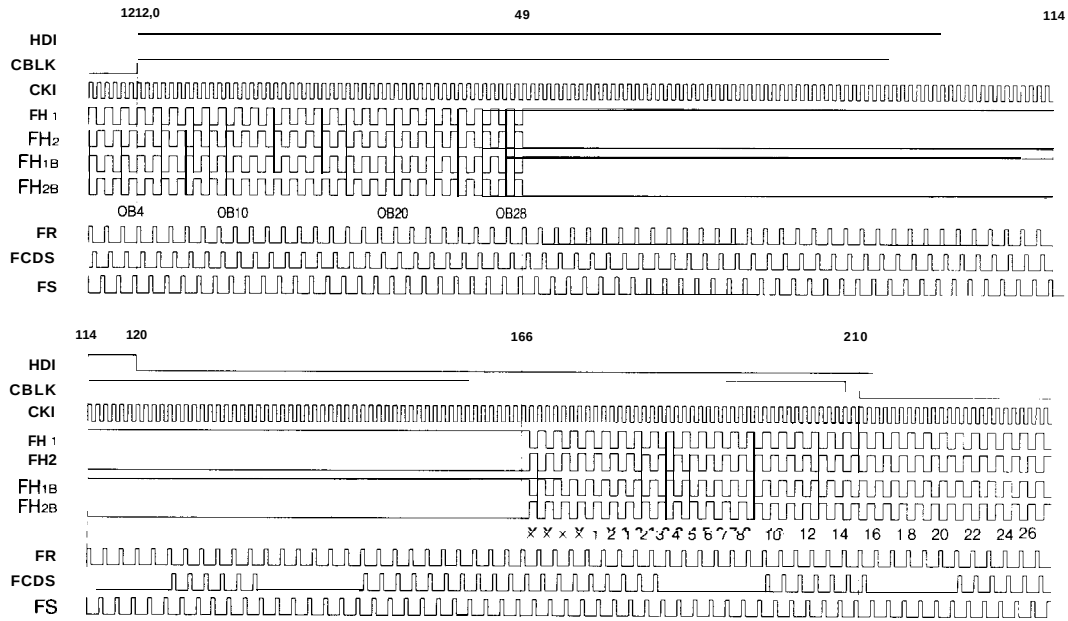
PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
13	CH	ICU	–	Phase control terminal for FCDS and FS	An input pin to select the phase of FCDS (pin 19) pulse and FS (pin 18) pulse. L level : adjustable H level or open : fixed
14	SI	IC	–	Phase-adjust input for FS	An input pin to control the phase of FS (pin 18). SO (pin 15) pulse put in this terminal after make it delay with resistor and capacitor.
15	so	o	⊓⊓	Phase-adjust output for FS	An output pin to control the phase of FS (pin 18). The output pulse put in SI (pin 14) after make it delay with resistor and capacitor.
18	cI	IC	–	Phase-adjust input for FCDS	An input pin to control the phase of FCDS (pin 19). CO (pin 17) pulse put in this terminal after make it delay with resistor and capacitor.
17	co	o	⊓⊓	Phase-adjust output for FCDS	An output pin to control the phase of FCDS (pin 19). The output pulse put in CI (pin 16) after make it delay with resistor and capacitor.
18	FS	o	⊓	Sample-hold pulse output	A pulse to sample-hold the signal from CCD area sensor. The phase of FS is fixed if CH (pin 13) equals H level and it can be adjustable if CH (pin 13) equals L level.
19	FCDS	o	n	CDS pulse output	A pulse to clamp the feed-through level form CCD area sensor. The phase of FCDS is fixed if CH (pin 13) equals H level and it can be adjustable if CH (pin 13) equals L level.
20	Vcc	–	–	Power supply	Supply +5 V power.

IC : Input pin (CMOS level input)
ICU : Input pin (CMOS level input with pull-up resistor)
ICS : Input pin (CMOS scnmitt input)
O, 08M, 012M : Output pin

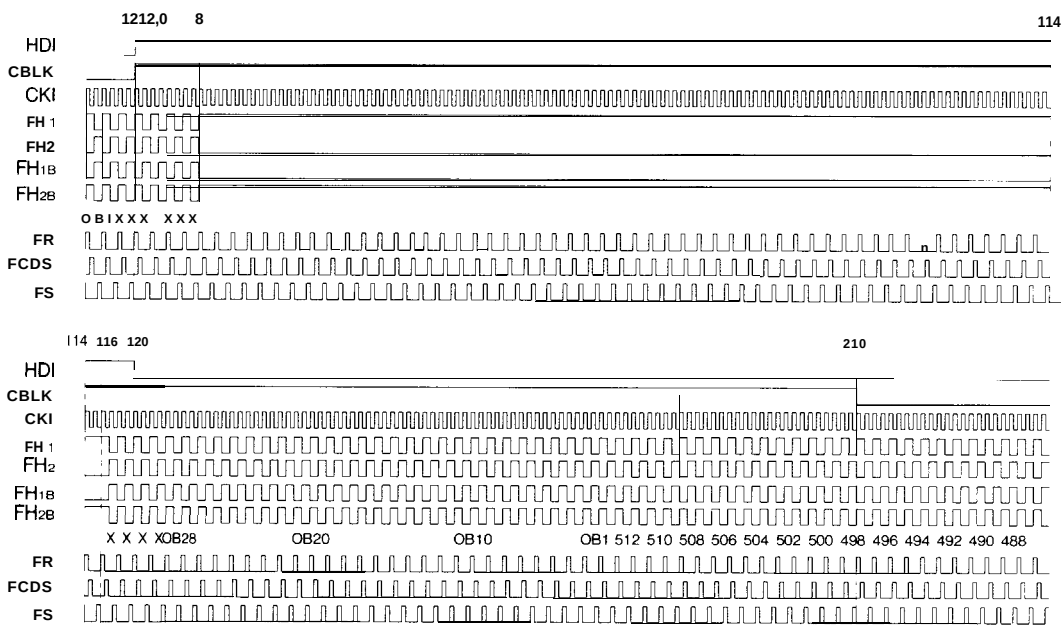
NOTE :
At the input pin, the rising edge of HDI (pin 6) is ± 20 ns shorter than that of CKI (pin 9).

TIMING DIAGRAM

NTSC(EIA) < A-TYPE, NORMAL MODE > 1 clock = 52.4 ns

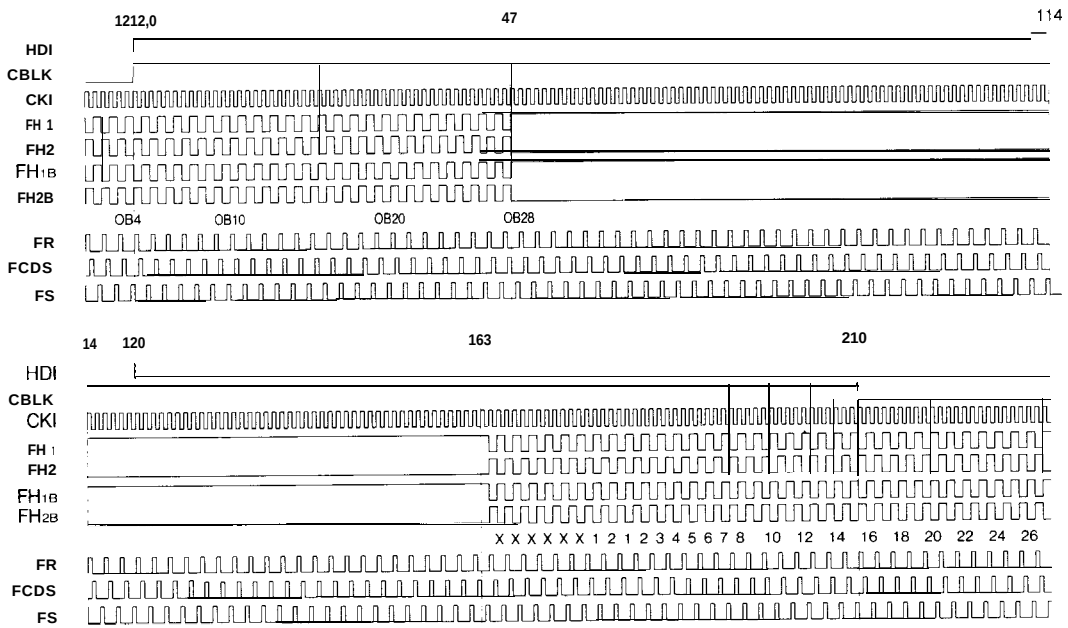


NTSC(EIA) < A-TYPE, MIRROR MODE > 1 clock = 52.4 ns



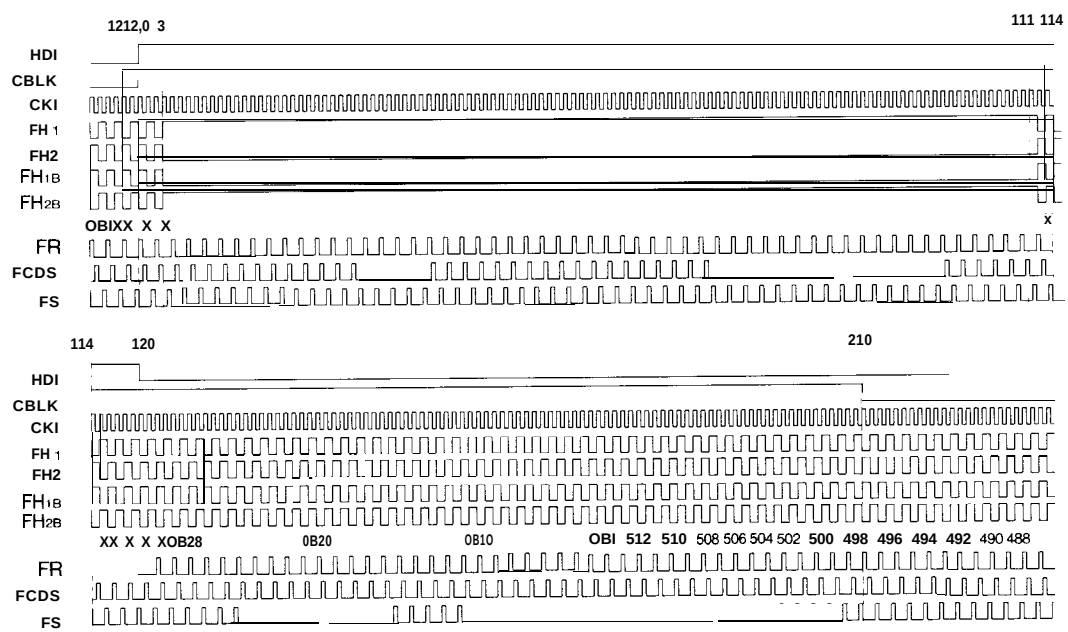
NTSC(EIA) < B-TYPE, NORMAL MODE >

1 clock= 52.4 ns



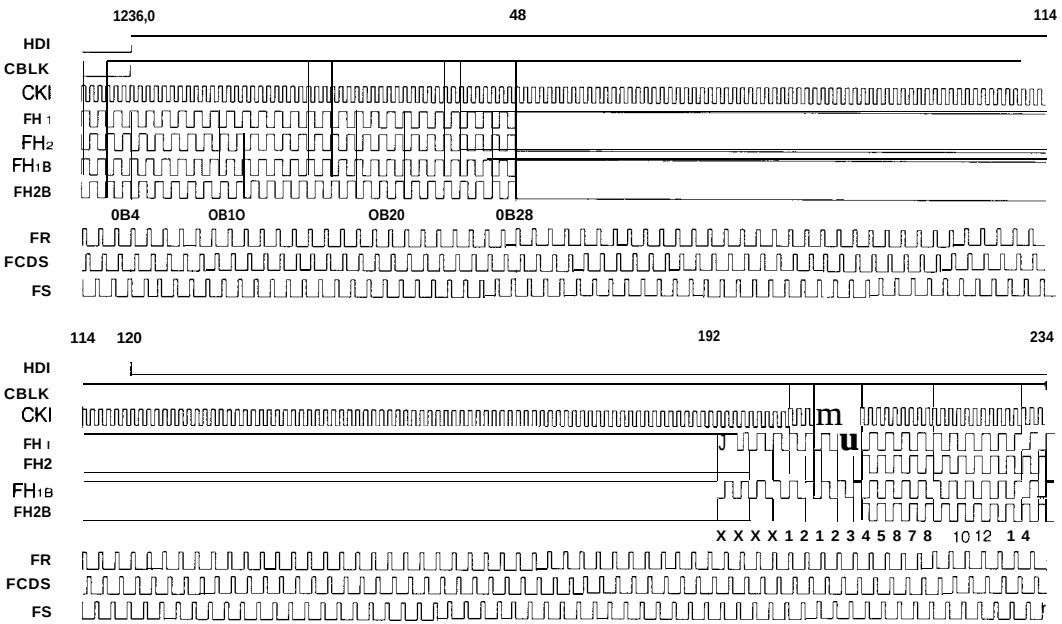
NTSC(EIA)< B-TYPE, MIRROR MODE >

1 clock =52.4 ns



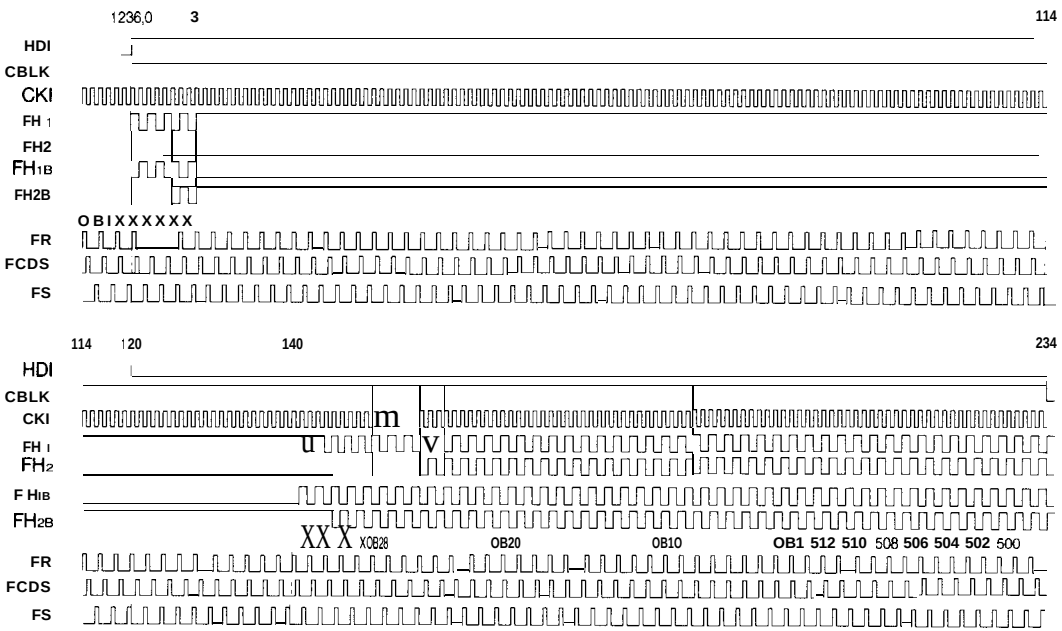
PAL(CCIR) < A-TYPE, NORMAL MODE >

1 clock = 51.8 ns



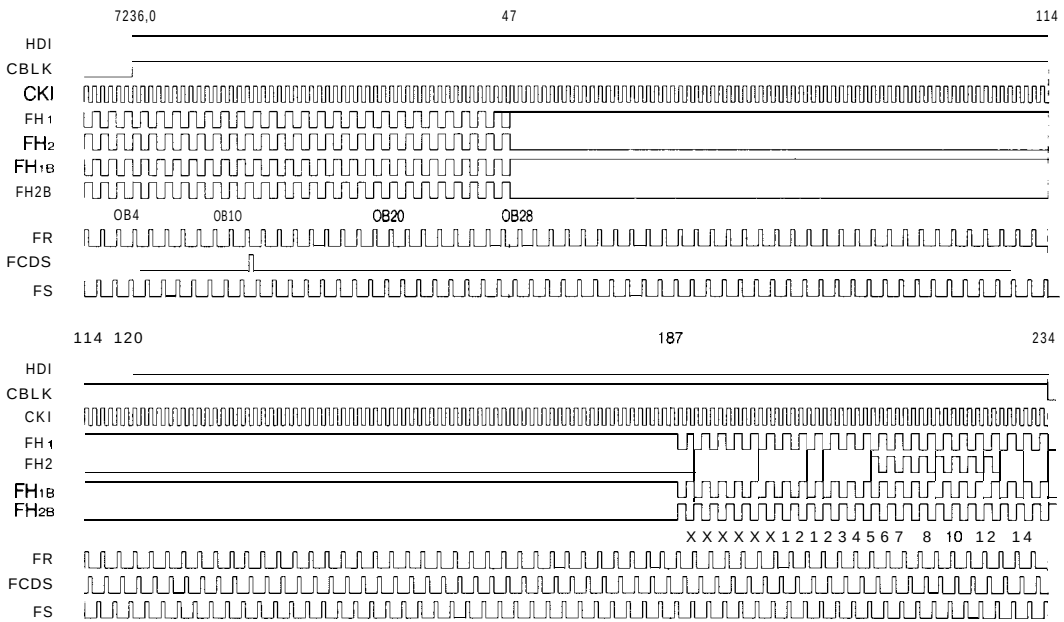
PAL(CCIR) < A-TYPE, MIRROR MODE >

1 clock = 51.8 ns



PAL(CCIR) < B-TYPE, NORMAL MODE >

1 clock = 51.8 ns



PAL(CCIR) < B-TYPE, MIRROR MODE >

1 clock = 51.8 ns

LZ93F33

Timing Pulse Generator LSI for CCD

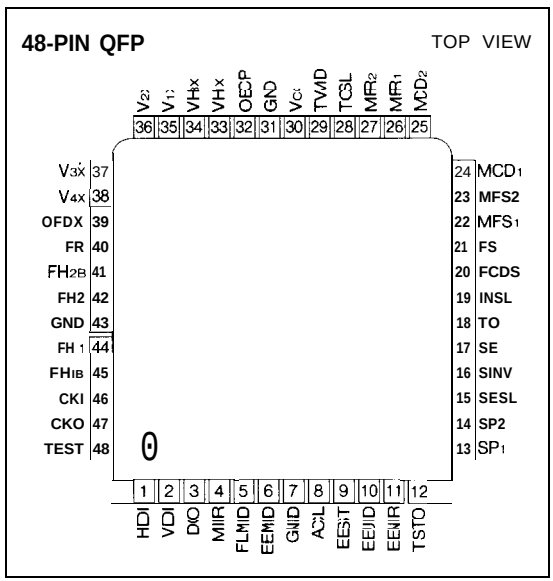
DESCRIPTION

The LZ93F33 is a CMOS timing generator LSI which provides timing pulses used to drive a CCD area sensor, in combination with the SSG LSI (LZ93N19 or LZ93B53).

FEATURES

- Switchable **between 270000 pixels CCD and 320000 pixels CCD**
- Switchable **between NTSC** (EIA) **and PAL** (CCIR) **systems**
- **Built-in EE (Electronic Exposure) control**
- **Flicker-less function**
- **Switchable between normal and mirror image**
- **Single +5 V power supply**
- **Package : 48-pin QFP(QFP048-P-101 O)**

PIN CONNECTIONS



BLOCK DIAGRAM