LZ93N19

Synchronous Signal Generator for CCD

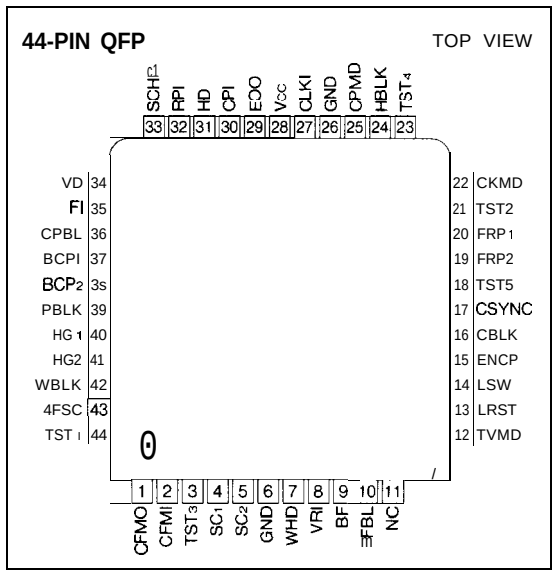
DESCRIPTION

The LZ93N19 is a CMOS synchronous signal generator LSI which provides TV synchronous pulses and video signal processing pulses, in combination with the timing signal generator LSI (LZ93N61, LZ93F50, LZ93F33 or LZ95D37/M).

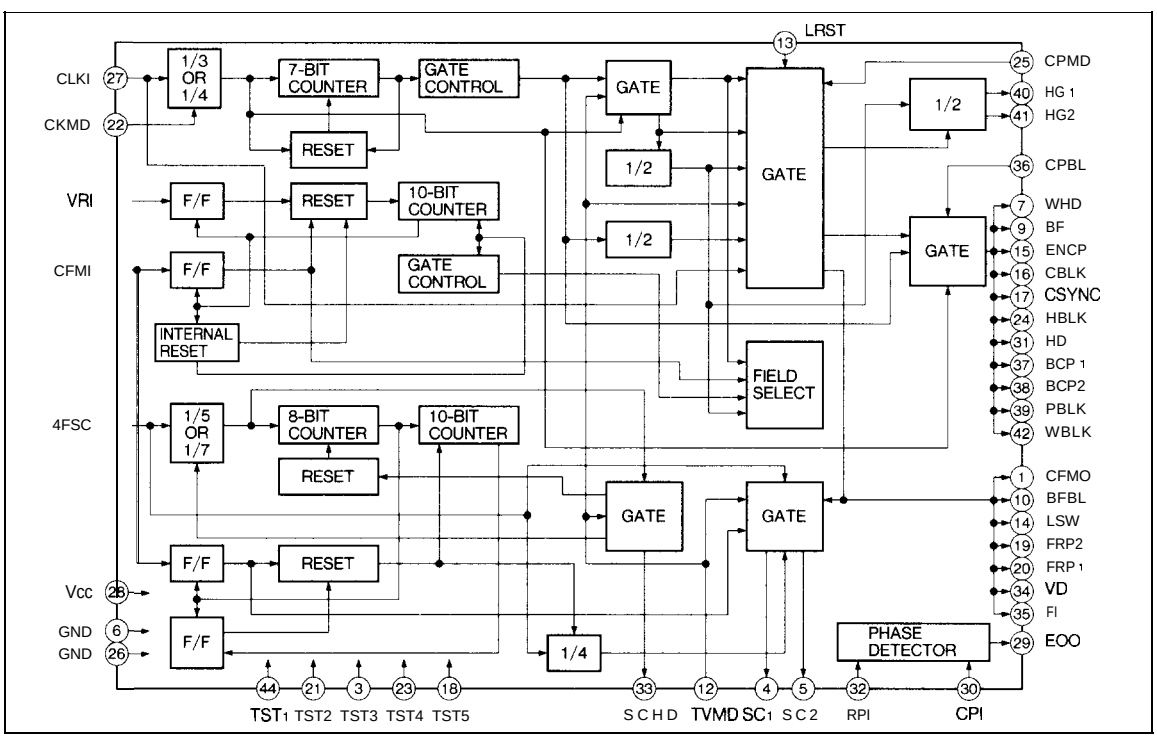
FEATURES

- Switchable **between 270000 pixels CCD and 320000 pixels CCD**
- Switchable **between NTSC** (EIA) **and PAL** (CCIR) **systems**
- **Single +5 V power supply**
- **External synchronization is possible**
- **Package : 44-pin QFP(QFP044-P-101 O)**

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	Vcc	-0.3 to 7.0	V
Input voltage	VI	-0,3 to Vcc + 0.3	V
Output voltage	Vo	-0.3 to Vcc + 0.3	V
Operating temperature	Topr	-20 to +70	°C
Storage temperature	Tstr	-55 to +150	°C

DC CHARACTERISTICS

(Vcc = 5 V ± 10%, Ta = -10 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Low voltage	V_{IL}				1.5	V	1
Input High voltage	V_{IH}		3.5			V	
Input High threshold voltage	V_{T+}				Vcc -0.8	V	2
Input Low threshold voltage	V_{T-}		0.9			V	
Hysteresis voltage	$V_{T+}-V_{T-}$		0.8			V	
Output Low voltage	V_{OL}	I_{OL} = 4 mA			0.4	V	3
Output High voltage	V_{OH}	I_{OH} = -2 mA	4.0			V	
Input Low current	$\lvert I_{IL1} \rvert$	VI=0 V			1,0	μA	4
	$\lvert I_{IL2} \rvert$	VI=0 V	8.0		60	μA	5
Input High current	$\lvert I_{IH1} \rvert$	VI= Vcc			1,0	μA	6
	$\lvert I_{IH2} \rvert$	VI=Vcc	8.0		60	μA	7
Leak Output current	$\lvert I_{OZ} \rvert$	High-Z			1.0	μA	8

NOTES :

1. Applied to all inputs except for VRI.
2. Applied to input (VRI).
3. Applied to all outputs.
4. Applied to all inputs except for VRI, LRST.
5. Applied to Inputs (VRI, LRST).
6. Applied to all inputs except for TST 1, TST2, TST3 TST4, TST5
7. Applied to inputs (TST 1, TST2, TST3, TST4, TST5).
8. Applied to output (EOO).

PIN FUNCTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	CFMO	O	n	bier frame output	A pulse to control color frame; occurs at every 4 fields in NTSC rode, recurs at every 8 fields in PAL mode.
2	CFMI	IC	n	Color frame input	An input pin for color frame signal. Connect to CFMO (pin 1) in Internal Synchronous mode. Connect to external color frame signal in External Synchronous mode. Connect to L level when 4FSC (pin 43) is set to L level.
3	TST3	ICD	–	Test terminal 3	A pin for tests, Set open or to L level in the Normal mode.
4	Scl	O	⎍⎍	Subcarrier output 1	An output pin for color subcarrier. The frequency of the signal is 1/4 the 4FSC frequency (pin 43). The signal is reset by color frame pulse CFMI (pin 2).
5	SC2	o	⎍⎍	Subcarrier output 2	An output pin for color subcarrier. When the phase of SC I (pin 4) is 180 degree, the phase of SC2 is 90 degree in NTSC mode in PAL mode, the phase of SC2 is 90 degree when LSW (pin 14) is Low and 270 degree when LSW is High.
6	GND	–	–	Grouding	A grouding pin.
7	WHD	O	⎍	Wide Horizontal drive output	An output pin for wide horizontal drive pulse. The pulse width is equal to that of PBLK (pin 39) and the repetition is horizontal frequency.
8	VRI	ICSU	V	Vertical reset	An input pin for resetting internal vertical counter. The input pulse is necessary 1/2 horizontal max. delay from vertical synchronous start point, because VRI is counted by 2 times horizontal frequency. Set open or to H level when not resetting.
9	BF	O	⎍	Burst flag	A pulse to define burst period.
10	BFBL	o	n	Burst flag blanking	At NTSC mode : holds H level. At PAL mode : stays at L level during the blanking period of BF (pin 9) otherwise, stays at H level.
11	NC	–	–	Non connection	A pin for no use.
12	TVMD	IC	–	TV mode	An input pin to select TV standards. At NTSC mode : L level At PAL mode : H level
13	LRST	ICU	u	Line switch reset	The input resets the output from LSW (pin 14). Set open or to H level when not used.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
14	LSW	o	⎍⎍	Line switch	The signal switches between H and L at every line. It is set at Low level at the 1st line of the 1st field.
15	ENCP	o	n	Encoder DC clamp	A clamp pulse that is used for recovering DC level. The repetition is horizontal frequency.
16	CBLK	o	⎍	Composite blanking pulse	Composite blanking pulses. In NTSC mode; H : 11.01 μs, V : 20 H period In PAL mode ; H : 12.12 μs, V : 25 H period
17	CSYNC	o	V	Composite synchronous signal	A composite synchronous signal.
18	TST5	ICD	–	Test terminal 5	A pin for to tests. Set open or to L level in the Normal mode.
19	FRP2	o	n	Frame read pulse 2	A clock output that is used for VTR servo. The pulse occurs at even fields and its repetition is frame period.
20	FRPI	o	⎍	Frame read pulse 1	A clock output that is used for VTR servo. The pulse occurs at odd fields and its repetition is frame period.
21	TST2	ICD	–	Test terminal 2	A pin for to tests. Set open or to L level in the Normal mode.
22	CKMD	IC	–	Clock mode select	A pin to select the factor of frequeny divisions, Division | 1/3 | 1/4 CKMD | LOW | HIGH Set to L level for LZ21 13, LZ2114, LZ2123, LZ2124, U2313, LZ2314, LZ2323 or LZ2324.
23	TST4	ICD	–	Test terminal 4	A pin for to tests. Set open or to L level in the Normal mode.
24	HBLK	o	⎍	Horizontal blanking pulse	A pulse that corresponds to the cease period of the horizontal transfer pulse.
25	CPMD	IC	–	Clamp Pulse mode seldct	An input pin to stop or continue BCP 1 (pin 37) and BCP2 (pin 38) pulses within the vertical blanking period. L level : continuous output. H level : becomes Low level during the absence of effective pixels within V blanking period.
26	GND	–	–	Grounding	A grounding pin.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
27	CLKI	IC		Main clock	An input pin for reference clock, Connect to DOUT (pin 3) of timing LSI (LZ93N61) or DO (pin 3) of timing LSI; following frequencies appear on this pin; At NTSC mode : 9.534964 MHz when CKMD = L level 12.713285 MHz when CKMD = H level At PAL mode : 9.656250 MHz when CKMD = L level 12.875000 MHz when CKMD = H level
28	Vcc	–	–	Power supply	Supply +5 V power.
29	EOO	TO	–	Phase comparator output	Phase comparator output for input signals RPI (pin 32) and CPI (pin 30). When CPI is advanced, output is Low level. When CPI is delayed, output is High level, When phases are equal, the terminal impedance is High.
30	CPI	IC	–	Horizontal comparison input	An input pin for comparison horizontal signal to the phase comparator. Connect to SCHD (pin 33) when comparator is used. Set to L level when comparator is not used.
31	HD	o		Horizontal drive pulse	The pulse occurs at the start of lines. Connect to timing LSI.
32	RPI	IC		Horizontal reference input	An input pin for the reference horizontal signal to the phase comparator. Connect to HD (pin 31) when comparator is used, Set to L level when comparator is not used.
33	SCHD	0		Subcarrier HD	A horizontal synchronization pulse obtained by dividing 4FSC (pin 43). At NTSC mode : dividing into 1 /91 O 4FSC. At PAL mode : dividing into 1/1 135 4FSC ordinarily and dividing into 1/1 137 4FSC during one horizontal period within the V blanking,
34	VD	0		V drive pulse	The pulse occurs at the start of every field. Connect to VDI (pin 2) of timing LSI (LZ93N61) or VDI (Pin 1) of timing LSI (LZ92E62).
35	FI	o		Filed index	The pulse is used for detecting field. At NTSC mode : 1st field; LOW 2nd field; HIGH At PAL mode : 1st and 3rd field; LOW 2nd and 4th field; HIGH
36	CPBL	IC		Blanking clamp pulse	When the input is High, BCPI (pin 37) and BCP2 (pin 36) are Low.

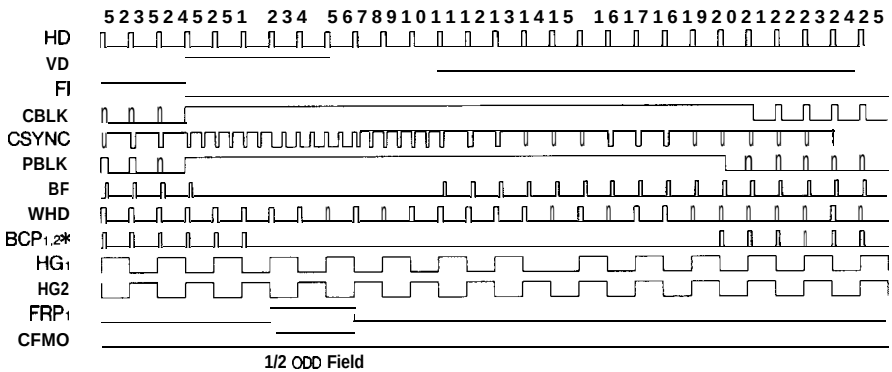
PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
37	BCP1	O	n	Optical black clamp pulse 1	A pulse to clamp the optical black signal. This pulse is continuous at horizontal cycle when CPMD (pin 25) and CPBL (pin 36) are Low. When CPMD is High and CPBL is Low, output stays Low during the absence of effective pixels within the Vertical blanking, otherwise is continuous at horizontal cycle.
38	BCP2	O	n	Optical black clamp pulse 2	BCP2 is the same as BCPI (pin 37) except that BCP2 is delayed by 900 ns from BCP 1.
39	PBLK	O	n	Pre-blanking pulse output	Equivalent to CBLK (pin 16) pulse except for shorter pulse width with cut-off trailing edge.
40	HG1	O	⎍⎍	Line index pulse 1	The pulse is used in color separator. The signal switches H and L at every line. It resets at the 14th line when in NTSC, and at the 9th line when in PAL mode.
41	HG2	O	⎍⎍	Line index pulse 2	The pulse is used in color separator. The signal switches H and L at every line. It resets at the 277th line when in NTSC, and at the 322th line when in PAL mode.
42	WBLK	O	⎍	Wide blanking pulse	Equivalent to CBLK (pin 16) except that its pulse width is wider than that of CBLK.
43	4FSC	IC	⎍⎍	4FSC input	An input pin for the signal 4 times the color subcarrier frequeny. At NTSC mode : 14,318180 MHz At PAL mode : 17.734475 MHz Connect to L level, when SC1 (pin 4) and SC2 (pin 5) signals are not required.
44	TST1	ICD	–	Test terminal 1	A pin for tests. Set open or to L level in the Normal mode.

IC : Input pin (CMOS level).
ICU : Input pin (CMOS level with pull-up resistor).
ICD : Input pin (CMOS level with pull-down resistor).
ICSU : Schmitt-trigger Input pin (CMOS level with pull-up resistor)
O : Output pin.
TO : Tri-state output pin.

TIMING DAIGRAM

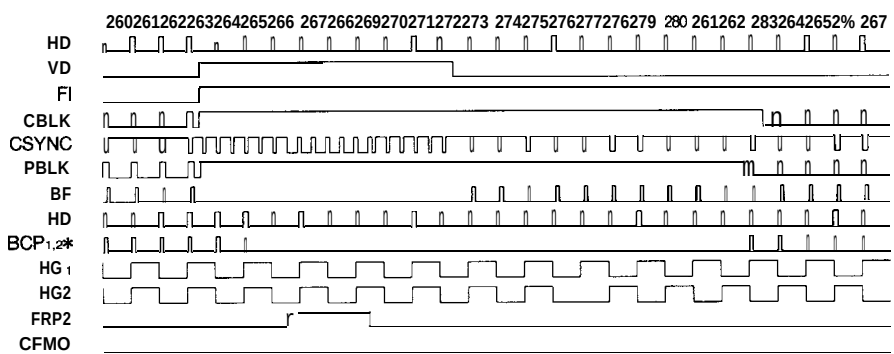
VERTICAL TIMING < NTSC >

(ODD FIELD)



* CPMD = H

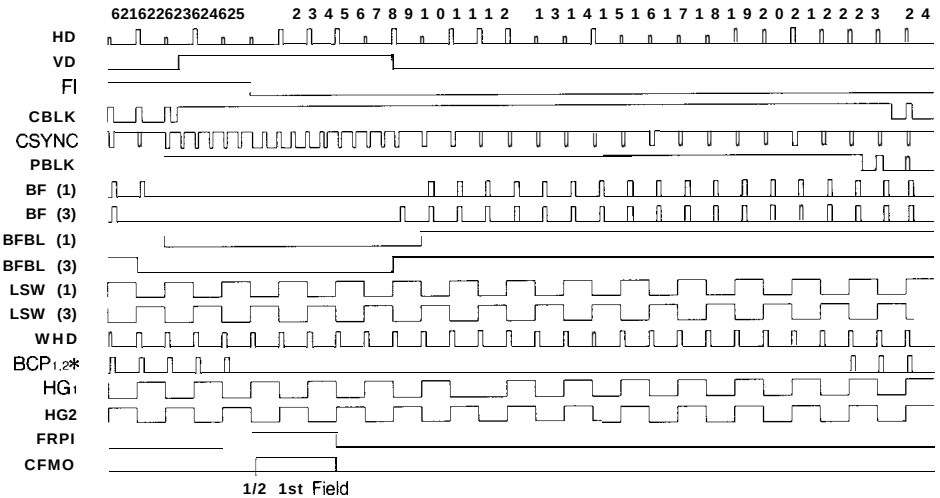
(EVEN FIELD)



* CPMD = H

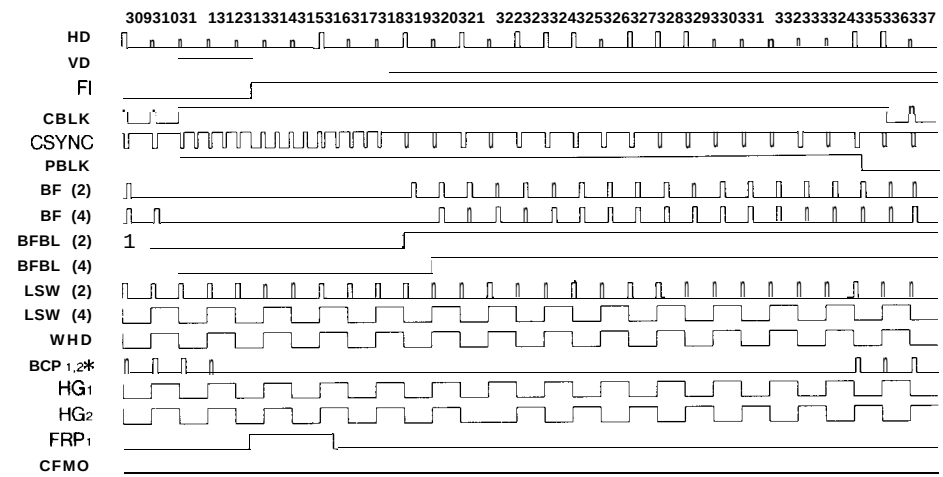
VERTICAL TIMING < PAL >

(1st, 3rd FIELD)



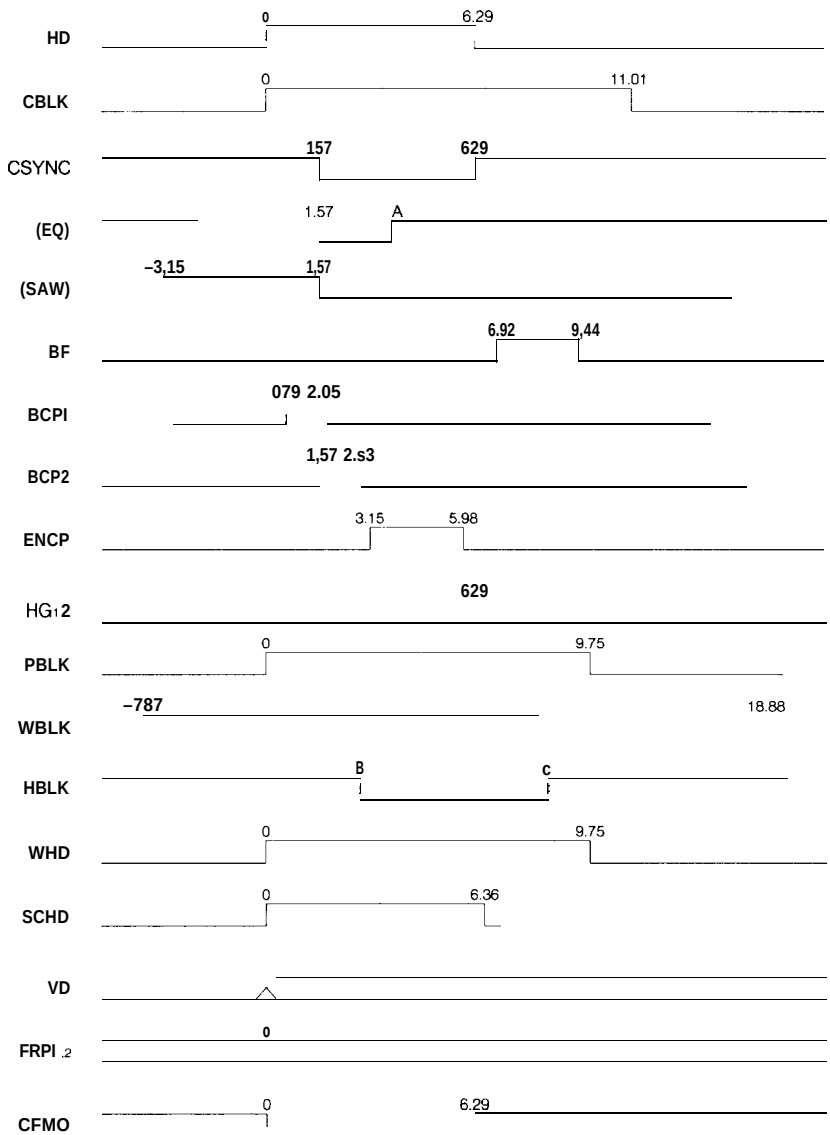
* CPMD = H

(2nd, 4th FIELD)



* CPMD = H

HORIZONTAL TIMING < NTSC > Unit : μs

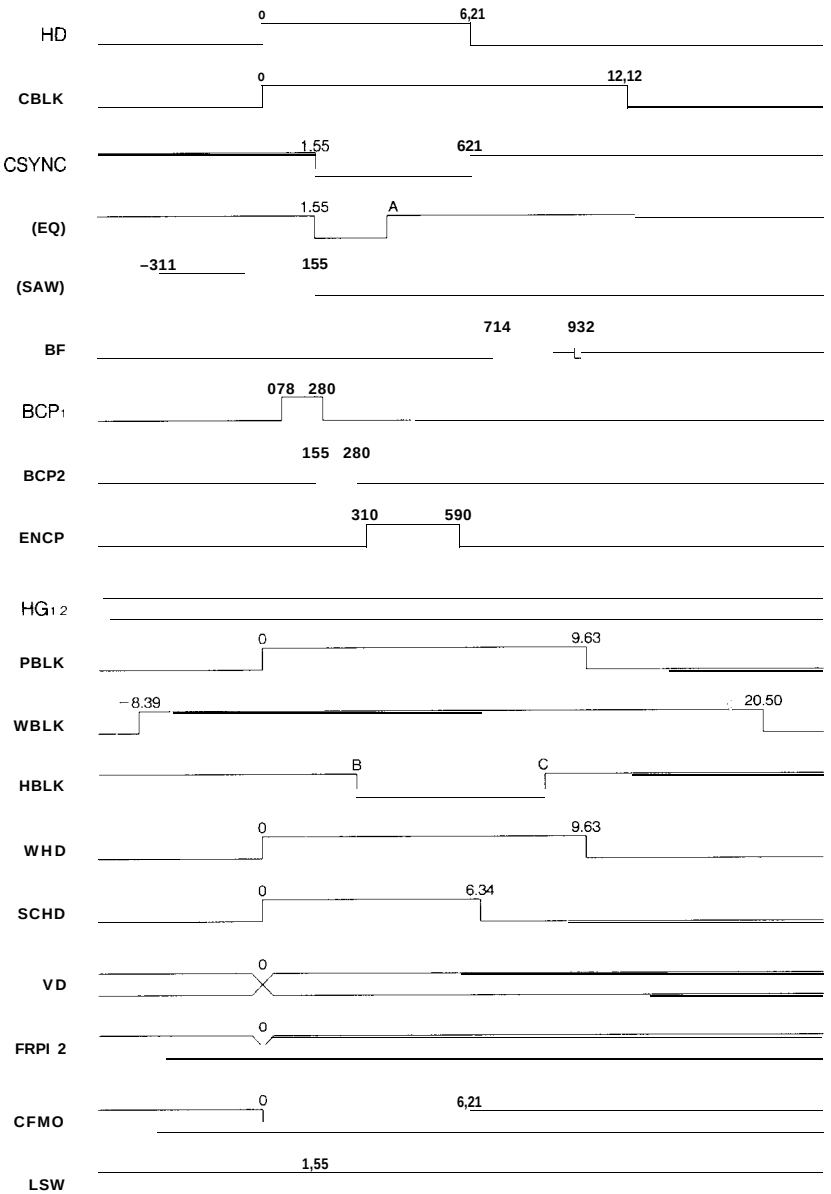


NOTES :

- **Applied to the CCD of 542 horizontal pixels** (CKMD = **L) A = 2.31** μs, **B = 2.94** μs, **C** = 8.60 μs
- **. Applied to the CCD of 762 horizontal pixels** (CKMD = **H) A =2.36** μs, **B = 2.91** μs, C = 8.57 μs

HORIZONTAL TIMING < PAL >

Unit : μS



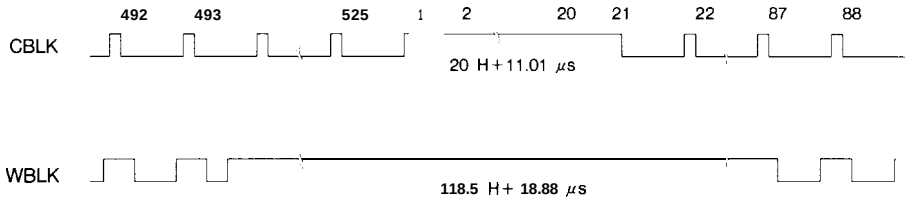
NOTES :

- Applied to the CCD of 542 horizontal pixels (CKMD = L) A = 2.28 μS, B = 2.90 μS, C = 9.73 μS
- Applied to the CCD of 762 horizontal pixels (CKMD = H) A=2.33 μS, B = 2.87 μS, C = 9.70 μS

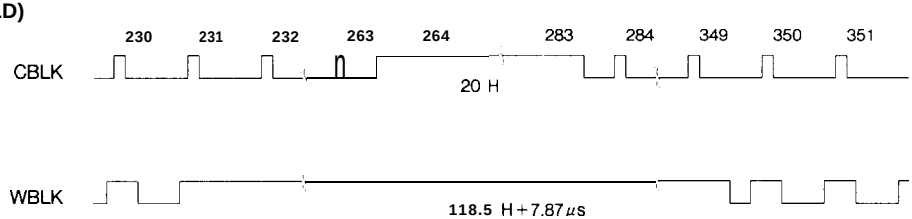
"WBLK", "CBLK" TIMING < NTSC >

Unit : μs

(ODD FIELD)

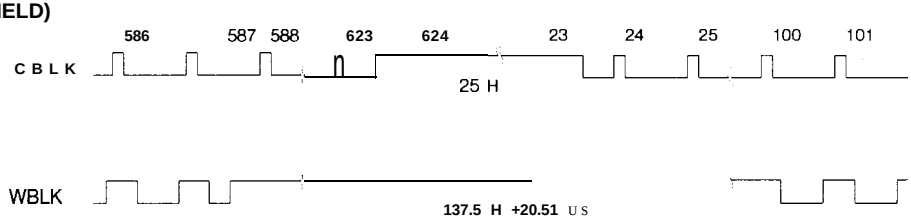


(EVEN FIELD)



"WBLK", "CBLK" TIMING < PAL >

(1st, 3rd FIELD)



(2nd, 4th FIELD)