SHARP

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TECHNICAL LITERATURE

FOR

Control IC for

TFT-LCD module

Model No. LZ9FC22

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1. Introduction

This data sheet is to introduce the specification of **LZ9FC22** , timing Control IC for TFT - LCD module.

Applicable TFT-LCD module : QVGA(Portrate / Landscape) pixel type module

Functions: Timing Control IC for TFT-LCD module

(1)By inputting Clock signal, Horizontal sync. signal, Vertical sync. signal, the following signals Synchronized with above signal are generated;

(A)Driving signal for source driver :CLK,SPL,SPR,LP,PS

(B)Driving signal for gate driver :CLS,SPS

(C)Signal for common electrode driving signal preparation :REV

(B)Signal for standard voltage preparation :REVV0

(2)Horizontal and Vertical reverse scanning function

Input/Output signal timing chart for above cases : See Fig.1. Fig.2. Fig.3.

Outline dimensions : See Fig.4.

2. Feature

Process	:	CMOS
Wafer substrate	:	P-type silicon substrate
Package	:	72QFP(0.5mm pin pitch)
Operating Temperature	:	-30℃ ~ +85℃
Propagation delay time	:	1ns/gate (Condition : V_{DD}=3.3V, Topr=25℃)

*REMARK

Not designed or rated as radiation harded

3. Pin assignment

Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	IC	DCLK	37	O3M	CLK
2	ICU	SETR	38	-	GND
3	IC	R0	39	O2M	OB5
4	IC	R1	40	O2M	OB4
5	IC	R2	41	O2M	OB3
6	IC	R3	42	O2M	OB2
7	IC	R4	43	O2M	OB1
8	IC	R5	44	O2M	OB0
9	-	GND	45	-	VDD
10	-	N.C.	46	-	GND
11	IC	G0	47	O2M	OG5
12	IC	G1	48	O2M	OG4
13	IC	G2	49	O2M	OG3
14	IC	G3	50	O2M	OG2
15	IC	G4	51	O2M	OG1
16	IC	G5	52	O2M	OG0
17	ICU	TEST	53	-	GND
18	IC	B0	54	O2M	OR5
19	IC	B1	55	O2M	OR4
20	IC	B2	56	O2M	OR3
21	IC	B3	57	O2M	OR2
22	IC	B4	58	O2M	OR1
23	IC	B5	59	O2M	OR0
24	ICU	TEST	60	-	GND
25	ICU	HREV	61	TO2M	CLS
26	ICD	ENAB	62	TO2M	SPS
27	-	VDD	63	-	VDD
28	-	GND	64	-	GND
29	ICU	TEST	65	TO2M	UBL
30	O2M	REV	66	ICU	VREV
31	O2M	REVV0	67	IC	TEST
32	O2M	PS	68	IC	SIZEC0
33	TO2M	SPR	69	O2M	MOD
34	O2M	LBR	70	ICU	REM
35	TO2M	SPL	71	IC	HS
36	O2M	LP	72	IC	VS

IC :Input buffer CMOS level

ICU :Input buffer CMOS level with PULL UP resistance

ICD :Input buffer CMOS level with PULL DOWN resistance

O2M :Output buffer IOL=0.8mA(VDD=3V)

TO2M :Tri-state Output buffer IOL=0.8mA(VDD=3V)

VDD :Power supply pin

GND :Earth pin

N.C. :Non Connection pin

4. **Explanation of input/Output signal**

Pin No	Signal Name	Explanation	I/O
1	DCLK	Input terminal for data clock signal	I
2	SETR	Input terminal for control signal for PS (SIZEC0 = "L" to the apploication)	I
3	R0	Input terminal for red data signal(LSB)	I
4	R1	Input terminal for red data signal	I
5	R2	Input terminal for red data signal	I
6	R3	Input terminal for red data signal	I
7	R4	Input terminal for red data signal	I
8	R5	Input terminal for red data signal(MSB)	I
9	GND	Ground	-
10	N.C.	Non connection	-
11	G0	Input terminal for green data signal(LSB)	I
12	G1	Input terminal for green data signal	I
13	G2	Input terminal for green data signal	I
14	G3	Input terminal for green data signal	I
15	G4	Input terminal for green data signal	I
16	G5	Input terminal for green data signal(MSB)	I
17	TEST	Input terminal for test normal state:H level	I
18	B0	Input terminal for blue data signal(LSB)	I
19	B1	Input terminal for blue data signal	I
20	B2	Input terminal for blue data signal	I
21	B3	Input terminal for blue data signal	I
22	B4	Input terminal for blue data signal	I
23	B5	Input terminal for blue data signal(MSB)	I
24	TEST	Input terminal for test (normal state:H level)	I
25	HREV	Input terminal for setting up right/left reverse scanning H level : Normal L level : Reverse scanning	I
26	ENAB	Input terminal for signal to settle the Horizontal display position	I
27	VDD	Input terminal for Power Supply voltage	-
28	GND	Input terminal for Ground	-
29	TEST	Input terminal for test (normal state:H level)	I
30	REV	Signal output for common electrode driving signal preparation	O
31	REVV0	Signal output for standard voltage preparation	O
32	PS	Control signal output for sourve driver	O
33	SPR	Start signal output for source driver (for right/left reverse scannning, normally high impedance)	O
34	LBR	Output signal for right/left reverse scannning HREV=H : H level output =L : L level output	O
35	SPL	Start signal output for source driver (for normal scanning. At right/left reverse scanning, high impedance)	O
36	LP	Data transferring signal output for source driver	O

Pin No	Signal Name	Explanation	I/O
37	CLK	Clock signal output for source driver	O
38	GND	Ground	-
39	OB5	Blue data signal output for source driver(MSB)	O
40	OB4	Blue data signal output for source driver	O
41	OB3	Blue data signal output for source driver	O
42	OB2	Blue data signal output for source driver	O
43	OB1	Blue data signal output for source driver	O
44	OB0	Blue data signal output for source driver(LSB)	O
45	VDD	Power Supply voltage	-
46	GND	Ground	-
47	OG5	Green data signal output for source driver(MSB)	O
48	OG4	Green data signal output for source driver	O
49	OG3	Green data signal output for source driver	O
50	OG2	Green data signal output for source driver	O
51	OG1	Green data signal output for source driver	O
52	OG0	Green data signal output for source driver(LSB)	O
53	GND	Ground	-
54	OR5	Red data signal output for source driver(MSB)	O
55	OR4	Red data signal output for source driver	O
56	OR3	Red data signal output for source driver	O
57	OR2	Red data signal output for source driver	O
58	OR1	Red data signal output for source driver	O
59	OR0	Red data signal output for source driver(LSB)	O
60	GND	Ground	-
61	CLS	Clock signal output for source driver	O
62	SPS	Start signal output for gate driver	O
63	VDD	Power Supply voltage	-
64	GND	Ground	-
65	UBL	Output signal for up/down reverse scanning VREV=H : H level output VREV=L : L level outuput	O
66	VREV	Input terminal for setting up up/down reverse scannning (H:Normal L:Reverse scanning)	O
67	TEST	Input terminal for test (normal state : L level)	I
68	SIZEC0	Input signal for drive condition change SIZEC0 = H : Portrate QVGA(240RGB x 320) = L : Landscape QVGA(320RGB x 240)	I
69	MOD	Output signal for gate driver	O
70	REM	Input terminal for reset signal (Give the signal that becomes H level fixation from the L level at the time of the power supply input)	I
71	HS	Input terminal for horizontal sync. signal	I
72	VS	Input terminal for vertical sync. Signal	I

5. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	-0.3 ~ 6.0	V
Input voltage	V_I	-0.3 ~ VDD+0.3	V
Output voltage	V_O	-0.3 ~ VDD+0.3	V
Operating temperature	Topr	-30 ~ +85	℃
Strage temperature	Tstg	-55 ~ +150	℃

6. Electrical Specifications

6-1.Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	2.7	3.3	3.6	V
Operating temperature	Topr	-30		+85	℃

6-2.Electrical Characteristics

(VDD=+2.7~+3.6V, Ta= -30 ~ +85℃)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit	*
Input "Low" voltage	V_{IL1}				$0.3\times V_{DD}$	V	1
Input "High" voltage	V_{IH1}		$0.7\times V_{DD}$			V	
Input" High "current	$\lvert I_{IH1} \rvert$	$V_I=V_{DD}$(V)			1.0	μA	2
Input "High" current	$\lvert I_{IH2} \rvert$	$V_I=V_{DD}$(V)	2.0		36.0	μA	3
Input "Low" current	$\lvert I_{IL1} \rvert$	V_I= 0 (V)			1.0	μA	4
Input "Low" current	$\lvert I_{IL2} \rvert$	V_I= 0 (V)	2.0		36.0	μA	5
Output "Low" voltage	V_{OL1}	I_{OL1}= 1.6 (mA)			0.4	V	6
Output "High" voltage	V_{OH1}	I_{OH1}= - 0.8 (mA)	V_{DD}-0.5			V	
Output "Low" voltage	V_{OL2}	I_{OL2}= 0.8 (mA)			0.4	V	7
Output "High" voltage	V_{OH2}	I_{OH2}= - 0.4 (mA)	V_{DD}-0.5			V	
Output Leakage current	$\lvert I_{OZ} \rvert$	High-impedance state			1.0	μA	8

*1 : Applied to Input pins (IC,ICU,ICD)

*2 : Applied to Input pins (IC,ICU)

*3 : Applied to Input pins (ICD)

*4 : Applied to Input pins (IC,ICD)

*5 : Applied to Input pins (ICU)

*6 : Applied to Output pins (O2M,TO2M)

*7 : Applied to Output pins (O2M, TO2M)

*8 : Applied to Output pins (TO2M)

7. Condition for signal input

(1) Portrate QVGA(240RGBx320) : SIZEC0 = H level

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	f_{DCLK}	4.5		6.8	MHz
HS frequency	f_{HS}	$f_{DCLK}/330$		$f_{DCLK}/254$	KHz
		15		26	KHz
VS frequency	f_{VS}	$f_{HS}/440$		$f_{HS}/332$	Hz
		50		80	Hz

(2) Landscape QVGA(320RGBx240) : SIZEC0 = L level

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	f_{DCLK}	4.5		6.8	MHz
HS frequency	f_{HS}	$f_{DCLK}/440$		$f_{DCLK}/334$	KHz
		12.5		20	KHz
VS frequency	f_{VS}	$f_{HS}/330$		$f_{HS}/248$	Hz
		50		82	Hz

1-1. Portrate type QVGA(240RGB x 320) (SIZEC0 = H level)

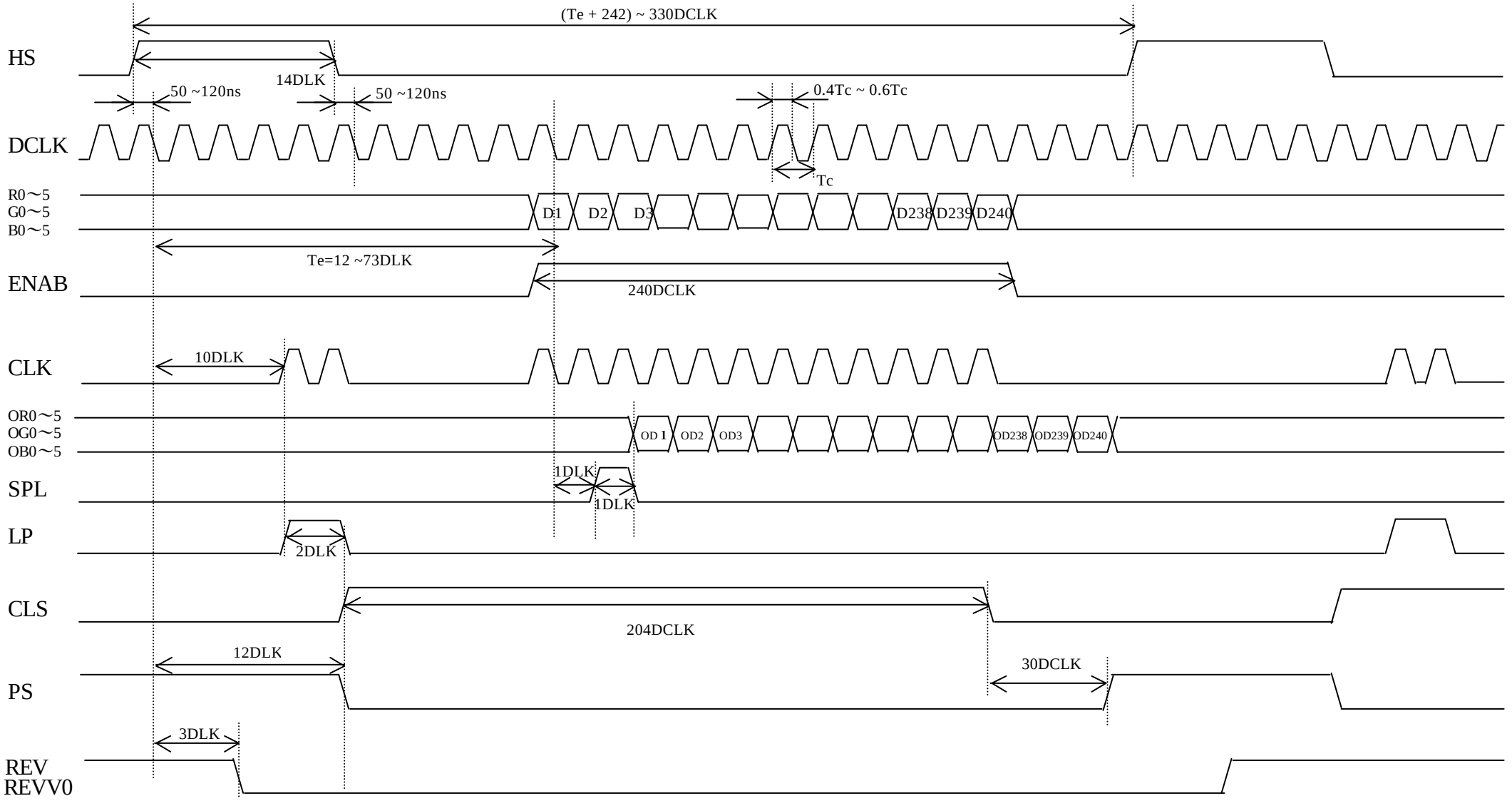

Fig.1-1 Horizontal counter timing chart-a (ENAB signal : valid)

1-2. Portrate type QVGA(240RGB x 320) (SIZEC0 = H level)

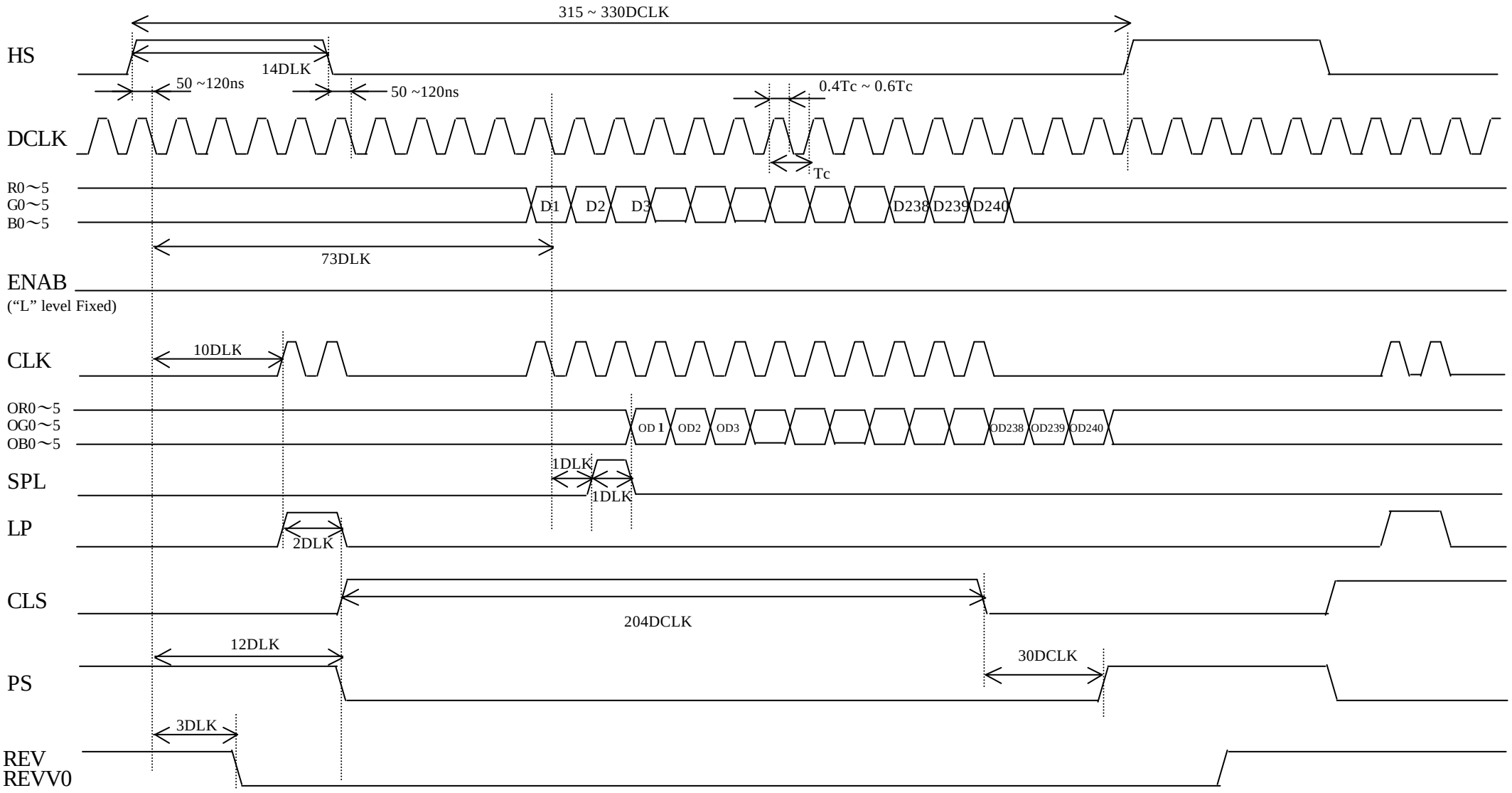

Fig.1-2 Horizontal counter timing chart-a (ENAB signal : L level fixed)

2-1. Landscape type QVGA(320RGB x 240) (SIZEC0 = L level)

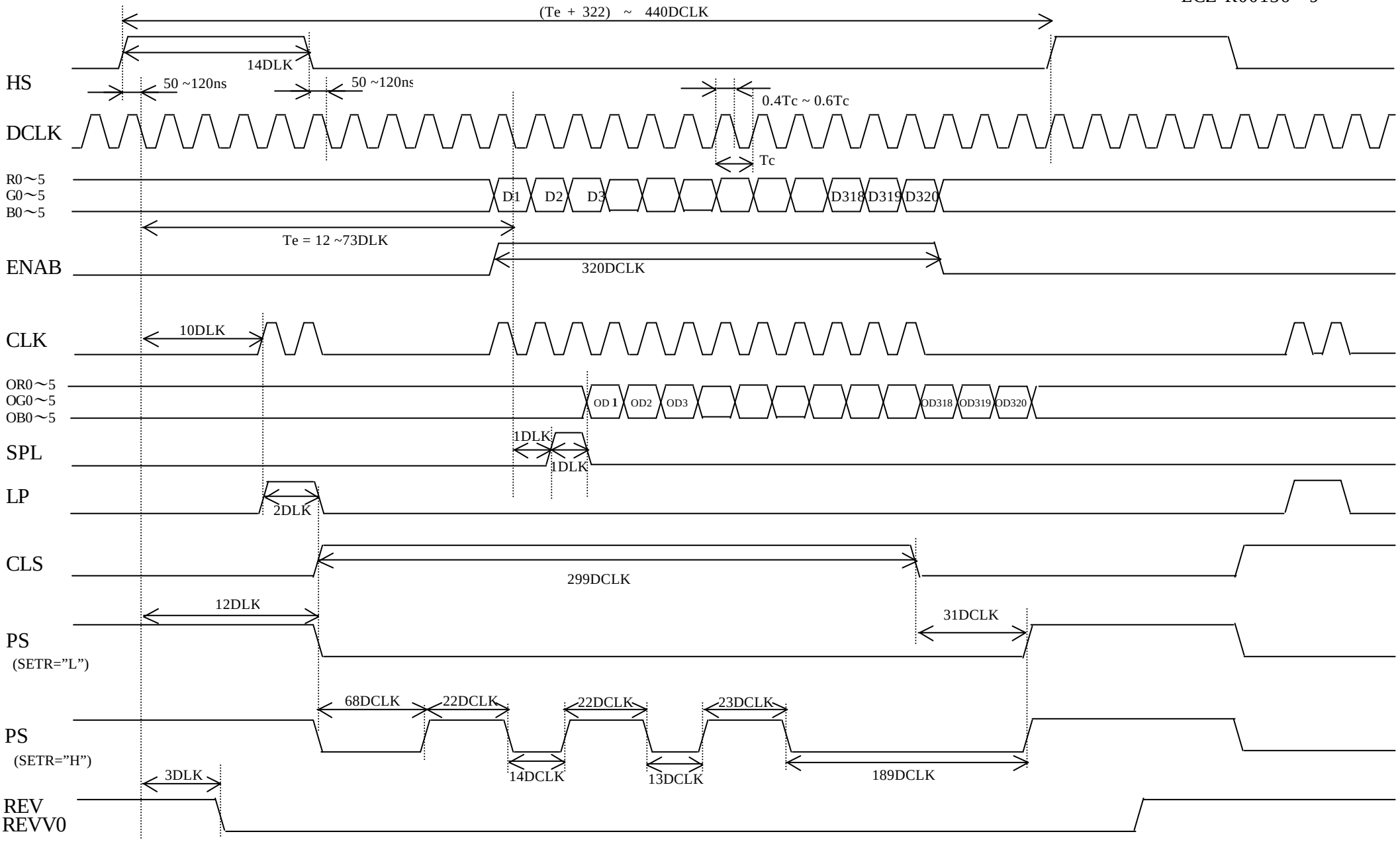

Fig.2-1 Horizontal counter timing chart-a (ENAB signal : valid)

2-2. Landscape type QVGA(320RGB x 240) (SIZEC0 = L level)

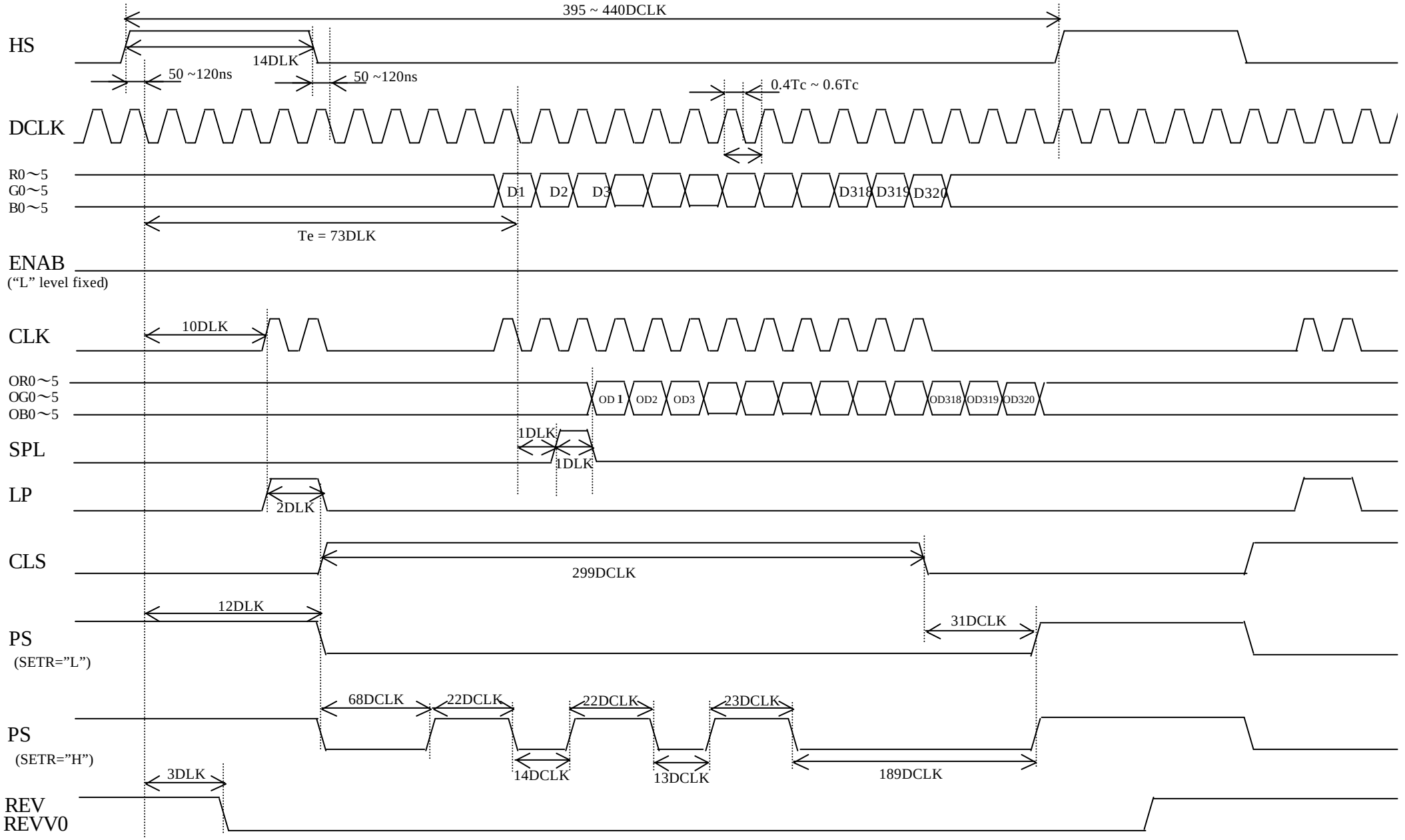

Fig.2-2 Horizontal counter timing chart-b (ENAB signal : L level fixed)

3. Vertical counter timing chart

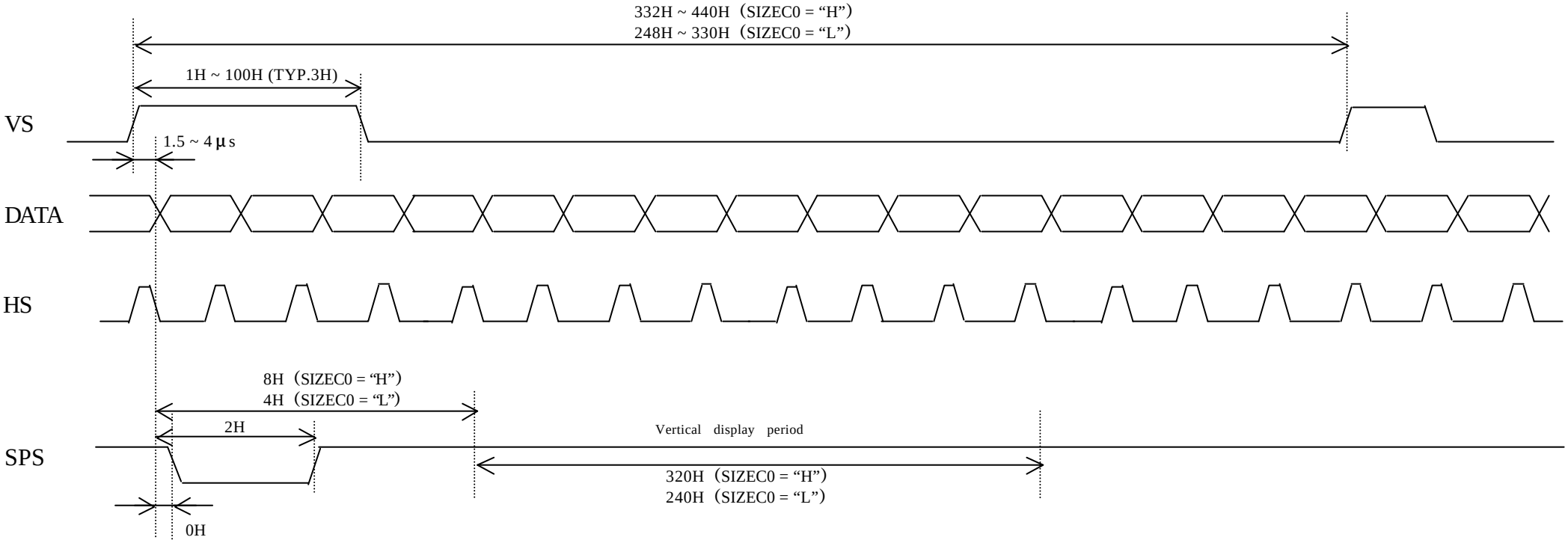

Fig.3 Vertical counter timing chart

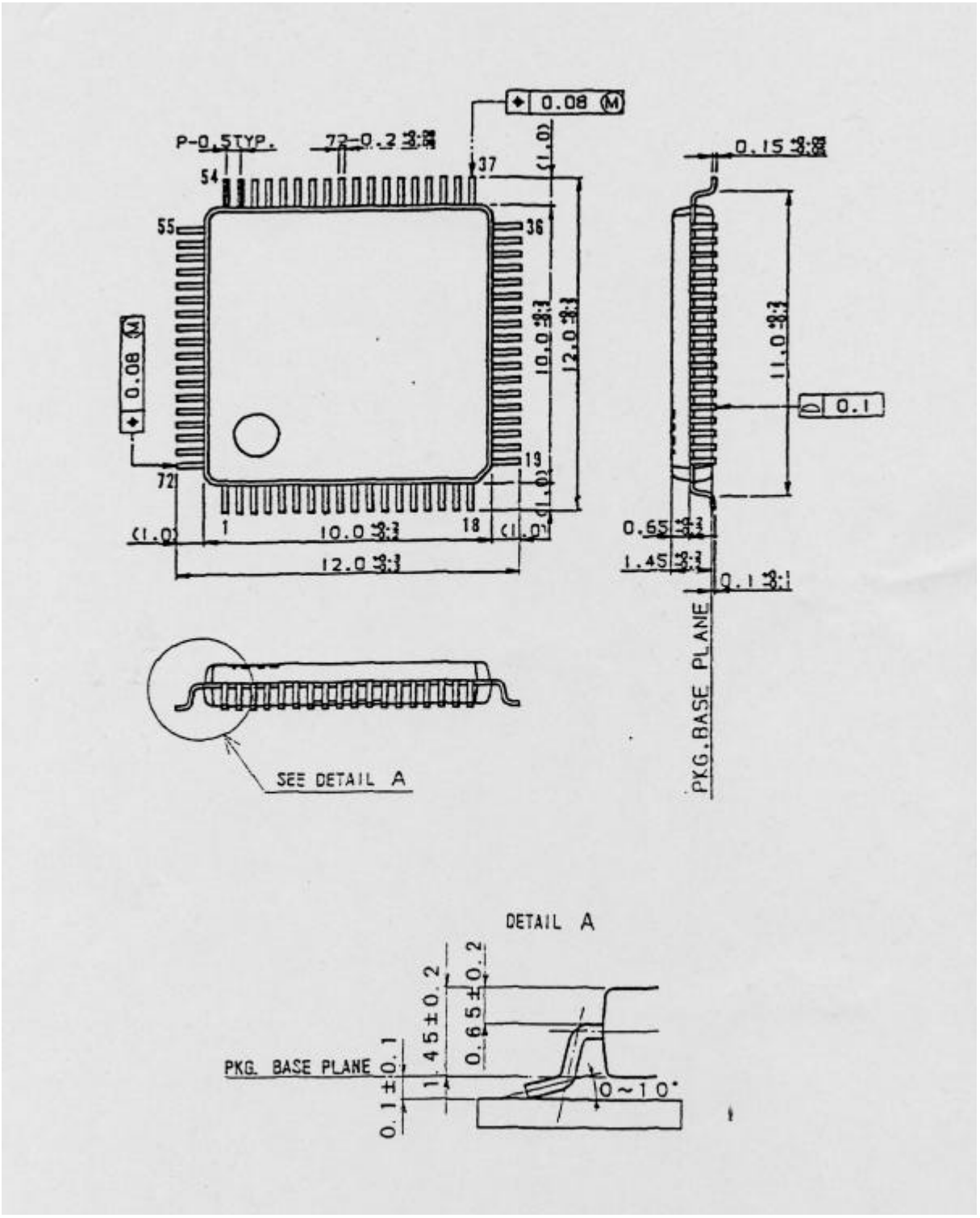

Fig.4. Outline dimentions